Trace Fusing Current Simulation in the Redistribution Layer of Wafer Level Packages

Nathan Whitchurch, JeongMin Ju, JiYeon Yoon, EunSook Sohn, KyungRok Park
Amkor Technology, Inc.
2045 E Innovation Circle
Tempe, AZ 85284 USA
Ph: 480-786-7712; Fax: 480-821-8276
Email: Nathan.Whitchurch@amkor.com

Abstract

This paper uses fusing current data measured from experiments to develop and validate a simulation method in Ansys Mechanical 2022 R1 finite element analysis (FEA) to study fusing current in redistribution layer (RDL) traces on a silicon die. Fusing current was evaluated for several similar trace designs for a range of trace cross-sectional areas and lengths on multiple thicknesses of silicon. Resistances in the experiment were measured by a four-point measurement technique and compared with the nominal resistance over the temperature range as predicted from literature material properties.

Two models were created to demonstrate the simulation approach. First, a model was made to test the fusing current for several lengths and diameters of wire in still air. The model showed only slight (<5%) variation between measured fusing current and simulated fusing current. This simple scenario gives confidence that the simulation approach is valid. Using the combination of transient heating of the wire from a ramped electric current with convection and radiation, the heat balance of the system can reliably simulate fusing current across a wider variety of systems when the surrounding thermal system is included in the model.

The second model was a representation of the Wafer Level Chip Scale Package (WLCSP) with RDL on silicon. The trace geometry and system were modeled, and current was ramped over time across the circuit until the melting point of copper was reached and the trace was considered to have melted and fused. Some variations were observed between measurement and simulation, with thicker silicon showing more capacity to absorb the heating of the trace than in real-world measurements. Overall, simulation aligned well with measurements, with simulation results being between 4 to 14% of the measured fusing current value. The simulation approach appears appropriate to generalize to additional electronics packaging scenarios. Note that dielectrics and material damage such as decomposition from temperature were not considered in this study.

Key words

Current, electrical, fusing, redistribution layer, simulation, thermal, trace, transient, wafer level package

I. Introduction

In recent years, two consistent trends have been observed in electronics packaging: packages are expected to continually increase in performance and simultaneously decrease in size [1]. The trend toward miniaturization across various industries has caused package designs to test the physical limitations of how much current can be passed through a trace before it fails due to Joule heating and fusing. Analytical and empirical solutions for calculating the fusing current, such as Onderdonk, are limited to describing fusing current of long insulated wires or cannot consider the specific and unique environment and heat balance for time scales relevant to electronics packaging [2].

Power delivery within a package is a critical factor that requires significant attention during the design process. As packages continue to get smaller and more feature-dense while power consumption remains constant or increases, the real estate within routing layers devoted to power delivery must be optimized to provide sufficient room for signal routing. This drives the need to understand the physical limits and boundaries that must be respected when determining design rules. The traces must be small enough to be able to route power where it is needed while remaining below the

resistance levels that would lead to: (1) runaway heating and melting of the trace (fusing) or (2) decomposition of surrounding dielectric materials and damage to the package structure.

Copper is the dominant material used for traces in redistribution layers of wafer-level packages. It has relatively low electrical resistance at typical package operating temperatures, but its resistivity increases as temperature increases. Joule heating occurs when electrical current passes through a conductor. While this phenomenon always occurs in every electrical system, it is mort notable and requires consideration when the heat generated within the conductor exceeds the capacity of the surrounding materials to absorb the heat and move it away from the conductor and into the surrounding environment. If the environment is unable to absorb the heat faster than it is generated and the current is sustained over a period of time, the temperature of the conductor increases and can achieve a self-heating feedback loop: copper resistivity increases as temperature increases, which leads to more Joule heating, which leads to additional temperature increase and higher resistivity, creating more heat generation and hotter temperatures, and so on until the current stops or the conductor melts and breaks the circuit.

The foundations for prediction of fusing current were laid by scientists well before the invention of the integrated circuit. Notable contributions to literature were written by W. H. Preece in the late 1800's [4] and by Onderdonk in the 1940's [2]. These studies focus on fusing current of long wires. There is less material published on the topic for the smaller-scale conductors within electronics packages. This paper builds on work presented in [5] and documents an approach for finite-element analysis simulation of fusing current in a wafer level package environment. The simulation approach aims to capture the transient imbalance of heat generation in the conductor against the immediately surrounding materials' heat absorption and compare simulation results against real-world experimental data.

II. Experiment Description

Multiple versions of a silicon block with an array of copper traces were fabricated to represent the redistribution layer (RDL) on a silicon die for a wide variety of scenarios (see Fig. 1). The following parameters were varied in this experiment setup:

a. Trace length
b. Trace cross-sectional area (trace width & thickness)
c. Silicon thickness

Trace routing was also varied, with three patterns: a straight trace, a trace with two 45° corners, and a trace with four 45° corners. There was little difference in the measured trace fusing current for these three patterns, so this paper will focus on the straight trace routing only for the sake of brevity.

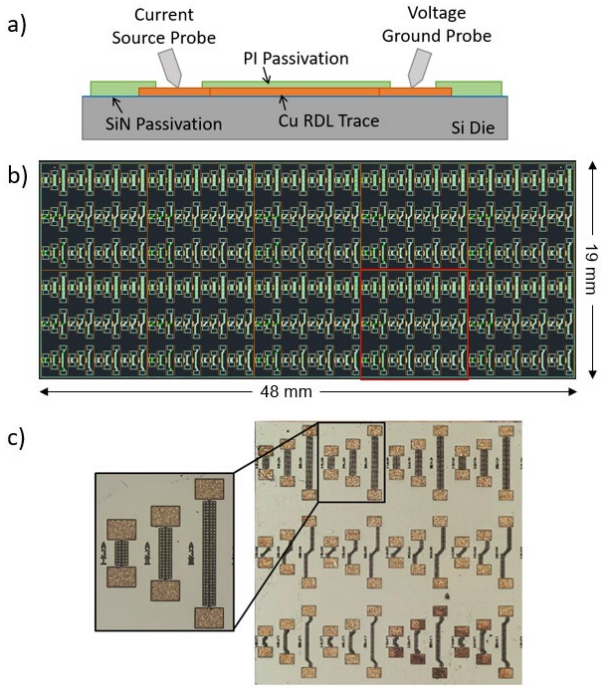

Figure 1 - Experimental test vehicle description: a) cross-section diagram of the test setup, b) design pattern of array of traces on the silicon block; a unit cell highlighted by the red square and c) the microscope image of the unit cell showing multiple trace configurations and surrounding dummy metal.

Current was driven by test probes from a power supply through the trace from the source pad to the ground pad, and current was step-increased over time, with 100 mA incremental increases every 0.5 seconds during the test. A second pair of test probes were applied to the trace pads to measure resistance through the circuit during the test. Each trace configuration was considered fused and the test ended when a discontinuity was observed for resistance measurement as the trace material melted. The experiment results are presented in Fig. 2.

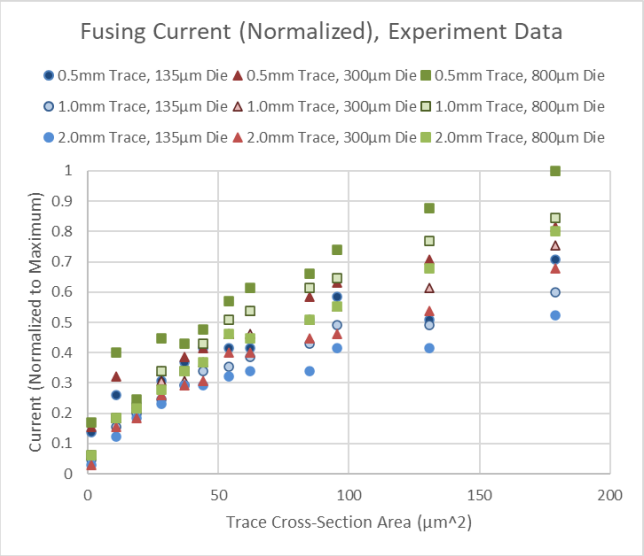

Figure 2 - Experiment results. Note the highest fusing current occurred in the shortest trace with the greatest area on the thickest die. The lowest fusing currents were observed for the longest traces with the smallest area on the thinnest die.

III. Simulation

A. Simulation Introduction and Objective

A simulation model was created in Ansys Mechanical 2022 R1 to explore techniques for simulation of this fusing current experiment. This simulation focuses on three objectives: first, validation of the simulation approach using separate experimental data of bare wire fusing; second, simulation of the wafer level package (WLP) RDL trace fusing experiment; and third, exploration of sensitivity of the system to assumptions and accounting for variations between the experimental results and the simulation results.

B. Simulation Background and Principle

A model for estimation of fusing current must consider several primary factors to achieve valid results. These factors are:

a. key qualities of the trace (its cross-sectional area, length, and material resistivity)
b. the thermal conductivity, dimensions, mass, and heat capacity of the surrounding materials in the system
c. the test current applied over time, and time that the trace is heated during each step
d. the balancing of heat transfer from radiation and convection into the environment around the system.

The "Thermal-Electric" coupled analysis system in Ansys Workbench uses the Mechanical APDL solver. This solver is able to capture the multiphysics electrical and thermal behaviors in this system and is appropriate to use for this simulation. Fusing was not an instantaneous process in this experiment system, nor was it a steady-state process. Therefore, transient simulation was performed to consider the time domain.

C. Baseline wire simulation and proof of concept

A simple bare wire model was created to demonstrate validity of the simulation approach in this paper. This model was compared against a subset of real-world measurement data (the wire fusing current data is from a separate experiment that is not within the scope of this paper). The model used convection and radiation (to ambient) thermal boundary conditions to match and approximate the real-world experimental setup, a ground (0 V) voltage applied to the distal end of the wire segment, and a steadily increasing current applied to the start of the wire segment. The copper resistivity property was from [3] and other physical properties were from [6] (see fig. 3). Wire length and diameter were varied as shown in Fig. 4 with the results presented in Fig. 5. The fusing current magnitude result is the current applied at the model time step where the peak temperature of the wire exceeds the melting point of copper (1086°C).

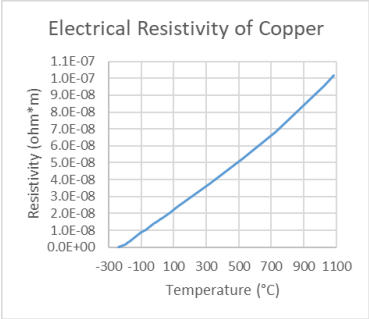

Figure 3 - Temperature dependent electrical resistivity of copper [3]. Note increase in resistivity as temperature increases.

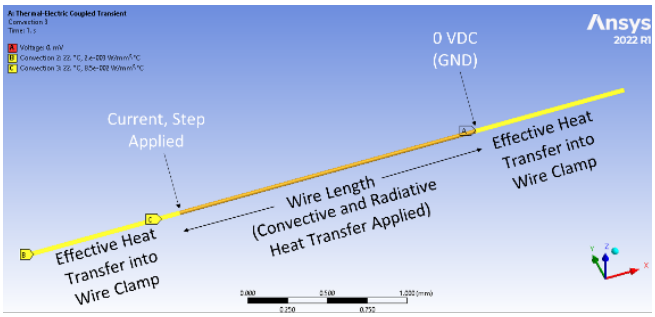

Figure 4 - Simulation setup of simple wire fusing experiment.

These simulation results in Fig. 5 closely match with the experimental measurements for this data set. This supports the position that the simulation tool and the simulation method and approach are able to accurately capture the physical phenomena of the experiment (transient Joule heating) and that the result criteria (fusing occurs at the melting point of the conductor) is appropriate.

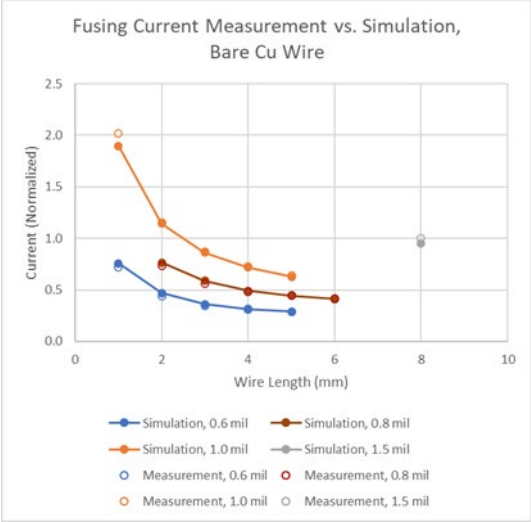

Figure 5 - Simulation results plotted with reference real-world measurement data. Simulation shows very good alignment with measurement data.

D. Model Description

A model of the 48 mm x 19 mm silicon WLP array was created. It was assumed that variation of the experimental results due to position of the traces on the silicon block would be averaged out across multiple measurements of the same trace parameters at different locations in the 5x2 array. Geometry was simplified to only include one trace centrally located on the die. Experimental results appeared to be similar across all three trace geometries (straight, 2-corner, and 4-corner), so only the straight trace geometry was simulated to reduce simulation scope due to time constraints. Future simulation work could include other trace geometries. Non-essential features such as the metal patterning around each trace was neglected. Melting of the copper trace was not simulated directly.

The experimental result set for the straight trace geometry involved four variables: trace width, length and thickness, and die thickness. These were also varied for the simulation task to build the simulation design of experiments (DOE). In total, there were 91 trace fusing current data points simulated in this simulation set. Note that the actual values (as measured) were used for simulation geometry. The trace in the model has an ideal rectangular cross-section and does not consider shape irregularities due to the plating process.

During the simulation setup, it was determined that the thin layer of silicon nitride had a negligible effect on simulation result. It was therefore assumed that this 0.5 µm thick layer of material was similar enough to bulk silicon that the geometry could be neglected to simplify the model and mesh. Likewise, it was observed during testing that the polyimide dielectric layer surrounding the trace appeared to rapidly decompose and burn off relatively early in the fusing test, and a) would generally provide thermal insulation against heat loss to the environment initially, and then b) would not contribute significant thermal mass that would delay fusing significantly. The polyimide layer was therefore also neglected in the simulation model to reduce model size and complexity.

Similar material properties to the copper wire fusing simulation were used for the plated copper trace since the resistivity for copper is documented across the full temperature range of the experiment (from room temperature up to the melting point of the trace). However, physical measurements of the resistance in two traces between room temperature and 300°C showed that the resistivity in the trace averaged approximately 12% higher than the literature value from [3]. It is noted that this material property is the primary factor in Joule heating, so it is expected that variability between documentation resistivity and resistivity in the real-world traces is going to significantly impact error and uncertainty in the measurement and simulation results. The resistance measurement of two traces is presented in Fig. 6 with the data normalized to the expected resistance of each trace at each temperature according to the resistivity in the NIST documentation. Trace resistance appears higher than equivalent drawn wire resistance, however it is outside the scope of this report to draw conclusions about this data.

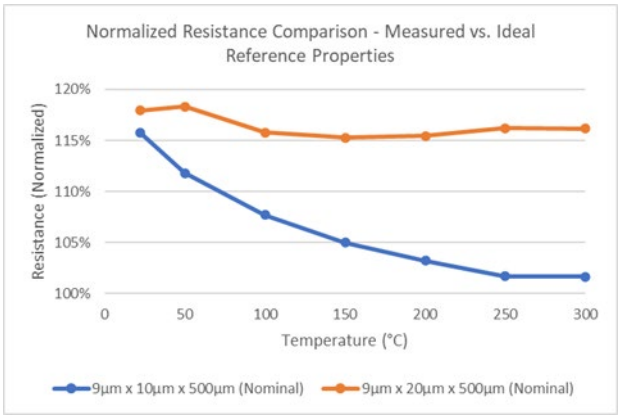

Figure 6 - Measured resistance of two traces versus expected resistance across a temperature range. Note that one trace (plotted in orange) shows a stable 15% to18% higher resistance than expected from reference data, but the other trace (plotted in blue) shows a trend toward matching the reference resistance as temperature increases.

Thermal boundary conditions were applied to the model. Convection from the external surfaces was captured by a small heat transfer coefficient (HTC) appropriate for a combination of convection into still air and radiation to distant room temperature surroundings. The precise value of this HTC was not critical to the model fusing current results since the dominant heat transfer mode during the test duration (typically less than 30 seconds) was via conduction into the surrounding silicon. Even the smallest thickness silicon block had sufficient mass to absorb the Joule heating in the trace

before exceeding an average temperature of 100°C in the model.

The driving current to achieve trace fusing was delivered to the system through a tungsten-tipped probe securely pressed against one trace pad with another matching probe contacting the opposite pad to complete the circuit and ground the end of the trace. The dimensions, location, and placement of these probes was assumed to have a negligible effect on the fusing current results, but they were represented in the model to capture heating introduced into the system by the probes themselves. Silicon and tungsten probe material properties were from [6].

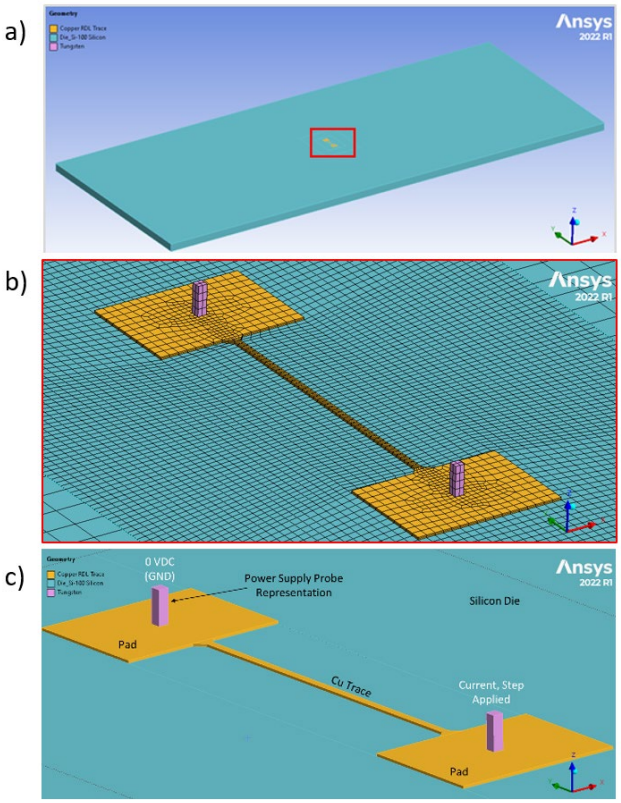

Figure 7 - Model example showing 1 mm x 20.8 µm x 8.6 µm trace on a 0.8 mm thick die, a) the full die and trace, b) detailed view of the trace and model mesh, and c) simulation setup and labels on key bodies in the model.

Fig. 7 shows the model setup and mesh for one of the trace scenarios. In the bottom diagram, the probes are shown in purple. Current in the simulation was applied via a boundary condition with Ansys MAPDL code to the top surface of one of the probes with the other set a 0 Volt reference. The MAPDL code snippet was used to increase the current at discrete time points at a rate that matched the real-world experimental setup. The temperature of the center of the trace was observed at each time substep of the model run, and the trace was considered to be fused when the trace temperature met or exceeded copper's melting point. The simulation is gracefully ended, and the applied current is reported as the fusing current at the time when the melting temperature threshold is met.

E. Result presentation and comparison

The full simulation set of 91 different combinations of trace cross section area, length, and die thickness was run, and results are reported here. One of these scenarios (the 1 mm x 20.8 µm x 8.6 µm trace on a 0.8 mm thick die) was selected to provide a representative example of the typical thermal behavior observed in the simulation system (see Fig. 8). The figure shows the state of the model at the time when the peak temperature in the model exceeded 1086°C. It was observed that the highest temperature occurs at the middle of the trace; this aligns well with observation of the real-world experiment where traces fused primarily near the halfway point along the length of the trace. The trace pads appear several hundred degrees cooler in the model, and the remainder of the system is cooler than the trace region. These images clearly show that heat is conducted horizontally away from the trace through the silicon. It is reasonable to expect that a thicker die will both absorb more heat and spread that heat more efficiently than a very thin die.

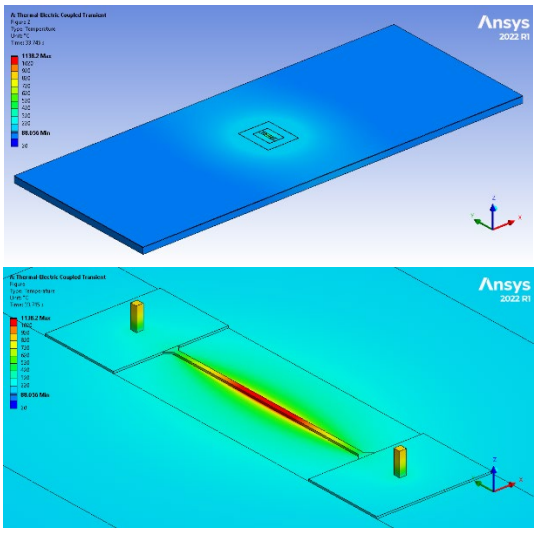

Figure 8 - Resultant thermal contour example plot of the 1 mm x 20.8 µm x 8.6 µm trace on a 0.8 mm thick die. The top view shows the full system model and the bottom view is a close up of the trace region itself. Note the highest temperature occurs at the center of the trace length.

Fig. 9 shows the temperature increase versus time of several different trace geometries during the simulation. These selected result plots show the rapid temperature increase in the last 10% of the time when the ramped current is applied to the trace. For low currents (relative to the cross-sectional area of the trace), the temperature reaches near steady-state before the next current increase. However, as the resistivity of copper increases as temperature increases, there appears to be a point where each increase of temperature also increases

the Joule heating in the trace. This temperature-resistance-heat feedback loop causes the temperature to quickly rise even between current steps, and the maximum temperature in the system rapidly rises to the point when fusing occurs.

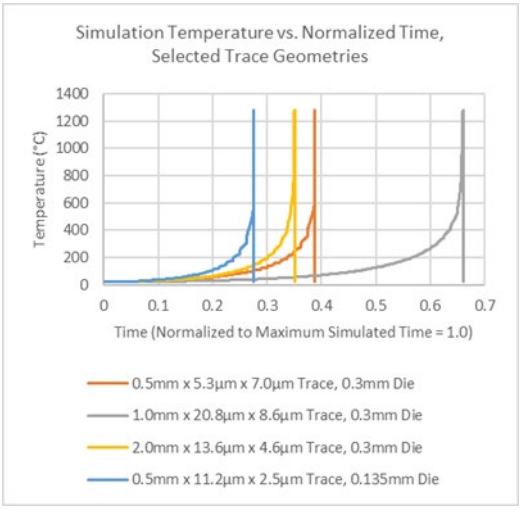

Figure 9 - Temperature vs. time curves of selected trace geometries. Note that time is normalized in this plot.

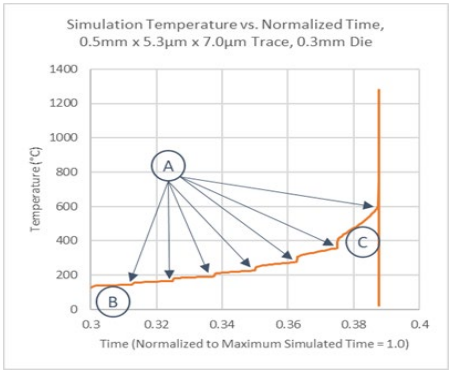

Figure 10 - Temperature vs. time curve with limited time shown on the x-axis. Time is normalized in this plot. Note important phases of the test: A) incremental step increases of the current driven through the trace causes discrete temperature jumps at regular intervals; B) current steps well below the fusing current appear to reach near steady state prior to the next current increment; and C) temperature increases rapidly near the fusing current and fusing time as the resistivity of copper increases with temperature.

The results of the full simulation set compared against the real-world experimental measurements are presented in Fig. 11. Results are organized by trace length.

Simulation results show excellent correlation with the trend of measurement data, with R values for each series ranging from 0.96 to 0.99. However, accuracy of the fusing current magnitude for each trace geometry and die thickness varies significantly, with the thick die showing the worst overall alignment between simulated fusing current and measured fusing current (see Fig. 12). Traces on the thinnest dies showed the best overall alignment between simulation and measurement. Fusing current for longer traces is also better predicted by the model.

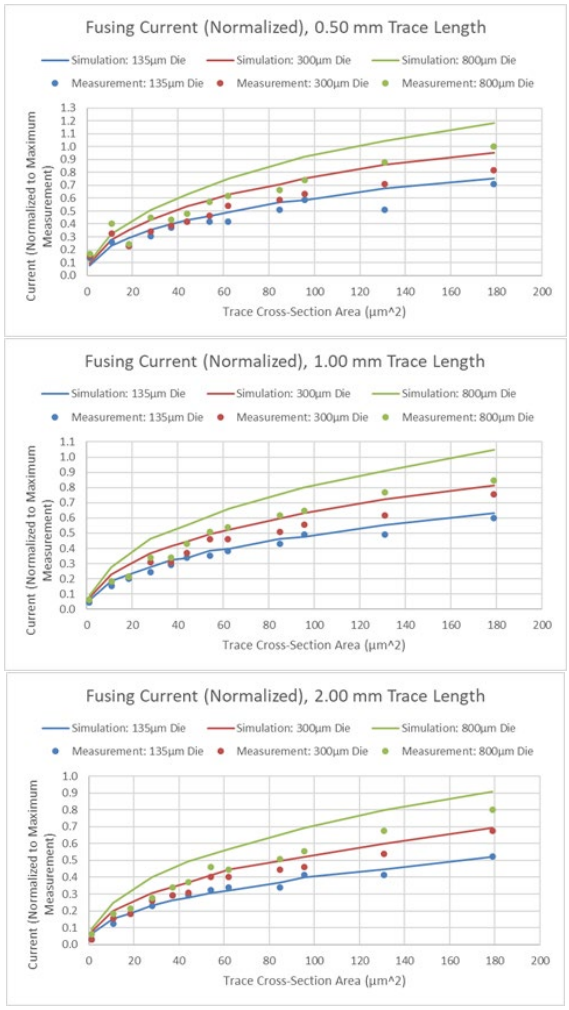

Figure 11 - Simulation results plotted with measurement results for the full simulation data set.

Figure 12 - Comparison of simulation results versus measurement results. Graph shows the average percent difference between each die thickness and trace length combination.

Future simulation work should validate assumptions such as the sensitivity of positioning of the trace on the die (i.e.,

determine how proximity to the edge or corner affects result magnitude). This simulation assumed negligible impact over the data set. In addition, the two-corner and four-corner trace geometries were not studied with simulation. There is an opportunity to further validate the observation that these bends in the trace have minimal impact on fusing current. Note that significantly different trace routing, such as a 2 mm trace that wraps back on itself in a zigzag or S shape, may have different fusing current characteristics due to one length of trace heating an adjacent length of the same trace. The impact of this effect is not studied here and could provide an opportunity for further research.

IV. Conclusions

A method for simulation of redistribution layer trace fusing current was presented in this paper. Simulations align with experiment measurements gathered in a lab environment and correlate well with the trends observed in the real world. Fusing current is a function of the dimensions of the conductor, the material properties of the conductor and the surrounding geometry, and the balance of heat transfer into the environment. Simulation results were reasonably close to the measured fusing current, and simulation data trends were well aligned versus real-world experiment with R values between 0.96 and 0.99. Therefore, it is believed that the simulation methodology shown in this paper is valid and can be used more generally for other trace routings and geometries.

There are several limitations of this paper to acknowledge. First, some differences were observed between simulation and measurement. Die thickness appears to have a much larger impact on fusing current magnitude in simulation than in the real-world experiment. Differences in simulations versus real-world measurements indicate that the resistivity of plated copper traces may be slightly higher than bulk copper resistivity documented in literature. Second, the data measured and modeled was from a test vehicle with limited complexity; any polyimide dielectric was neglected, and the copper trace was directly deposited on the thin passivation layer of the test die. It is reasonable to expect that a trace fully surrounded by polyimide to experience significant degradation of heat transfer out of the trace as the chemical breakdown temperature of the dielectric is approached and exceeded. Finally, only one simple trace shape was modeled, and there is additional opportunity to correlate the measured fusing currents other trace geometries with predictions.

The foundation and building blocks of the simulation method presented in this paper are all well established in the engineering fields: conductive and convective heat transfer, joule heating, energy balance, materials science and material property definition, and CAD geometry modeling are fundamental topics in engineering education and already incorporated into simulation tools and software. These building blocks were applied in this paper to a WLP device, but they are also more generally applicable to the wide array of systems that can be found in electronics packaging. Additionally, future work could extend from this simulation approach to observe and correlate predictions of fusing current due to trace geometry degradation from electromigration in high-current systems over long-term operation with steady-state current. Since the results of real-world measurement and simulation are well matched in this study, and no part of the approach is uniquely limited only to wafer level devices, it is expected that realistic fusing current values can be obtained with these methods for WLP and other package types in the future.

Acknowledgment

The authors of this paper are indebted to Amkor's factory and lab measurement teams, without which none of the real-world data would exist. The skill, dedication, and support of the many people that are involved in our research and development never fails to impress.

References

[1] Laepdus, Mark, "Current And Future Packaging Trends", Semiconductor Engineering, August 2021, https://semiengineering.com/current-and-future-packaging-trends/, retrieved 2024-02-06.

[2] Onderdonk, J. M., "Short-Time Current Required to Melt Copper Conductors," Electrical World 121:26, 98 (1944).

[3] R. A. Matula, "Electrical resistivity of copper, gold, palladium, and silver," J. Phys. Chem. Ref. Data 1 October 1979; 1161. https://srd.nist.gov/JPCRD/jpcrd155.pdf, retrieved 2023-10-24.

[4] Preece, W. H., "On the Heating Effects of Electric Currents", Proc. Royal Society 36, 464-471 (1883). No. II, 43, 280-295 (1887). No. III, 44, 109-111 (1888).

[5] JeongMin Ju, Nathan Whitchurch, JiYeon Yoon, EunSook Sohn, and KyungRok Park, "Fusing Current Characterization of Various Cu RDL Designs in Wafer Level Packages," 2024 IEEE 74th Electronic Components and Technology Conference (ECTC), pp. 661-664, 2024.

[6] F. P. Incorpera, D. P. DeWitt, T. L. Bergman, and A. S. Lavine, "Fundamentals of Heat and Mass Transfer-6th Edition", John Wiley, New York, 2006. pp. 929

[7] Norocel D. Codreanu, Radu Bunea, and Paul Svasta, "Advanced Investigations on PCB Traces Fusing in High Power Applications," 2010 IEEE 16th International Symposium for Design and Technology in Electronic Packaging (SIITME), 2010, pp. 193-196, doi : 10.1109/ SIITME.2010.5652937

[8] Choi, C. S., Shong, K. M., Kim, D. O., Kim, D. W., and Kim, Y. S., "Analysis of dispersive characteristics and structures of copper wire melted by overcurrent," IEEJ Transactions on Power and Energy, 2005, vol.125(12), pp. 1327-1331