Development of high density, enhanced reliability wafer level packages

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Abstract

Fan in and fan out wafer level packages are primarily used in the industry for applications in handheld consumer electronic products. The key benefits of wafer level package (WLP) are small form factor, reduced cost, improved electrical and thermal performance. WLP investigated in this study are directly surface mounted on PCB and have no intermediate substrate. Direct mount of package on PCB, leads to significant CTE mismatch between the package and board which stresses the package solder joint, leading to different failure modes like; cyclic fatigue induced solder joint cracking, package interconnect failure, silicon BEOL failure. Due to these reliability constraints WLP, are limited to relatively smaller sizes and less pin counts. This study investigates development of high pin count, high reliability WLP by ensuring chip package integration at all levels of interconnect; board to package, package to die and die BEOL.

Package development was done with DOE variables like, multi-layer package routing, dielectric materials, solder alloys. Tradeoffs between different DOE variables must be achieved for overall package reliability improvement. Excellent reliability, functional performance, and chip package integration was achieved for highly integrated fan in and fan out wafer level packages.

Key words

Wafer level package, reliability, chip-package integration

I. Introduction

Over the past few years, fan out wafer level package (FOWLP) platform has gained a lot of traction for consumer and hand-held electronic applications. Key FOWLP benefits are:

1. The absence of packaging substrate or reduced substrate layer count enables a smaller footprint area and package thickness.
2. Lack of organic substrate leads to shorter heat dissipation, interconnect path from die to printed circuit board (PCB), thus enabling better thermal and electrical performance of the package.
3. Wafer fab-like fabrication process leads to good process tolerance for high density and fine pitch package interconnects.
4. A low loss and tightly controlled package interconnect scheme also enable the excellent electrical performance of integrated packages, with significantly reduced package interconnect parasitic loss.

There are different flavors of FOWLP that have been developed and exist in the industry today [1-4]. Traditional wafer level fan out is a die first, die down FOWLP that has been in volume production for low end baseband, PMIC, Codec, Wi-Fi, RF kind of applications [1]. A die up high density fan out package process was developed that found adoption for mobile phone processors and DRAM in a package-on-package format [4]. For the high density fan out package, multiple redistribution layers at a relatively fine pitch and high interconnect density are used. To date, most of the traditional wafer level fan out products are limited to single package interconnect layers. For fan in wafer level package (FIWLP), the package routing is confined to the silicon die. FIWLP thus leads to the smallest possible package size. FOWLP and FIWLP that are directly mounted on PCB have limitations in achieving good board level reliability (BLR) performance. During board level temperature cycling (BL-TC) reliability, solder joint cracking is the dominant failure mode. Solder joint cracking results from the cyclic fatigue stress on the solder ball interconnects during BL-TC. The stress arises due to the coefficient of thermal expansion mismatch between the wafer level package and the printed circuit board [5]. Stiffer solder alloys have been evaluated to minimize the fatigue damage due to cyclic stress and thus improve the solder joint fatigue life [6]. However, the higher stiffness of the solder transfers the induced cyclic stress and failure from the solder joint to the package interconnect trace [7]. Wafer level

packages for advanced silicon nodes have fragile low-k and extremely low-k (ELK) back end of line (BEOL) dielectric layers that can crack or delaminate in cyclic fatigue [8, 9]. The focus of this work is to improve the reliability of FOWLP, FIWLP. Design of experiment involving different solder alloys, package design was done to assess package reliability.

II. Package Development Details

Fig. 1 shows the overall fan out package process flow used in this work. The incoming silicon wafer was background to desired silicon thickness followed by laser groove and blade saw. Advanced node silicon in this work had ELK/LK BEOL layers, for which both laser groove and mechanical saw were used to ensure BEOL integrity, and a defect-free die saw process. After die saw the known good die from the fab wafer map were picked and placed active side down on the metal carrier wafer. The die placement and spacing on the metal carrier were determined by the final FOWLP design. After die pick and place, the wafer was molded, and the carrier wafer was removed. This step is followed by a package redistribution layer fabrication process with six or five lithography layers to form the Under Bump Metallization (UBM) or no UBM design versions respectively. After RDL formation, the molded wafer was the background to final package thickness followed by solder ball drop and package singulation into individual units. FOWLP size, solder ball pitch, solder ball count are 7x7mm, 0.4mm, 249 respectively. Fig. 2, shows the FIWLP process flow. Dielectric 1, metal redistribution, dielectric 2 and under bump metallization (UBM) layers are fabricated by wafer lithography process, followed by wafer level solder ball drop. After which the wafer is the background to desired thickness and singulated into individual packages. FIWLP size, solder ball pitch, solder ball count are 4.2x4.2mm, 0.35mm, 114 respectively.

III. FOWLP Process Characterization

As shown in fig. 1, for FOWLP process the first step is wafer backgrind, followed by laser groove and blade saw. The separated dies are then placed face down on a carrier wafer, after which wafer level molding is done followed by package redistribution layer process. During laser groove process high energy laser beams are used to melt/evaporate metal layers from the saw street which are then removed by directional flow of air pressure. However, these molten metals also get redeposited on edges of saw street, generating debris. It's critical to control the height of the laser groove debris because too high debris can penetrate through the dielectric and cause short/leakage failures during package reliability test or field operation. Fig. 3 shows package cross section where after laser groove process optimization debris height less than seal ring height was achieved. Laser groove process can vary across the wafer, so debris and seal ring height were measured across the wafer, for which data is shown in table 1. Laser groove process optimization

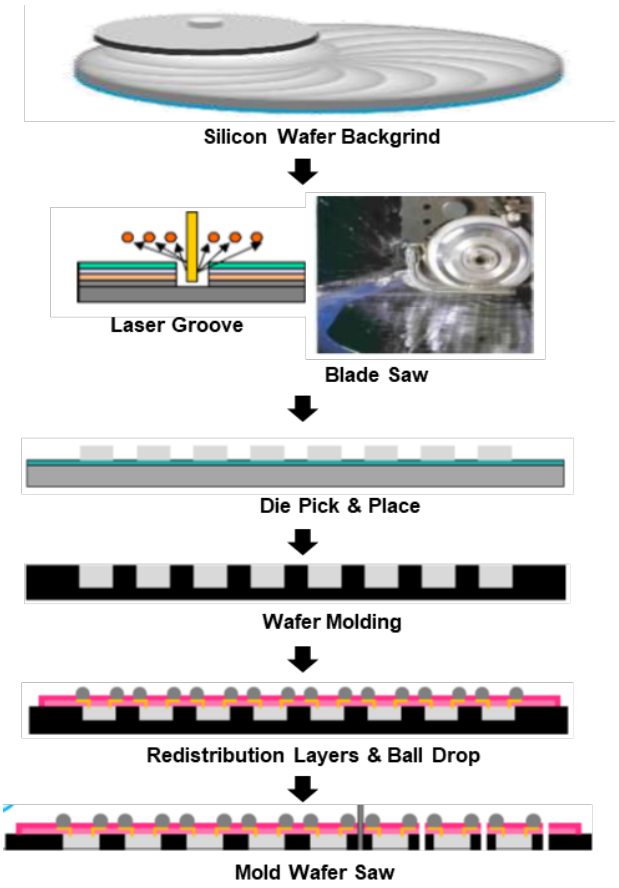

Fig. 1: FOWLP process flow

was done to achieve the following: low metal debris height, complete metal removal, optimum laser groove depth. Laser groove process has significant impact on front side die strength, which is a critical parameter for wafer level packages as these are directly mounted on PCB. Backside die strength is influenced by the wafer grinding process. Process optimization of laser groove, wafer backside grinding, ensured that the measured die strength met the spec.

Fig. 4 and 5 show in process images from the FIWLP and FOWLP. Fig. 4 (a), 5 (a) shows the dielectric 1 vias and probe marks. Vertical probing technology was used to minimize probe induced die pad damage. Also, the dielectric 1 via and probe mark are kept separate by design. This is to ensure that redistribution layer 1 (RDL1) via is not formed on top of the probe mark. Metal via fabrication on top of the probe mark can lead to poor seed layer coverage over the probe mark that can cause seed layer adhesion, coverage issue, resulting in poor electroplating quality, which can cause high via resistance, package reliability issues. For FIWLP and FOWLP RDL via, trace resistance, leakage are measured and monitored during the assembly process. Resistance and leakage measurements are done on test dies with Kelvin probe structures that are included in wafer layout designs for FIWLP and FOWLP. Fig. 5 (d) is failure mode

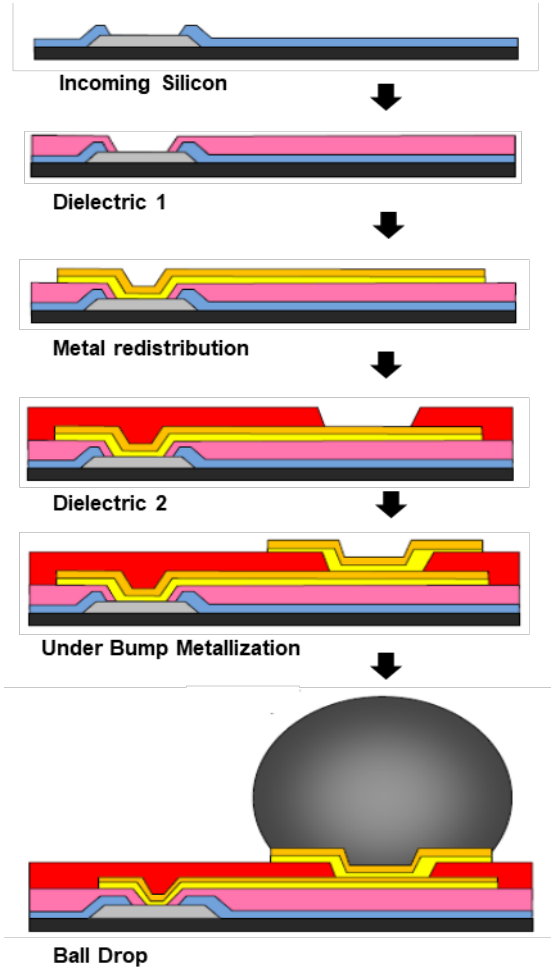

Fig. 2: FIWLP process flow

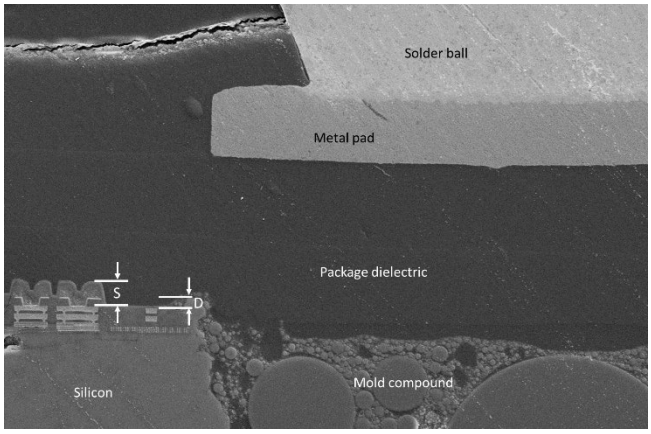

Fig. 3: Laser grove debris height (D) versus seal ring height (S)

Lot number	Parameter (µm)	Position		
		Wafer edge 1	Middle	Wafer edge 2
Lot 1	D	2.78	2.17	1.08
	S	4.56	4.75	4.75
Lot 2	D	2.48	2.98	3.03
	S	4.66	4.71	4.61
Lot 3	D	3.06	2.17	1.81
	S	4.85	4.75	4.29

Table 1: Laser groove debris height versus seal ring measurements

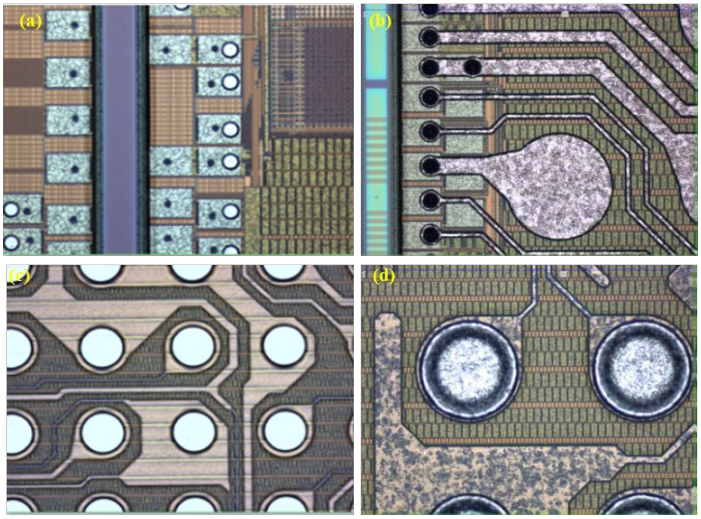

Fig. 4: FIWLP in process images (a) Dielectric 1 via (b) Redistribution layer (c) Dielectric 2 via (d) Under Bump Metallization (UBM)

image after solder bump shear test in FOWLP. Stiff solder alloy is used for FOWLP and still the failure mode is in bulk solder, which is indicative of good integrity of package layers underneath the solder ball pad.

IV. FOWLP/FIWLP Reliability Results and Discussion

Both FIWLP and FOWLP passed the reliability stress conditions of Temperature cycling (TC), -55°C/+125°C/700 cycles, Highly Accelerated Stress Test (HAST), 110°C / 85%RH/3.3V/528h, High Temperature Storage Life (HTSL), 150°C/1000h, Board Level Temperature Cycling (BL-TC), -40°C to 125°C/500 cycles Drop Impact Test 1500 g / 0.5 ms/30 drops, Application Level Temperature Cycling (AL-TC), -40°C to 125°C /600 cycles. During AL-TC a functional product is mounted on a translation board, which then undergoes thermal cycling. To confirm the robustness of product package after AL-TC stress, die passivation was checked after removing all package layers. Fig. 6 and fig. 7 show optical

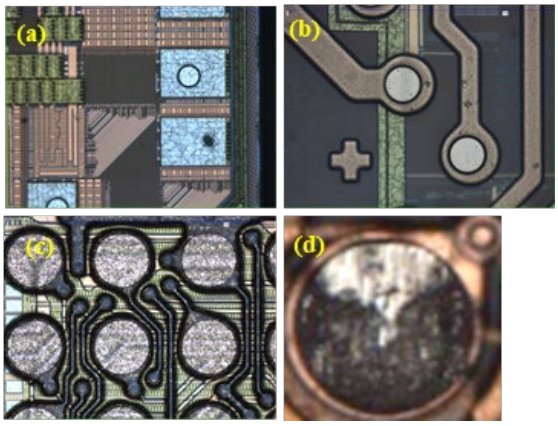

Fig. 5: FOWLP in process images (a) Dielectric 1 via (b) Dielectric 2 via (c) Dielectric 3 via (d) Solder bump shear

images of die passivation. No die passivation cracks or damages can be seen, which further confirms robust chip package integration.

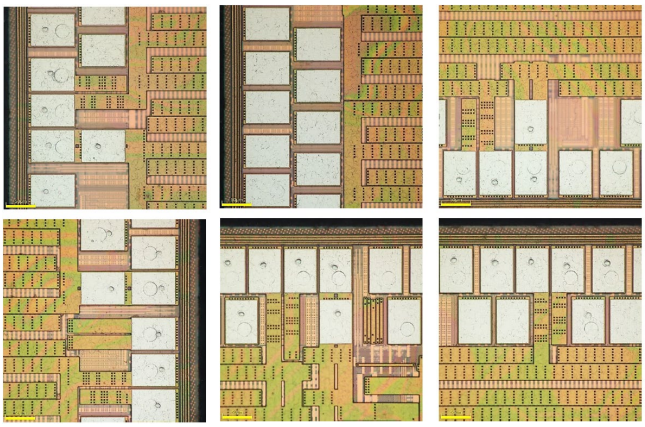

Fig. 6 : FOWLP die passivation images after AL-TC 600c reliability stress. All package layers were chemically removed for die passivation check.

Fig. 8 below is a schematic showing three levels of daisy chain connections in FIWLP: 1st level - PCB, 2nd level - package, 3rd level - die BEOL. Daisy chain package is used for BL-TC reliability. Different test read out points were designed to isolate failure location. To mimic the product design the daisy chain package design and routing are kept same as the product. Three solder alloys with different stiffness are evaluated for BL-TC reliability. Relative stiffness of solder alloys is as follows: SACC>SACB>SACA. Table 2 shows relative first fail of solder alloys, which is as follows: SACA>SACB>SACC. For SACA and SACB the failure mode is bulk solder failure whereas for SACC the failure mode is package trace

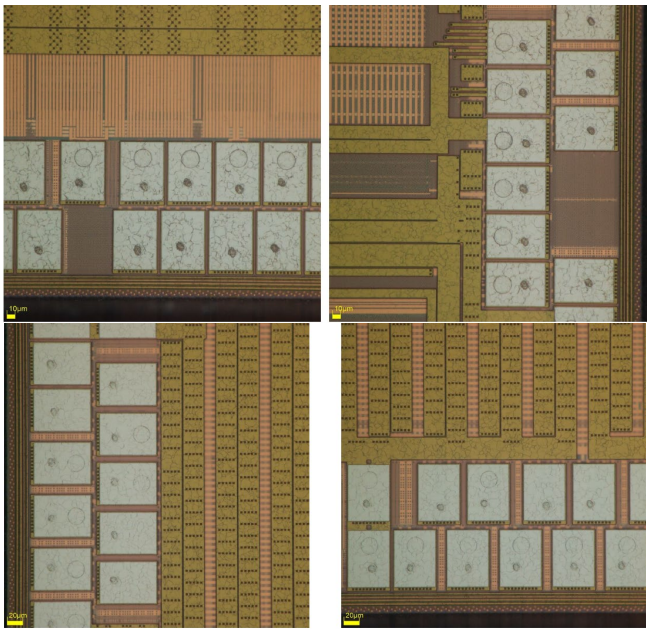

Fig. 7: FIWLP die passivation images after AL-TC 600c reliability stress. All package layers were chemically removed for die passivation check.

cracking. SACC is the stiffest solder alloy, which does not fracture due to BL-TC stress but in turn transfers the high stress to package trace, which is the first to fail. SACB, which is of intermediate stiffness shows an earlier first fail than SACA, despite the failure mode for both being same as bulk solder. As has been reported in our earlier work that though overall stiffness of SACB is higher than SACA, there is a large variation in creep strength of SACB, which can even be lower than SACA [10]. If the lower creep strength of SACB is at critical solder joint, it can fail earlier than SACA. However as shown in table 2, SACA and SACB have comparable BL-TC characteristic life (~63.2% fail). SACC shows the highest characteristic life. The failure mode for SACC is different from SACA and SACB.

Fig. 9 below shows daisy chain connection schematic for FOWLP. The daisy chain runs through PCB, package and die BEOL layers. To mimic product performance the package design for daisy chain is same as product design. Table 3 shows relative BL-TC performance comparison for SACA, SACC, no UBM, UBM legs. For FOWLP, stiff solder alloy leads to quite significant improvement in both first fail and characteristic life. For both SACA and SACC alloys the failure mode is bulk solder alloy fracture. For all cases, the characteristic life is better for UBM versus no UBM. However, with stiff solder alloy SACC, first fail for UBM is earlier than no UBM. For stiff alloy with UBM, the first fail

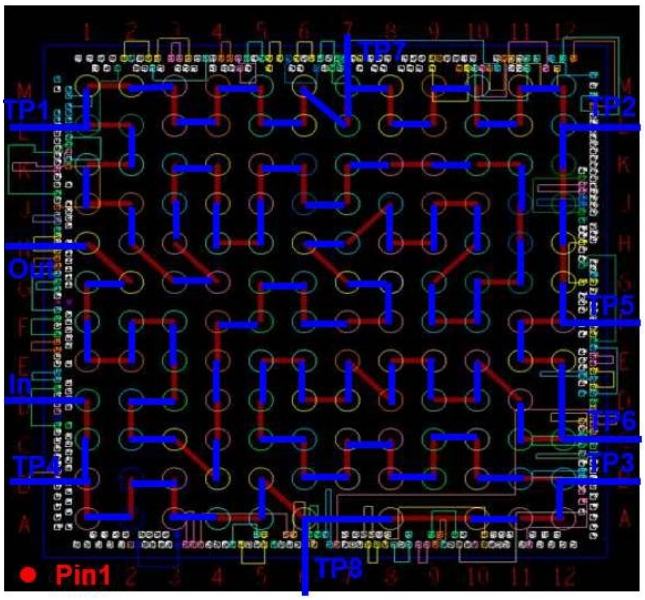

Fig. 8: Schematic showing FIWLP daisy chain connections through PCB (**blue**) and die/package (**red**). Die pads that are connected through the BEOL are also indicated.

Solder alloy	SACA	SACB	SACC
Relative Stiffness	Low	Intermediate	High
Relative first fail	Y	0.8Y	0.6Y
Relative BL-TC CZ life (~63.2% fail)	X	0.97X	1.45X
Failure mode	Bulk solder	Bulk solder	Package trace

Table 2: FIWLP BL-TC reliability comparison for different solder alloys.

is due to PCB trace fracture. Stiff solder alloy, UBM, two metal layers significantly increase the FOWLP strength, and the fatigue stress during BL-TC gets transferred to PCB trace, which becomes the weakest link and first to fail. For package with stiffer solder alloy SACC, a stiffer package dielectric was also used in comparison to package dielectric with SACA solder alloy.

V.Conclusion

FIWLP, FOWLP were developed and qualified to stringent reliability conditions. Solder alloy, dielectric materials, package design variations were used to optimize package performance for critical reliability conditions like AL-TC and BL-TC. For FIWLP using a stiff solder alloy did not improve the BL-TC performance as the first fail mode was changed from bulk solder alloy to early package trace failure. For FOWLP, on the other hand, stiff solder alloy led to quite significant improvement in BL-TC performance. This is

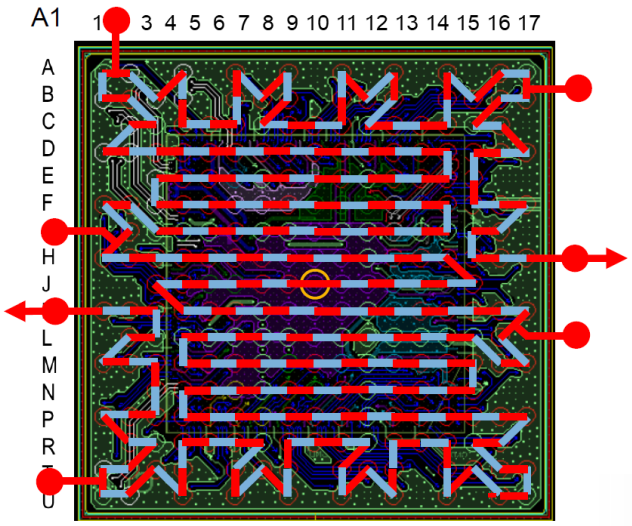

Fig. 9: Daisy chain routing through PCB (**red**) and die/package (**blue**).

Solder alloy	SACA	SACC	UBM
Relative Stiffness	Low	High	
Relative BL-TC CZ life (~63.2% fail)	X	4.4X	No
	1.2X	5.7X	Yes
Relative first fail	Y	4.9Y	No
	1.4Y	3.4Y	Yes
Failure modes	Bulk solder	Bulk solder	No
	Bulk solder	Bulk solder, package trace, PCB trace	Yes

Table 3: FOWLP BL-TC reliability comparison for different solder alloys.

because all FOWLP interconnect layers are robust to handle the higher fatigue stress imposed by the stiff solder alloy. To improve overall chip package integration and reliability a through optimization of overall package structure including solder alloy, package bill of materials, package design is thus required.

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