Fan-Out Chip-Last Panel-Level Packaging for Heterogeneous Integration

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Abstract
In this study, the fan-out chip-last panel-level packaging in fabricating an ultra-large organic interposer of a hybrid substrate for heterogeneous integration is investigated. Emphasis is placed on the design, materials, process, fabrication, and reliability of a hybrid substrate (85 mm x 80 mm) with an ultra-large organic interposer (5 RDLs with the minimum metal line width (L) and spacing (S) = 2 µm) and a 5-2-5 build-up package substrate. Also, some recommendations are provided.

Key words
Organic interposer, heterogeneous integration, hybrid substrate

A. INTRODUCTION

Recently, the large body size substrate is essential to carry on more chips or modules for the application such as AI (Artificial Intelligence), CPO (Co-Packaged Optics) etc. The applications are demanding more chips in one package to ensure the high performance computing and high speed signal transmission.

2.3D IC integration [1-22] is a good way to perform the heterogeneous integration for the large body size substrate since the organic interposer and build-up pack substrate are fabricated by itself which means the known-good-substrate (KGS) before assembly. Also, the objective of 2.3D IC integration is to save cost from the 2.5D IC integration by replacing the TSV (through-silicon via) interposer with the fine metal line width (L) and spacing (S) RDL (redistribution-layer) substrate (organic interposer). On the other hand, organic interposer is with thinner thickness (~0.05 mm-thick) than TSV interposer for shorter signal transmission path for higher transmission speed showed in Figure 1 [1, 2].

In this study, the fan-out chip-last panel-level (515 mm x 510 mm) packaging in fabricating an ultra-large organic interposer of a hybrid substrate for heterogeneous integration is investigated. Emphasis is placed on the design, materials, process, fabrication, and thermomechanical reliability of a hybrid substrate (85 mm x 80 mm) with an ultra-large organic interposer (5 RDLs with the minimum L/S = 2 µm) and a 5-2-5 build-up package substrate. To avoid the most serious problem "warpage" of large body size assembly, a thermal compression bonding (TCB) is used to substitute the mass reflow process.

B. THE STRUCTURE

The hybrid substrate (85 mm x 80 mm x 2.055 mm) assembly of the organic interposer with 4 RDLs and build-up package substrate with reflow method has been demonstrated in [1,2]. In this study a 5-2-5 build-up package substrate (2 mm-thick), and an ultra-large organic interposer (0.05 mm-thick) with 5 RDLs, and the C4 (controlled collapse chip connection) Sn0.7Cu solder joints (~55 µm-thick) with underfill shown in Figure 2 is investigated. Each RDL layer consists of the dielectric layer (P) and metal layer (ML). The line width, spacing, and thickness of P1, … P5, and RDL1, … RDL5 are shown in the table of Figure 3, where the via (V) size between metal layers is also provided.

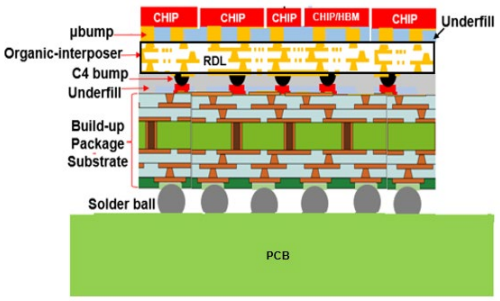


Fig. 1. 2.3D IC integration with ultra-large organic interposer.

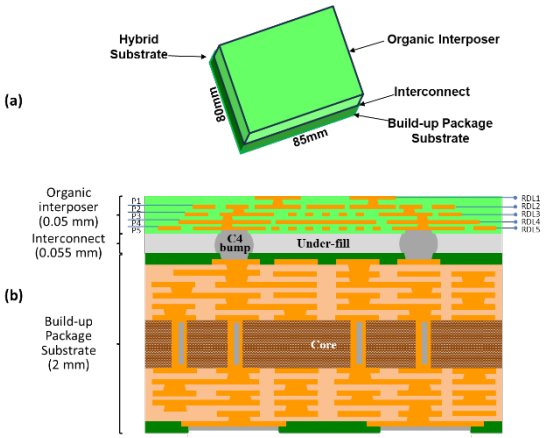
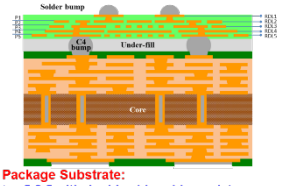


Fig. 2. Hybrid substrate with ultra-large organic interposer. (a) 3D view. (b) Cross-section view.



Package Substrate:
- 5-2-5 with double-side solder resist
- Surface finishing: IT
- Thickness: 2mm
- Size: 98mm x 89mm

Organic Interposer:
- 5 RDLs: 5 metal layers and 5 dielectric layers
- Surface finishing: ENEPIG
- Thickness:0.05mm
- Size: 87mm x 82mm

Hybrid Substrate:
- Organic interposer + package substrate
- Solder joints: ~ 50,000
- Size: 85mm x 80mm

RDLs	Key Elements of RDL	Line width/ Spacing/ Thickness (μm)
RDL1	ML1 (Metal layer 1)*	12/29/8
	P1 (Dielectric between ML1 and ML2)	NA/NA/6
	V_{12} (Via between ML1 and ML2)	20
RDL2	ML2 (Metal layer 2)	8/8/4
	P2 (Dielectric between ML2 and ML3)	NA/NA/5
	V_{23} (Via between ML2 and ML3)	20
RDL3	ML3 (Metal layer 3)	60/30/4
	P3 (Dielectric between ML3 and ML4)	NA/NA/5
	V_{34} (Via between ML3 and ML4)	20
RDL4	ML4 (Metal layer 4)	8/8/4
	P4 (Dielectric between ML4 and ML5)	NA/NA/5
	V_{45} (Via between ML4 and ML5)	20
RDL5	ML5 (Metal layer 4)	8/8/4
	P5 (Dielectric between ML5 and pad)	NA/NA/5

*There are some ML1 with L/S = 2/2μm near the corners of the organic interposer

Fig. 3. Key features and dimensions of the hybrid substrate with ultra-large organic interposer.

C. HYBRID SUBSTRATE

The hybrid substrate of the current study consists of an ultra-large organic interposer, a build-up package substrate, and C4 solder bumps with underfill (Figure 2). The key process steps in fabricating the hybrid substrate are shown in Figure 4, the organic interposer (87 mm x 82 mm) and the build-up substrate (98 mm x89 mm) are bonded together then dicing to 85 mm x 80 mm at once. There are 2 critical issues of large body size hybrid substrate assembly: first is the warpage of organic interposer no matter it is at room temperature or high temperature during assembly, the other one is the void of underfill filling. To reduce the effect of these issues, the material of dielectric and underfill had been changed from [1, 2], and the assembly tool also changed from mass reflow to TCB.

Since the chip side connection pad is intensive in smaller area than the body size of organic interposer (87 mm x 82 mm), the Cu plating uniformity is hard to control with low Cu density for a panel size = 510 mm x 515 mm, therefore the structure is modified to 5 metal layers (5M5P) from 4 metal layers (4M5P) to increasing the pad uniformity and the structures are shown as Figure 5.

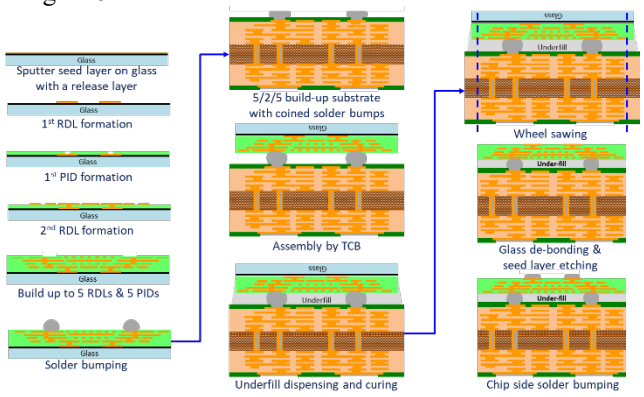


Fig. 4. Key fabrication steps of the hybrid substrate with ultra-large organic interposer.

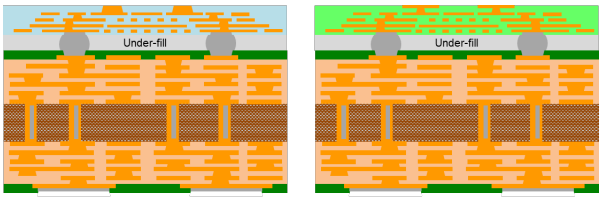


Fig. 5. Hybrid substrate structure schematic with (a) 4M5P organic interposer. (b) 5M5P organic interposer.

C1. Ultra-Large Organic Interposer

The 5-RDLs ultra-large organic interposer (~0.05 mm-thick) is fabricated with the fan-out chip last on a temporary panel process. A released film (sacrificial layer) is slit coating on a temporary glass panel (515 mm x 510 mm x 1.1 mm) and then a Ti/Cu seed layer is deposited by PVD (physical vapor deposition) on the top, as shown in Figure 4. The thickness of the sacrificial layer is 1 μm and it is a light-to-heat conversion (LTHC) film. The contact pad can be obtained by photoresist, laser direct imaging (LDI), development, ECD (electrochemical deposition) Cu, and stripping off the photoresist then etching the seed layer of Ti/Cu. After the metal layer formation, a photoimageable dielectric (PID) is slit coating, exposure and development to form the via as P1, then repeating the same process steps to RDL5 and P5. The solder mask (passivation, P5) can be obtained by slit coating a PID and LDI. Then, the surface is finished with ENEPIG (electroless nickel electroless palladium immersion gold). The C4 solder bumps at 0.15 mm-pitch are formed by stencil Sn0.7Cu solder ball mounting and then reflowed. Two PIDs (PID A and PID B) are considered and their material properties are shown in Table 1. The warpage comparisons between PID A and PID B are shown in Table 2. It can be seen that PID B exhibits smaller warpage than PID A. The higher young's modulus and lower residual stress are assumed to be the reasons.

Item	Condition		Unit	PID	
				PID A (Previous)	PID B (New)
Tg	TMA		℃	280	200
CTE (TMA)	XY	α1	ppm/℃	60	60
Dk	@20 GHz		-	3.0	2.9
Df	@20 GHz		-	0.02	0.02
Td (5%)	TGA		℃	350	335
Young's Modulus	-		GPa	2.0	3.5
Tensile Strength	-		MPa	132	130
Elongation	-		%	59	50
Residual Stress			MPa	29	19

Table 1. PID material properties of organic interposer

4M5P Organic interposer with PID A				5M5P Organic interposer with PID B			
Temp. (°C)	Warpage (μm)	Variation with RT. (%)	Moiré photo	Temp. (°C)	Warpage (μm)	Variation with RT. (%)	Moiré photo
30	-247.1	N/A		30	-232.5	N/A	
158	-31.2	-87.37		158	-42.1	-81.89	
260	-85.1	-65.56		260	-26.0	-88.82	
160	-161.5	-34.64		160	-145.2	-37.55	
31	-333.3	34.88		31	-266.1	14.45	

Concave: "-"; Convex: "+"

Table 2. Warpage comparison between PID A and PID B

C2. Build-up Package Substrate

The 5-2-5 build-up package substrate (98 mm x 89 mm x 2 mm) is fabricated on a 510 mm x 510 mm panel by a conventional method. The coined C4 solder bumps are formed by stencil Sn0.7Cu solder ball mounting and then reflowed and pressed. There are solder resists on both sides of the substrate and the surface finishing is IT (immersion tin).

C3. Hybrid Substrate

The final assembly of the hybrid substrate is by TCB. Since the large body size tool is not matured in the market yet. In this study, we use Toray TCB tool, Figure 6 and the tool information is shown in Table 3.

The temperature monitoring by 9 points with thermal couple at the sample edges and center as shown in Figure 7. The bonding head and carrier stage are set to 275°C, and the temperature spec is 265 ± 10°C. The temperature delta is only 5°C with very high stability as Figure 8.

The individual (87 mm x 82 mm) organic interposer with the temporary glass carrier on the individual (98 mm x 89 mm) build-up package substrate with flux spray and then do the TCB process as the tuned conditions of temperature 275 °C, force 15 N, press down 30 μm with 6.8 °C/sec heating up gradient of 25 sec, and 2 °C/sec cooling down gradient of 45 sec, which means the total process time of TCB is 70 sec as shown in Figure 8.

Item	Value
Alignment accuracy (3σ)	1 μm
Available heater (bonding head)	☐ 12 mm, ☐ 16 mm, ☐ 22 mm, ☐ 32 mm, ☐ 52 mm, ☐ 80 mm, 120x80 mm, ☐ 130 mm
Force	10~490 N (Ultra low pressure head: 0.1~9.8 N)
Available pulse heater on stage side	☐ 12 mm, ☐ 16 mm, ☐ 22 mm, ☐ 32 mm, ☐ 52 mm, ☐ 80 mm, 120x80 mm, ☐ 130 mm
Available heater (stage) (constant: ~150 °C)	Φ12 inch, ☐ 300 mm

Table 3. Toray TCB tool information

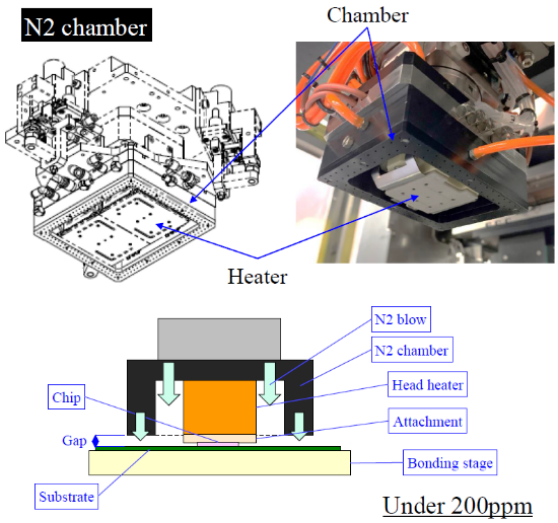
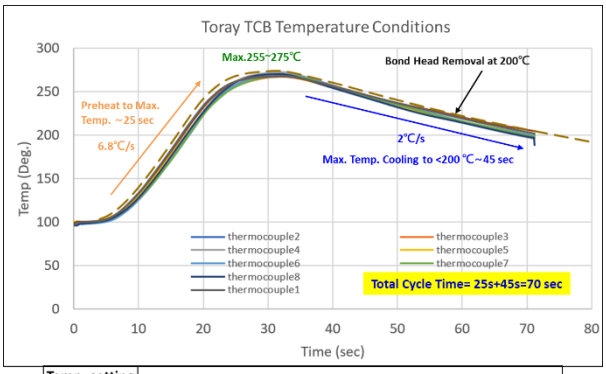


Fig. 6. Toray TCB tool schematic.

Fig. 7. Temperature monitoring positions of device-under-test by thermal couple.



Temp. setting (°C)		Monitoring position								
Bond head	Stage	1	2	3	4	5	6	7	8	9
275	275	267.6	269.8	268.7	272.3	268.5	269.3	268.7	270.4	267.3
Target spec		Max temp.		Min. temp		Avg.		Std.		Range
265 ± 10		272.3		267.3		269.2		1.52		5

Fig. 8. Temperature monitoring results of devices under test.

After TCB, underfill dispensing is the next step. In order to reduce the void in underfill due to the large body size, the underfill type was changed from [1, 2] to a low viscosity type as shown in Table 4. Low viscosity underfill also reduced the process time of dispensing about 3 times from 10.3 minutes [1,

2] to 3.5 minutes. However, as the result shown in Figure 9, the void still existed in underfill even decreasing the viscosity. But the number of voids is greatly reduced.

The coplanarity of the hybrid substrate during processes is shown in table 5. It can be seen that the coplanarity, in average, is 0.775 mm (convex) after TCB and increases to 0.930 mm (convex) after underfill process but decreases to 0.464 mm (convex) after edge singulation. The final structure after temporary glass removal, it is only 0.030 mm (concave). It's basically a flat surface for further chip assembly.

Feature				Under-fill	
				Type A (Previous)	Type B (New)
Filler	Content		wt%	67	60
	Size	Mean	µm	1.0	0.6
		Max		5	3
Viscosity	25 °C, 50 rpm		Pa.S	55	20
Tg	DMA		°C	115	110
	TMA			95	88
CTE	<Tg		ppm/°C	22	28
	>Tg			80	105
Storage modulus	<Tg		GPa	11.0	9.9
	>Tg			0.20	0.08
Curing condition				165 °C/2 hrs	165 °C/2 hrs

Table 4. Underfill material properties comparison

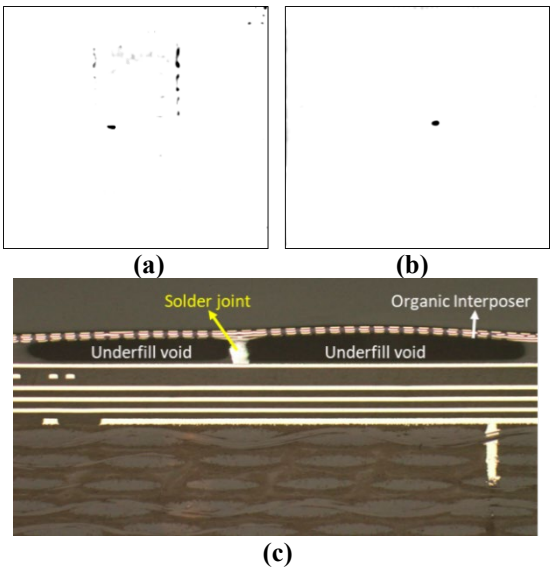


Fig. 9. Underfill void (a) previous underfill (b) new underfill (c) x-section of new underfill void.

By the optimal TCB conditions, the good interconnection of joint height is about 55 µm and joint size is about 110 µm as shown in Figure 10.

Process	Structure	Coplanarity (mm) 1	2	3	4	Statistics	
After TCB						Max	0.812
						Min.	0.750
		0.7758	0.7500	0.8124	0.7625	Avg.	0.775
After under-fill						Max	0.985
						Min.	0.828
		0.9851	0.9259	0.8279	0.9829	Avg.	0.930
After singulation						Max	0.472
						Min.	0.457
		0.4629	0.4627	0.4724	0.4571	Avg.	0.464
After glass removal						Max	-0.035
						Min.	-0.024
		- 0.0291	- 0.0236	- 0.0311	- 0.0348	Avg.	-0.030

Concave: "-"; Convex: "+", only points the shape

Table 5. Coplanarity comparison of processes

Before the optimal hybrid substrate, there are some assembly defects observed like untouched joint in Figure 11 (a) stretched joint in Figure 11 (b), flattened joint in Figure 11 (c) and HIP (head-in pillow) joint in Figure 11 (d). The bonding force, pressing down depth, temperature and alignment are all important factors for a good bonding process.

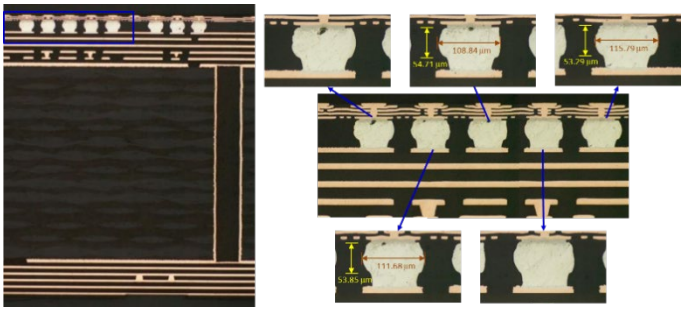


Fig. 10. Cross-section of joints for the optimal hybrid substrate.

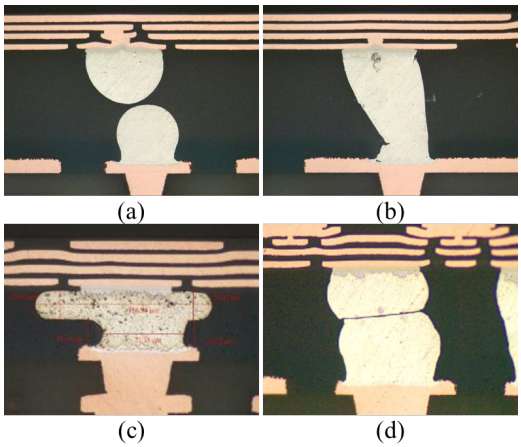


Fig. 11. Cross sections of the solder joint during condition tuning (a) untouched joint (b) stretched joint (c) flattened joint (d) HIP joint

D. ELECTRICAL TEST & THERMAL CYCLING TEST

The joints O/S (open/short) yield by TCB in this study increases to 99% from 85~95% [1,2] by reflow process. The yield loss of reflow process is along the edge positions shown in Figure 12 (a), however, the TCB process can reduce the warpage influence during bonding to improve the yield shown in Figure 12 (b).

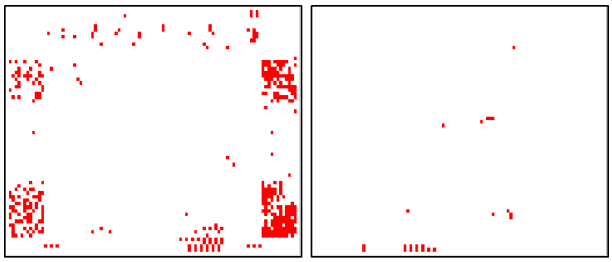


Fig. 12. Opened joints mapping after assembly to the 85 mm x 80 mm hybrid substrate (a) Reflow method (b) TCB method.

Thermal cycling test (TCT) to confirm the solder joint reliability result (-55ºC ↔ 125ºC), and precondition L3a before TCT. The samples of condition tuning also do the TCT for the connection yield comparison. The sample A (with the optimal conditions) O/S yield is over 99% among after assembly, and the sample B and sample C (the samples during conditions tuning) are about 90%, after TCT 500 cycles and after TCT 1000 cycles. The O/S yield variations of the TCT samples are with less variation < 1%, it means most of the joints are stable with good connection result.

	Assembly	TCT 500 cycles	TCT 1000 cycles
Sample A	>99%	>99%	>99%
Sample B	90~91%	90~91%	90~91%
Sample C	86~87%	86~87%	86~87%

Table 6. Hybrid substrate O/S yield of TCT (Sample A: with

E. SUMMARY

Some important results are summarized as follows.

- The feasibility of design, materials, process, fabrication, and reliability of a hybrid substrate (85 mm x 80 mm) which consists of an ultra-large organic interposer, build-up package substrate, and solder joints with underfill has been demonstrated.
- The ultra-large organic interposer consists of 5 RDLs with L/S = 2 µm (minimum) and a thickness of 50 µm [1]. The PID is with a CTE = 60x10^{-6}/ºC. The organic interposer (87 mm x 82 mm) has been fabricated by a fan-out RDL-first process on a large glass temporary carrier (515 mm x 510 mm x 1.1 mm).
- The build-up package is 5-2-5. The ABF is with a CTE = 20x10^{-6}/ºC and 49x10^{-6}/ºC. The build-up package substrate (98 mm x 89 mm x 2 mm) has been fabricated by an ordinary process on a 510 mm x 510 mm x 2 mm panel.
- The final assembly of the hybrid substrate is by TCB process to connect the organic interposer and the build-up package substrate with >50,000 Sn0.7Cu solder bumps.
- Underfill dispensing of the gap between the organic interposer and build-up package substrate with 50,000 solder joints of such a large hybrid substrate has been a big challenge. In this study, the void still observed even use the low viscosity underfill material. Thus, there are rooms for improvement.
- After underfill, it is wheel sawing the 4 sides into an 85 mm x 80 mm hybrid substrate.
- The coplanarity of the hybrid substrate (without the temporary glass carrier) has been measured with a small value of 0.03 mm. The value of the warpage depends on the hybrid substrate thickness and material. Usually, the thicker the substrate the smaller the warpage. The CTE of the dielectric material also plays a very important role on the warpage.
- The yield of O/S test of the optimal conditions (Sample A) is over 99%, the full around interconnections of such large body size is a big challenge.
- The reliability of TCT showed < 1% variations of O/S yield, almost interconnection solder joints are with good connection.
- There are still some rooms to be improved of the yield of conditions tuning, material selection and processes improvement.

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