Solder Joint Reliability of Glass Core Substrate Assembly

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Abstract
The thermal-fatigue reliability of flip chip micro solder joints on glass core build-up package substrate and C4 (controlled collapse chip connection) solder joints on printed circuit board (PCB) is investigated. Emphasis is placed on the structural deformation and the accumulated inelastic strain at the critical locations of the micro and C4 solder joints. Some recommendations are also provided.

Key words
Glass core substrate, organic core substrate, solder joint reliability, Anand constitutive model

I. INTRODUCTION

So far, reliability issues because of the glass core substrate are seldom discussed. In this study, the solder joint reliability because of the glass core substrate is investigated. Figure 1 shows the structures under consideration. In order to make the µbump solder joint reliable between the chip and the build-up package substrate the coefficient of thermal expansion (CTE) of the glass core substrate is made to be as close as the Si chip. In this case, the thermal expansion mismatch between the glass-core build-up package substrate and the PCB is increased and the C4 solder joint reliability is questionable!

In this study, the solder cap of the µbump is made of Sn0.7Cu (melting point = 227°C) and the solder of the C4 bump is made of Sn3Ag0.5Cu (or SAC and the melting point = 217°C). Both solders obey the Anand constitutive model [1-6], i.e., the thermal-fatigue reliability of the solder joints is performed by a nonlinear temperature and time dependent finite element analysis.

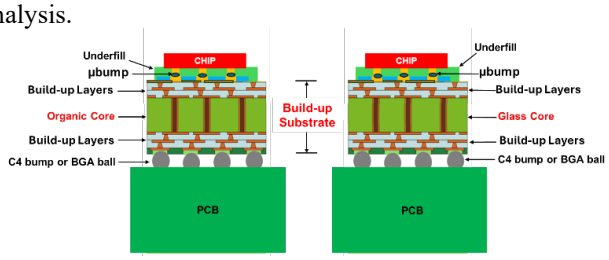

Fig. 1 Cross section of the structures.

II. THE STRUCTURES

Figure 1 schematically shows the structures under consideration. The silicon chip (10mm x 10mm x 350µm) is supported by a build-up package substrate (20mm x 20mm x 832µm), which is fabricated by the conventional material such as the organic core (800µm-thick) and the new glass core (800µm-thick) material. There are two build-up layers on the core's top and bottom sides which are fabricated by a PID (photoimageable dielectric) for the dielectric layer (5µm-thick) and electrochemical deposition (ECD) Cu for the metal layer (3µm-thick).

III. FINITE ELEMENT MODELING

Due to double symmetries of the structure shown in Figures 1 and 2, only a quarter of the structure is modeled (Figure 3). Figure 3 shows the chip, package substrate, PCB, µbumps and C4 bumps. Finner meshes are used for the critical locations (higher stress/strain areas) such as corner µbumps connecting the chip and the build-up package substrate and the corner C4 bumps connecting the build-up package substrate and the PCB.

The displacement/rotation boundary conditions along the x-axis are that there is no displacement in the y-direction (UY = 0), and there is no rotation about the x-axis and the z-axis. The boundary conditions along the y-axis are that there is no displacement in the x-direction (UX = 0), and there is no rotation about the y-axis and the z-axis. At the center, the boundary conditions are that there are not any displacement and rotation.

Since the focus of the present study is on the solder joint reliability, in order to simplify the modeling and save the computing time, the organic and glass build-up package substrates are modeled as an equivalent block which will be discussed in the next section. For both structures, the number of elements, the distribution of mesh sizes, and the modeling are the same, except the effective material properties of the equivalent block.

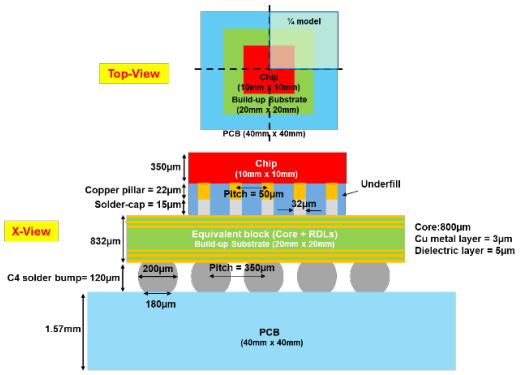

Fig. 2 Top-view and Cross-section view of the structure.

III. MATERIAL PROPERTIES

Table 1 shows the material properties for modeling. All the materials are assumed to be constant except solder (Sn3Ag0.5Cu), which is time and temperature dependent. Also, the solders, Sn3Ag0.5Cu and Sn0.7Cu, obey the Anand viscoplasticity constitute equation. The Anand flow equation which governs the inelastic strain ε has the following form [1-6]:

$$\frac{d\varepsilon}{dt} = A\left[\sinh\left(\frac{\xi\sigma}{s}\right)\right]^{1/m} \exp\left(-\frac{Q}{RT}\right)$$

where $d\varepsilon/dt$ is the inelastic strain rate, A is the pre-exponential factor, Q is the activation energy, R is the universal gas constant (8.314 $J{\cdot}K^{-1}{\cdot}mol^{-1}$), T is the absolute temperature (Kelvin), ξ is the multiplier of stress, σ is the equivalent stress, m is strain rate sensitivity. The evolution equation which defines an internal variable s of the model, and its saturation value is:

$$\frac{ds}{dt} = \left\{h_0(|B|)^{\alpha}\frac{B}{|B|}\right\}\frac{d\varepsilon}{dt}$$

where

$$B = 1 - \frac{s}{s^*}$$

and

$$s^* = \hat{s}\left[\frac{d\varepsilon_p/dt}{A}\exp\left(\frac{Q}{RT}\right)\right]^n$$

where h_0 is the hardening/softening constant, a is the strain rate sensitivity of hardening/softening. The quantity s^* represents a saturation value of deformation resistances. $\hat{s}$ is a coefficient, and n is the strain rate sensitivity for the saturation value of deformation resistance, respectively. The evolution equation has an extra initial condition of $s(0) = s_0$, where s_0 is the initial value of s at initial time $t = 0$. The loading-unloading criterion and viscoplastic flow occurs for yield criterion or an any non-zero stress. The Anand model does not have an explicit criterion or a loading-unloading criterion and viscoplastic flow occurs for any non-zero stress.

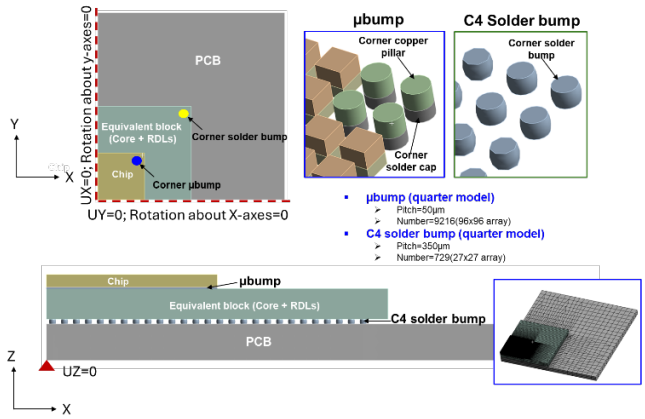

Fig. 3 Finite element modeling of the structure.

Table 1 Material properties for simulations.

Materials	Young's modulus (GPa)	Poisson's ratio	CTE ($10x^{-6}$/°C)
Silicon	131	0.278	2.8
µbump (Sn0.7Cu)	30	0.3	22
C4 bump (SAC305)	49 - 0.07T(°C)	0.3	21 + 0.017T(°C)
PCB	$E_x = E_y = 22$; $E_z = 10$	0.28	$\alpha_x = \alpha_y = 18$; $\alpha_z = 70$
Underfill	4.5	0.35	50
RDL (Dielectric)	2.0	0.3	60
RDL (Copper)	121	0.34	16.3
Glass core	72	0.29	4.8
Organic core	24	0.3	$\alpha_x = \alpha_y = 10$; $\alpha_z = 24$
Equivalent block (Glass core + RDLs)	71	0.29	6.3
Equivalent block (Organic core + RDLs)	25	0.3	$\alpha_x = \alpha_y = 11.3$; $\alpha_z = 24.8$

There are a total of nine (9) constants (parameters) of the Anand equation (model), namely A, Q, ξ, m, s, n, h_0, α, and s_0. For Sn3Ag0.5Cu (SAC) [1-5] and Sn0.7Cu [4, 6], these constants are shown in Table 2.

Table 2 Anand parameters for Sn3Ag0.5Cu (SAC305) and Sn0.7Cu.

Anand Model		
Parameters	**SAC305**	**Sn0.7Cu**
s_0 (Pa)	$18.07x10^6$	$33.8x10^6$
Q/R (K)	9096	5276
A (s^{-1})	3484	9875
ξ	4	2
m	0.2	0.176
h_0 (Pa)	$1.44x10^{11}$	$61987.3x10^6$
ŝ (Pa)	$26.4x10^6$	$65.2x10^6$
n	0.01	0.003
a	1.9	1.03

The effective material properties of the organic build-up equivalent block can be calculated by the following and are summarized in Table 1.

For equivalent Young's modulus:

$$\frac{121\times(3*4)+2\times(5*4)+24*800}{(3*4)+(5*4)+800} = 25\text{GPa}$$

For equivalent CTE in X and Y:

$$\frac{16.3\times(3*4)+60\times(5*4)+10\times800}{(3*4)+(5*4)+800} = 11.3\text{x}10^{-6}/^{o}\text{C}$$

For equivalent CTE in Z:

$$\frac{16.3\times(3*4)+60\times(5*4)+24\times800}{(3*4)+(5*4)+800} = 24.8\text{x}10^{-6}/^{o}\text{C}$$

For equivalent Poisson's ratio:

$$\frac{0.34\times(3*4)+0.3\times(5*4)+0.3\times800}{(3*4)+(5*4)+800} = 0.3$$

The effective material properties of the glass build-up equivalent block can be calculated by the following and are summarized in Table 1.

For equivalent Young's modulus:

$$\frac{121\times(3*4)+2\times(5*4)+72*800}{(3*4)+(5*4)+800} = 71\text{GPa}$$

For equivalent CTE:

$$\frac{16.3\times(3*4)+60\times(5*4)+4.8\times800}{(3*4)+(5*4)+800} = 6.3\text{x}10^{-6}/^{o}\text{C}$$

For equivalent Poisson's ratio:

$$\frac{0.34\times(3*4)+0.3\times(5*4)+0.29\times800}{(3*4)+(5*4)+800} = 0.29$$

V. THERMAL BOUNDARY CONDITION

The temperature boundary condition is shown in Figure 4. It can be seen that the temperatures are −40°C ↔ 85°C, and the dwell-time at hot, dwell-time at cold, ramp-up time, and ramp-down time are 15 min each. Stress free is at room temperature (25°C).

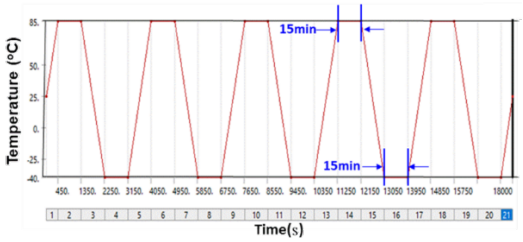

Fig. 4 Temperature boundary condition.

VI. STRUCTURAL DEFORMATION

The deformed shape (color contours) and the undeformed shape (dark lines) of the flip chip PCB assembly with organic core substrate are shown in Figure 5(a) at 450s (85°C) and in Figure 5(b) at 2250s (−40°C). It can be seen that at 85°C, the PCB expands more than the organic package substrate and the silicon chip, and the structure is deformed in a convex shape (smiling face), and at −40°C, the PCB shrinks more than the organic package substrate and the silicon chip, and the structure is deformed into a concave shape (crying face). These results show that the displacement, rotation, and temperature boundary conditions are prescribed correctly.

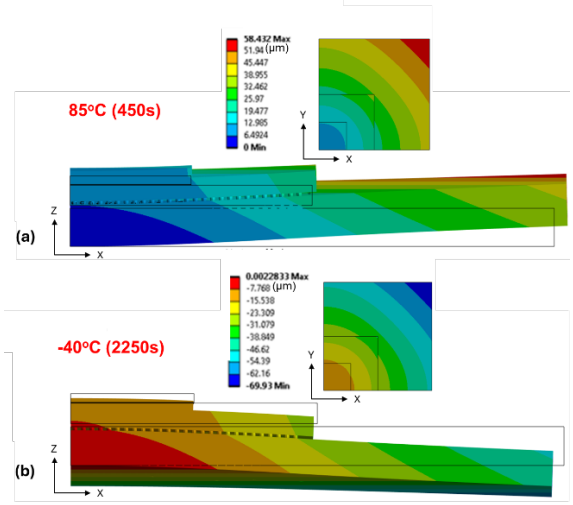

Fig. 5 Deformation of structure with organic core substrate.

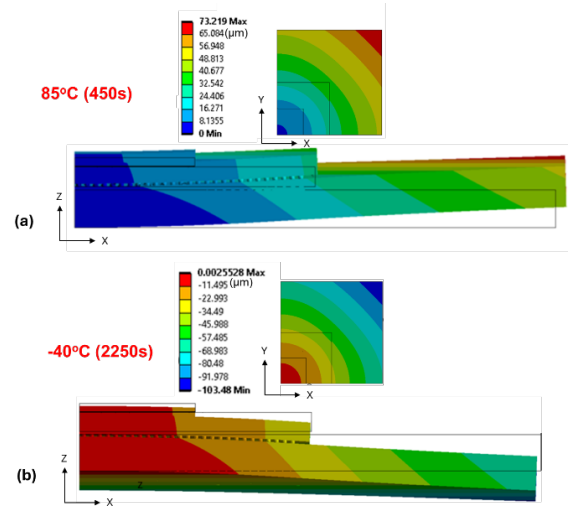

Fig. 6 Deformation of structure with glass core substrate.

The deformed shape and the undeformed shape of the flip chip PCB assembly with glass core substrate are shown in Figure 6(a) at 450s (85°C) and in Figure 6(b) at 2250s (−40°C). It can be seen that, just like those with the organic package substrate, at 85°C, the PCB expands more than the glass package substrate and the silicon chip, and the structure is deformed in a convex shape (smiling face), and at −40°C, the PCB shrinks more than the glass package substrate and the silicon chip, the structure is deformed into a concave shape (crying face). However, because of the difference in thermal expansion coefficient between the organic core

substrate ($\alpha_x = \alpha_y = 11.3x10^{-6}/^oC$, $\alpha_z = 24.8x10^{-6}/^oC$), the glass core substrate ($\alpha = 6.3x10^{-6}/^oC$), and the PCB ($\alpha_x = \alpha_y = 18x10^{-6}/^oC$, $\alpha_z = 70x10^{-6}/^oC$) the magnitudes of deformation are different. The maximum deformations of the assembly with the glass core substrate (73.219µm at 85ºC and -103.48µm at -40ºC) are larger than those with the organic core substrate (58.432µm at 85ºC and -69.93µm at -40ºC). The larger the thermal expansion mismatch between the build-up package substrate and the PCB the larger the deformation.

VII. ACCUMULATED INELASTIC STRAIN

The accumulated equivalent inelastic strain contour distributions at the corner µbump of the flip chip assembly made of the organic core package substrate at 450s (85ºC), at 2250s (−40ºC), and at 18000s (25ºC) are shown in Figure 7. It can be seen that the maximum inelastic strain at the corner µbump solder joint occurs at a small local area and the value is 2.2% at 450s (85ºC), 6.6% at 2250s (−40ºC), and 44.6% at 18000s (25ºC).

The accumulated equivalent inelastic strain contour distributions at the corner µbump of the flip chip assembly made of the glass core package substrate at 450s (85ºC), at 2250s (−40ºC), and at 18000s (25ºC) are shown in Figure 8.

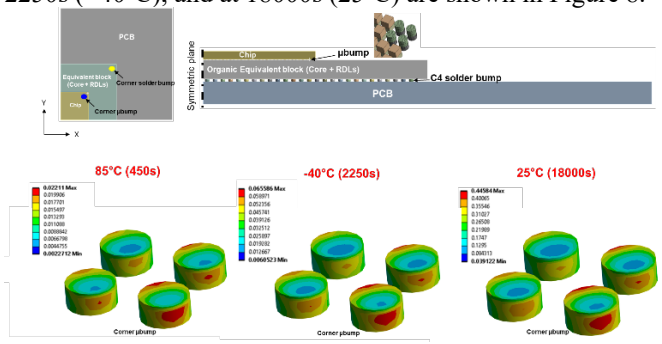

Fig. 7 Maximum accumulated inelastic strain in corner µbump of structure with organic core substrate.

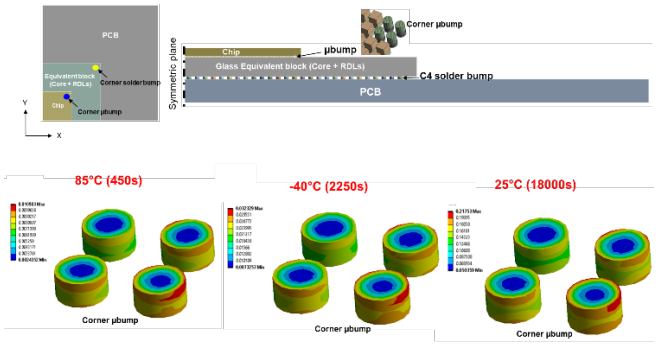

Fig. 8 Maximum accumulated inelastic strain in corner µbump of structure with glass core substrate.

It can be seen that the maximum inelastic strain at the corner µbump solder joint occurs at a small local area and the value is 1.1% at 450s (85ºC), 3.2% at 2250s (−40ºC), and 21.8% at 18000s (25ºC). Comparing these values with those with organic core package substrate, the maximum equivalent inelastic strain at the corner µbump with glass core substrate is smaller than that with organic core substrate. Figure 9 shows the inelastic stain time-history in the corner µbump with the organic and glass substrates. It can be seen that the strain is smaller in the glass structure. This is because of the thermal expansion mismatch between the glass core substrate and the silicon chip is smaller than that between the organic core substrate and the silicon chip.

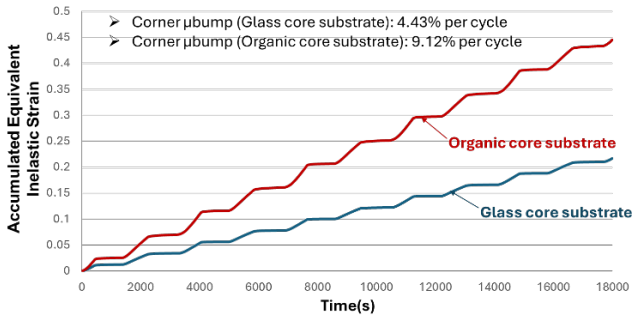

Fig. 9 Maximum accumulated inelastic strain time-history in corner µbump of structures with organic and glass substrates.

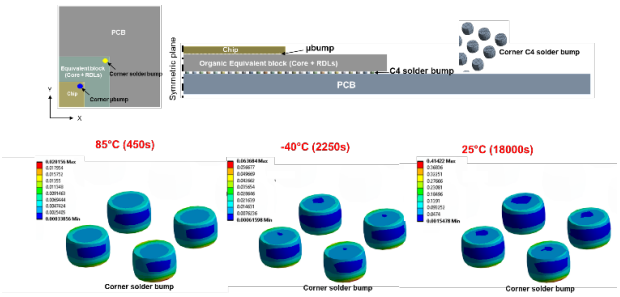

Fig. 10 Maximum accumulated inelastic strain in corner C4 solder joint of structure with organic core substrate.

The accumulated equivalent inelastic strain contour distributions at the corner C4 solder joint of the flip chip assembly made of the organic core package substrate at 450s (85ºC), at 2250s (−40ºC), and at 18000s (25ºC) are shown in Figure 10. It can be seen that the maximum inelastic strain at the corner C4 solder joint occurs at a small local area and the value is 2.0% at 450s (85ºC) and 6.4% at 2250s (−40ºC), and 41.4% at 18000s (25ºC).

The accumulated equivalent inelastic strain contour distributions at the corner C4 solder joint of the flip chip assembly made of the glass core package substrate at 450s (85ºC), at 2250s (−40ºC), and at 18000s (25ºC) are shown in Figure 11. It can be seen that the maximum inelastic strain at the corner C4 solder joint occurs at a small local area and the

value is 4.8% at 450s (85ºC), 15.0% at 2250s (−40ºC), and 94.2% at 18000s (25ºC). Comparing these values with those with organic core package substrate, the maximum equivalent inelastic strain at the corner C4 solder joint with glass core substrate is larger than that with organic core substrate. Figure 12 shows the maximum accumulated inelastic strain time-history in the corner C4 solder joint of structures made of the organic and glass substrates. It can be seen that the maximum accumulated inelastic strain in the corner C4 solder joint is larger with the glass core substrate. This is because of the thermal expansion mismatch between the glass core substrate ($\alpha = 6.3x10^{-6}/ºC$) and the PCB ($\alpha_x = \alpha_y = 18x10^{-6}/ºC$, $\alpha_z = 70x10^{-6}/ºC$) is larger than that between the organic core substrate ($\alpha_x = \alpha_y = 11.3x10^{-6}/ºC$, $\alpha_z = 24.8x10^{-6}/ºC$) and the PCB.

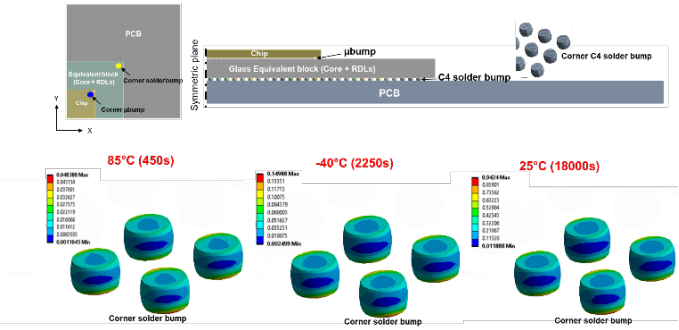

Fig. 11 Maximum accumulated inelastic strain in corner C4 solder joint of structure with glass core substrate.

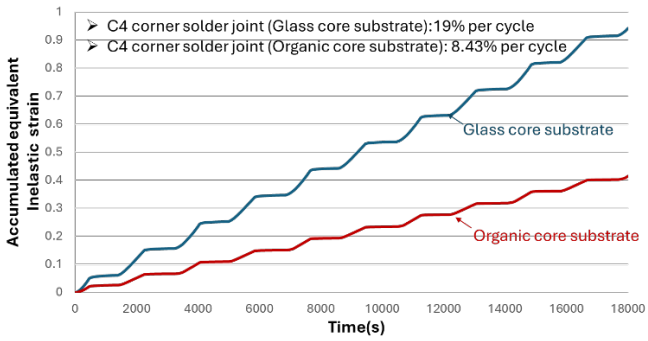

Fig. 12 Maximum accumulated inelastic strain time-history in corner C4 solder joint of structures with organic and glass substrates.

VIII. CONCLUSIONS

Some important results and recommendations are summarized as follows.

- The thermal-fatigue reliability of flip chip micro solder joints on glass core build-up package substrate and C4 solder joints on PCB has been investigated. For comparison purposes, the same structure with the conventional organic core build-up package substrate has also been studied.
- The solder cap of the µbump is made of Sn0.7Cu and the C4 sold joint is made of Sn3Ag0.5Cu. Both solders obeyed the Anand viscoplasticity constitutive equation.
- The deformations of the structures with both the glass substrate and the organic substrate behavior the same: at 85ºC, the PCB expands more than the organic and glass package substrates and the silicon chip, and the structure is deformed in a convex shape (smiling face), and at −40ºC, the PCB shrinks more than the organic and glass package substrate and the silicon chip, and the structure is deformed into a concave shape (crying face). However, the deformation magnitudes of these two structures are very different. The structure with glass substrate exhibits larger deformation than that with organic substrate. This is because of thermal expansion mismatch between the PCB and the glass substrate is larger than that between the PCB and the organic substrate.
- The maximum accumulated equivalent inelastic strain in the µbump solder joint is smaller in the structure with glass core substrate than in the structure with organic core substrate. This is because the thermal expansion mismatch between the chip and the glass core substrate is smaller than that between the chip and the organic core substrate.
- The maximum accumulated equivalent inelastic strain in the C4 solder joint is more than two times larger in the structure with glass core substrate than in the structure with organic core substrate. This is because the thermal expansion mismatch between the glass core substrate and the PCB is larger than that between the organic core substrate and the PCB.
- In packaging under thermal condition, underfill is usually needed for silicon chips on package substrate to ensure the µbump solder joint reliability. However, underfill is seldom used for package substrate on PCB. Thus, in order to have a reliable C4 solder joint, the thermal expansion mismatch between the package substrate and PCB should be as small as possible especially for larger package substrates (because of larger chips). Unfortunately, glass package substrate is heading in the other direction, i.e., the glass CTE is getting closer to the silicon CTE and farther to the PCB CTE. It is recommended when choosing the material properties such as the CTE of a glass substrate, care must be taken for the thermal expansion mismatch between the glass substrate and the PCB, especially for large glass substrates. As a matter of fact, the CTE of the glass substrate should be closer to the PCB CTE because there is underfill protection of the µbump solder joint on the glass substrate but there is no underfill protection of the C4 or BGA solder joints on the PCB especially for larger glass package substrates.

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