Effects of Constraints on Solder Joint Reliability of Electronic Packages

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Abstract

IC package modelling and simulation has been cornerstones in electronic package reliability for more than three decades. Although there is rich literature available on various modelling approaches and experimental data on package failure during thermal cycling tests, the understanding of system level effects such as bolt location on solder joint reliability is limited. For this analysis, thermal cycle tests on 256 pin 17mm × 17mm BGA and 2512 chip resistor were conducted at (1) -40ºC to +125ºC, and (2) +25ºC to +125ºC. Test results were compared with Finite Element Analysis (FEA) results. A total of ten samples of each package type were mounted onto a 1.6 mm thick printed circuit board (PCB) coupon. Four coupons were evaluated per condition with SAC305 solder. To understand the effects of constraints, the test coupons were bolted to an aluminum fixture. Three structural conditions were considered for the test, namely, (1) Free Warp, (2) Semi-Constrained, & (3) Fully Constrained. Moreover, four packages of each type were mirrored to better understand the solder joint reliability due to mirroring packages. All the packages were daisy chained and electrical resistance of the packages were monitored. A tenfold increase in resistance for five consecutive cycles was considered a complete failure. The cycles to failure were analyzed using a 2-parameter Weibull distribution for characteristic life.

Key words: BGA, Solder Joint Reliability, 2512, Finite Element Analysis, Garafalo Model

I. Introduction

Whether it be the reliability needs for the handheld devices to survive more shock drops or the harsher thermal and vibrational loads the automotive electronics as well as avionics must meet, the need for reliability has never been as demanding as it is today. Keeping up with Moore's law, the number of transistors on a single device will be about a trillion by the year 2030 [1]. The importance of electronic reliability is here to stay. One of the major reliability challenges has been that of electronics undergoing elevated temperature field conditions and temperature cycles [2]. Most of the electronic failures during temperature cycle if not all is due to the difference in the coefficient of thermal expansion (CTE) between the printed circuit board (~17ppm) and the package (~6ppm to ~15ppm). Figure 1 shows the effect of temperature on an electronic system. During temperature cycling, the system will expand (above room temperature) and contract (below cold temperature) different amounts, which will in turn load the second level interconnects/solder joints, connecting the package to the board. Repetitive loading of the joints causes solder to fatigue eventually leading up to inelastic strain build up which in turn causes solder failure.

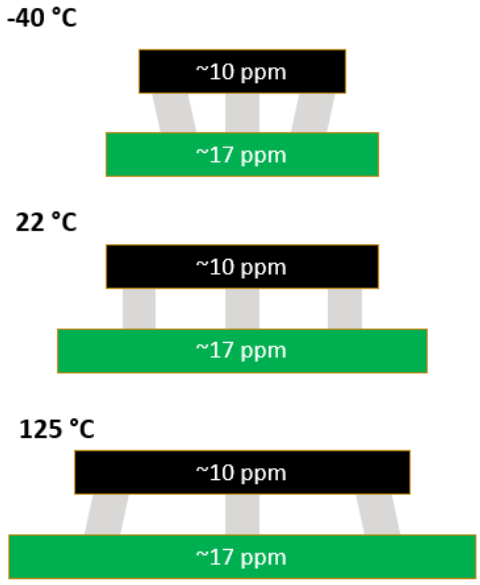

Figure 1. CTE mismatch at hot and cold temperature.

Adding to an already complex system, the influence of enclosure mount hole location, neighboring components, underfill, mirrored components, stackup and other system level effects must be well understood to accurately predict package reliability. Although there is literature talking about effects of underfill [3]-[6] and mirroring [7]-[10] during thermal cycle tests, the number of publications considering the third level packaging reliability or the mounting effects and their interactions with other system effects are limited.

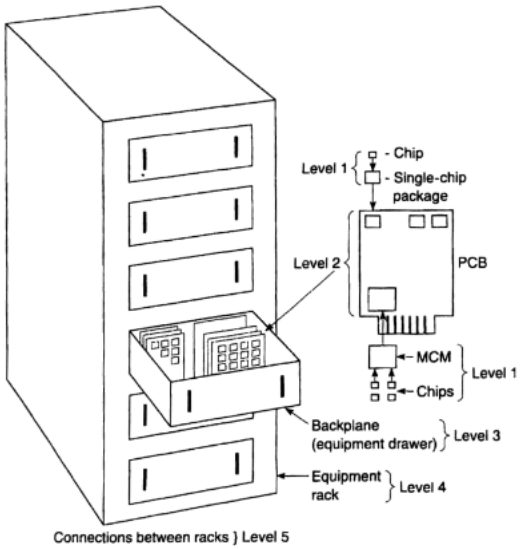

Figure 2. Electronics packaging hierarchy [11]

Standards that define the qualification requirements for thermal cycling test, such as JESD22-A104-B, MIL-STD 883 – Method 1010 and IPC9701 describe the conditions rules for unconstrained board. However, the constraints on the board can have as much as 60% reduction in the reliability of QFN as shown by Vandevelde et.al [12]. Chun-Sean Lau et.al [13] showed that the effect of housing affects QFN and BGA depending on the housing design and package location. QFN reliability was reported by Dudek et. al [14], when the test coupon was mounted onto an aluminum housing for both temperatures cycling as well as thermal shock test. Martin [15] et al, also reported similar effects on reliability of QFN due to housing effects using ANSYS.

In this paper, the effects of constraints on BGA and 2512 chip resistors are investigated. Thermal cycling tests were carried out for two temperature profiles, (1) -40°C to +125°C, & (2) +25°C to +125°C. The results were plotted on a 2-parameter Weibull chart and the characteristic life was compared with results from Finite Element simulation. The predicted life for BGA and chip resistors were found to be within two times of the experimental life. Results with constraints were also compared with that of baseline condition, without constraints (or free warp condition).

II. Experimental Setup

Temperature cycling tests were carried out on four different daisy-chained packages to evaluate the effect of board level constraints on the reliability of SnAgCu solder by considering three structural conditions. For the test, a six layered FR4 PCB test coupon, with immersion gold finish was designed to accommodate ten samples of: (1) 256 pin 17mm × 17mm BGA, (2) 2512 chip resistors, (3) 32 pin 5mm × 5mm QFN and (4) 24 pin TSSOP. In this paper, only the results for BGA and 2512 chip resistors are discussed. Four pairs (eight samples) of each package type were designed to be mirrored for testing the mirroring effects on the solder joint reliability. The remaining two components of each package type were mounted to one side of the board. The test coupon considered was 139.7 mm in length, 118.15 mm in width and 1.575 mm in thickness. The top and bottom sides of the test coupon are shown in Figure 3 and Figure 4, respectively. Components U1 through U10 represents BGA and R1 through R10 represents 2512 resistors. U1, U6, R5 and R6 represents unmirrored components; rest of the packages in the considered sample sets are mirrored.

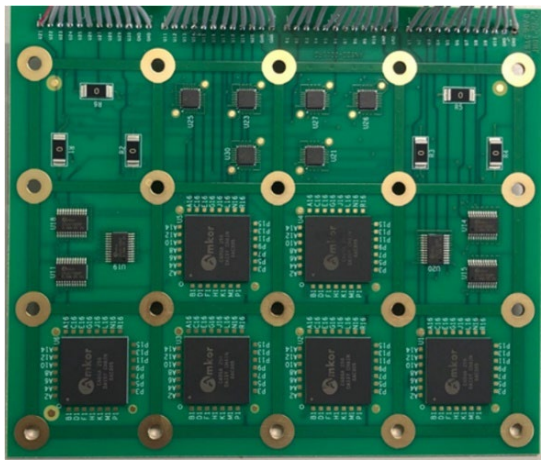

Figure 3. Test coupon, components on the top side of the board.

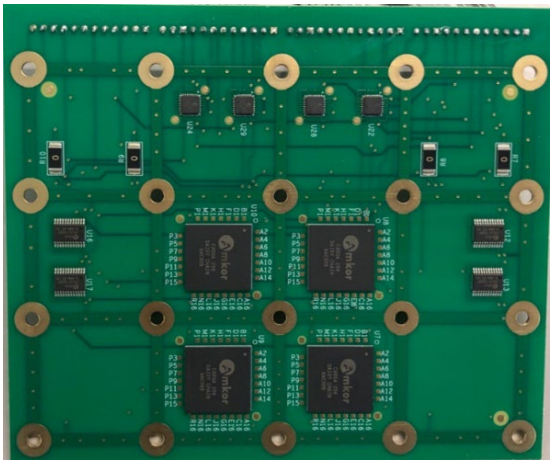

Figure 4. Test coupon, components on the bottom side of the board.

Three structural conditions were considered for the test, namely, (1) Fully constrained, (2) Semi constrained, (3) Free warp. In fully constrained conditions, as shown in Figure 5, the test coupon was bolted to a 7 mm thick aluminum fixture with a 6.5 mm standoff, such that the board warpage is constrained in all the four corners. In semi-constrained condition, the test coupon is bolted to the aluminum fixture only at the four corners as shown in Figure 6.

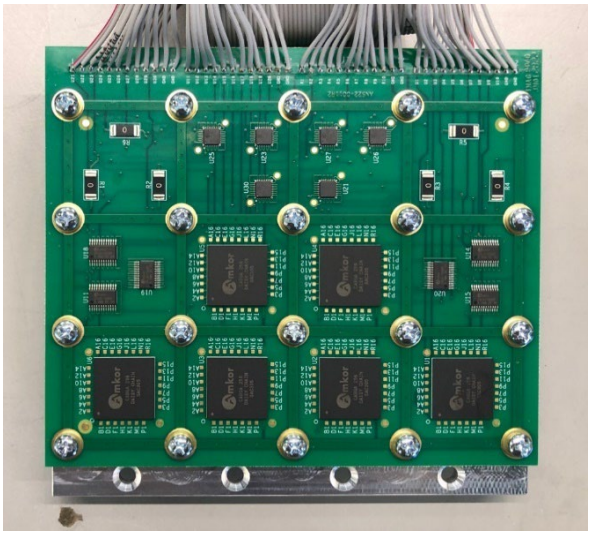

Figure 5. Fully constrained board

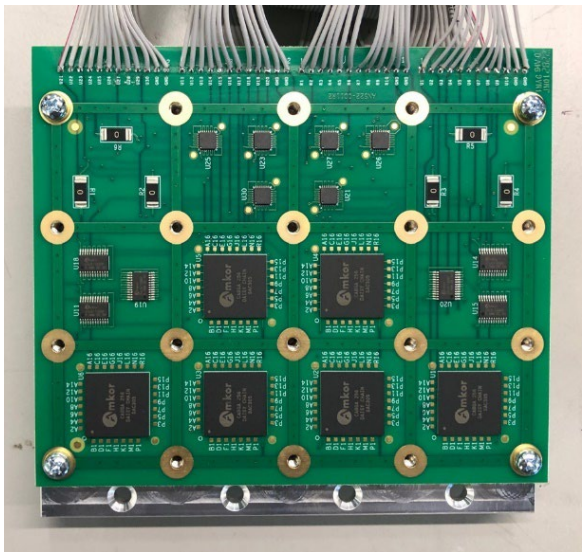

Figure 6. Semi constrained board

Free warp is a condition to mimic the general qualification test condition where the boards are hung without any constraints. Much of the electronic assembly is placed inside a casing for protection from the environment. The board must be mounted to the casing and where these mount holes must be located from a package reliability point of view must always be considered during design. During temperature cycling, the board will expand along with the mounting bolt and the casing material. Whenever there is a difference in expansion between these materials, it will stress the solder adding to the CTE mismatch between the board and the package. Packages away from the mounting locations will have the least impact and those closer will have the highest impact. The three structural conditions considered in this test in a sense represent the worst case, the best case and close to the field condition via fully constrained, free warp and semi-constrained conditions, respectively.

Each test coupon carried forty samples and a total of four coupons per structural condition were thermally cycled between two temperature conditions:

- TC1: -40°C to +125°C, 11°C/min ramp, 20 min dwell
- TC2: +25°C to +125°C, 11°C/min ramp, 20 min dwell

The test matrix is as shown in Table 1. For TC1, the boards were split between two temperature chambers, and for TC2, all the boards were accommodated in one temperature chamber, as shown in Figure 7.

Table 1. Test matrix

	TC1	TC2
Fully Constrained (FC)	4 boards	4 boards
Semi Constrained (SC)	4 boards	4 boards
Free Warp (FW)	4 boards	4 boards

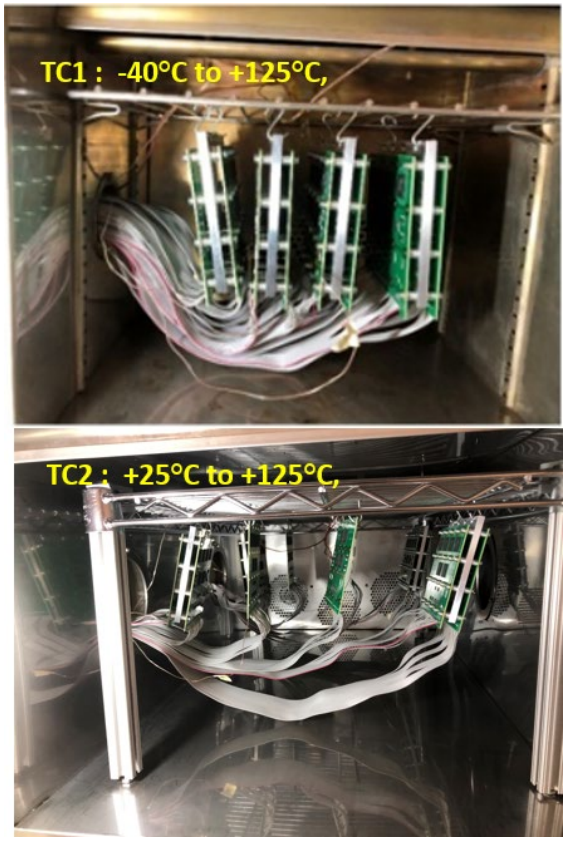

Figure 7. Temperature cycle setup

Chamber air temperature was monitored at the center of the chamber for thermal profiling and thermal cycle count calculation. Besides the chamber temperature, thermocouples were also placed on the board and inside the aluminum fixture to monitor the board temperature and the fixture temperature. Thermal profile tests were carried out to identify any cold spots in the chamber before running the temperature cycling test. Measured test temperature cycles are shown in Figure 8 for thermal condition, TC1. All the chambers were cycled for a total of five thousand temperature cycles.

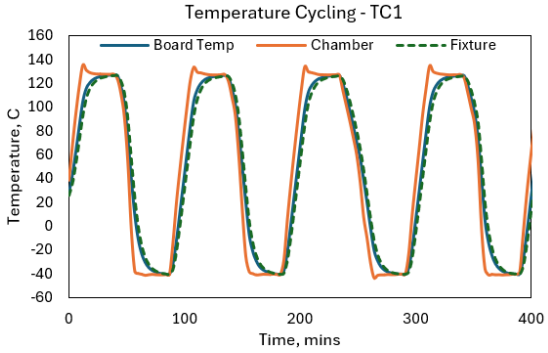

Figure 8. Test temperature cycle

All the BGA and 2512 packages showed failure. A tenfold increase in resistance was noted as a complete failure. The failures were confirmed by electrical characterization. Results were plotted onto a 2-parameter Weibull for characteristic life.

III. Temperature Cycle Test Data, BGA

Each structural condition considered had two sets of failure distribution, one for mirrored and another for unmirrored packages. The package information such as package and die size and solder ball dimensions were confirmed using X-ray and cross-sections. The details are as tabulated in Table 2.

Table 3. Package dimension

BGA	Dimensions in mm
Package Size	17.0 × 17.0 × 1.0
Overmold Thickness	0.41
Substrate Thickness	0.28
Die Size	14.0 × 14.0 × 0.26
Die Attach	0.05
Solder Height	0.3
Solder Diameter	0.54
Solder Package Interface Dia.	0.378
Solder PCB Interface Dia.	0.432
Package Pad Diameter	0.45
PCB Pad Diameter	0.40
Package Pad Thickness	0.0305
PCB Pad Thickness	0.0305
Ball Pitch	1.0

The BGA package considered was A-CABGA256-1.0-17mm-DC-LF-305 by AMKOR with SAC305 interconnects. The cross-section of the package as shown in Figure 9. The failure data were plotted on 2-parameter Weibull using Weibull++. Summary of the characteristic life to failure for the distribution is shown in Table 3.

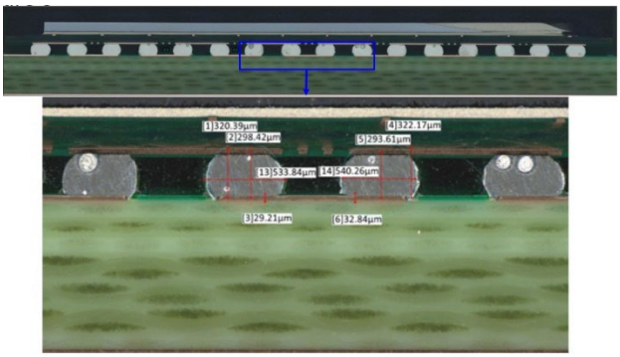

Figure 9. BGA cross-section

Table 2. Failure data, BGA

Structural Condition	Mirrored	Temperature Condition	First Failure	Weibull Beta	Weibull Characteristic Life
Fully Constrained	Yes	TC1	131	5.58	217
Semi Constrained	Yes	TC1	163	5.02	341
Free Warp	Yes	TC1	256	7.99	426
Fully Constrained	No	TC1	621	3.49	1119
Semi Constrained	No	TC1	436	1.96	1224
Free Warp	No	TC1	992	6.42	1382
Fully Constrained	Yes	TC2	193	4.84	339
Semi Constrained	Yes	TC2	313	3.56	736
Free Warp	Yes	TC2	374	5.32	887
Fully Constrained	No	TC2	492	2.57	1449
Semi Constrained	No	TC2	338	1.55	1509
Free Warp	No	TC2	2060	4.73	3343

BGAs on unconstrained board survived 1382 cycles and 3343 cycles for TC1 and TC2, respectively. With constraints, there was only a 20% reduction in life for TC1 and approximately 50% life reduction for TC2. Mirroring can be seen to have a more dominant effect for both the temperature conditions. TC1 and TC2 showed 69% and 73% reduction in life from unconstrained conditions. Mirroring with constraints can be even more damaging. The comparison can be seen in Figure 10.

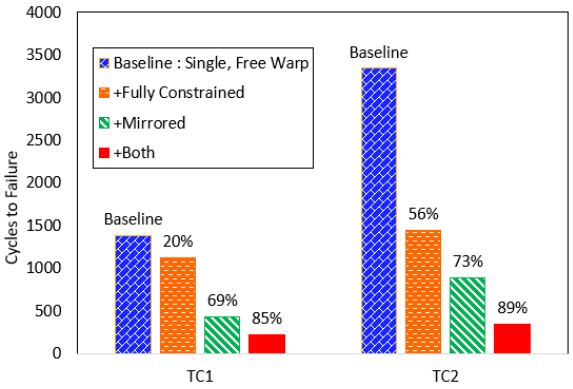

Figure 10. Effect of housing & mirroring

From the Weibull plots, Figure 11 and Figure 12, the effect of constraints is evident for mirrored packages. The margin of differentiation of cycles to failure in TC1 is very thin. This indicates the dominance of mirroring effect over constraints. Under TC2, the life reduced by 50% from free warp to fully constrained condition. The reduction in life due to mirroring is in line with that discussed in literature. Pitarresi [7] showed that the decrease in life is more drastic for stiffer packages. Ye [8] reported the life of a 25×25×1.5 mm BGA with 23×23×0.5 mm die with 1.0 mm ball pitch can show as close as 4x reduction in life. Syed [9] and Lee [10] showed approximately 50% reduction in life between single and double sided BGA packages. Package to die size considered by Ye [8] is similar to that considered in this experiment. Life dropped from 1382 cycles to 426 cycles when mirrored, approximately 3.2x drop in life.

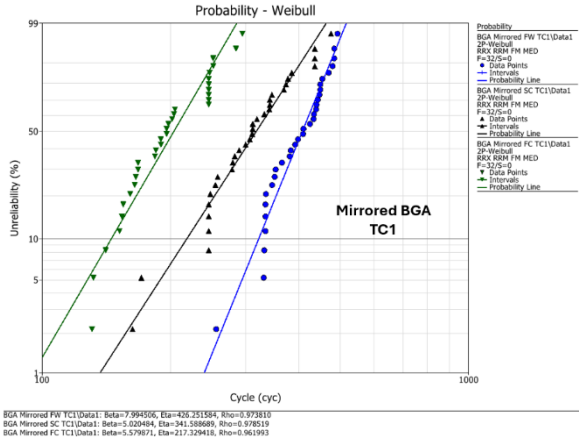

Figure 11. Mirrored BGA, TC1

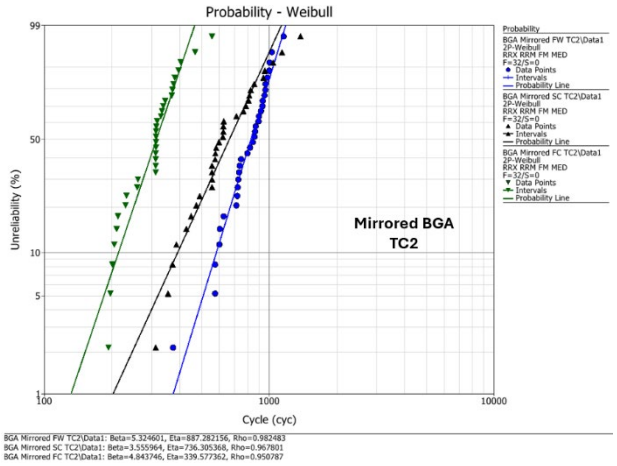

Figure 12. Mirrored, BGA, TC2

All the conditions showed a high Weibull beta except for single sided package on semi constrained board. The spread from the Weibull plot, Figure 13, is quite evident. It could be the position of the boards in the chamber. However, more investigation is needed to narrow down the reason for its spread.

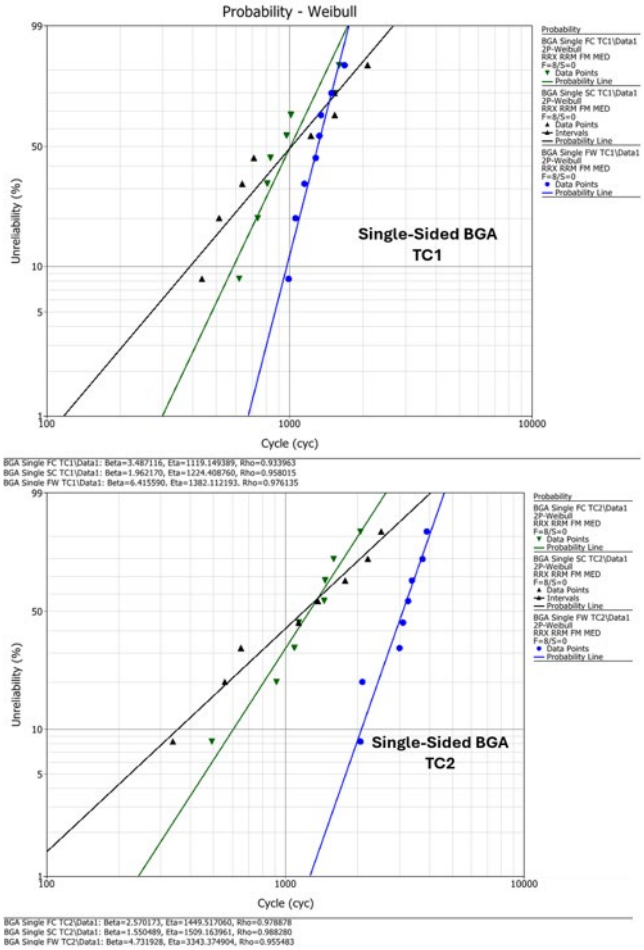

Figure 13. Single-sided BGA, TC1 and TC2

III. Temperature Cycle Test Data, 2512

Boundary conditions considered for 2512 were the same as those considered for BGA. The dimensions of the package are as shown in Table 4.

Table 4. 2512 Chip resistor dimensions

2512 Resistor	Dimensions in mm
Package Length	6.3
Package Width	3.2
Package Thickness	0.55
Pad Distance	4.65
Pad Length	1.6
Pad Width	3.5
Solder Height	0.040
Termination Length	0.6
Termination Thickness	0.0175
Solder Fillet Footprint	0.5

Cross-section for the package is as shown in Figure 15. Failure data from the temperature cycle test are tabulated in Table 5. The overall trend is as expected. The difference between unconstrained and constrained boards are evident for all the conditions. However, there are no differences in life between fully constrained and semi constrained.

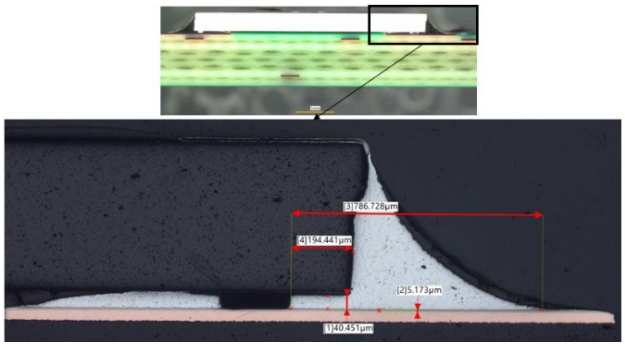

Figure 14. 2512 Cross-section.

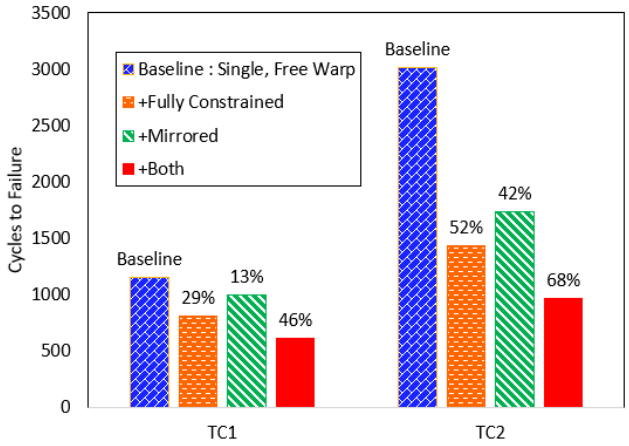

Figure 15. Effects of mirroring and constrains

The effect of mirroring and constraints are about the same for both temperature conditions. For TC1, mirroring decreases life by 13% and constrains decreases life by 29%. For TC2, the changes are 52% and 42%, respectively. As expected, for both the packages considered, BGA and 2512, the higher the temperature change, the lower the life. However, with system level effects included, the change in life between TC1 & TC2 is lower. This clearly indicates that the stresses imparted by mirroring and constraints are significant. The comparison can be seen in Figure 15.

Figure 16 through 18, shows the Weibull plots for the considered configurations for 2512. The beta for all the plots is high and we can clearly see that the unconstrained dataset, inverted triangle, stands out and ahead of the constrained boards.

Table 5. Failure data, 2512

Structural Condition	Mirrored	Temperature Condition	First Failure	Weibull Beta	Weibull Characteristic Life
Fully Constrained	Yes	TC1	266	4.68	612
Semi Constrained	Yes	TC1	168	3.86	606
Free Warp	Yes	TC1	520	5.67	999
Fully Constrained	No	TC1	329	2.82	810
Semi Constrained	No	TC1	336	2.81	815
Free Warp	No	TC1	849	5.48	1148
Fully Constrained	Yes	TC2	427	3.68	963
Semi Constrained	Yes	TC2	126	2.27	1099
Free Warp	Yes	TC2	642	3.14	1736
Fully Constrained	No	TC2	971	4.79	1432
Semi Constrained	No	TC2	699	2.89	1435
Free Warp	No	TC2	1559	3.86	3014

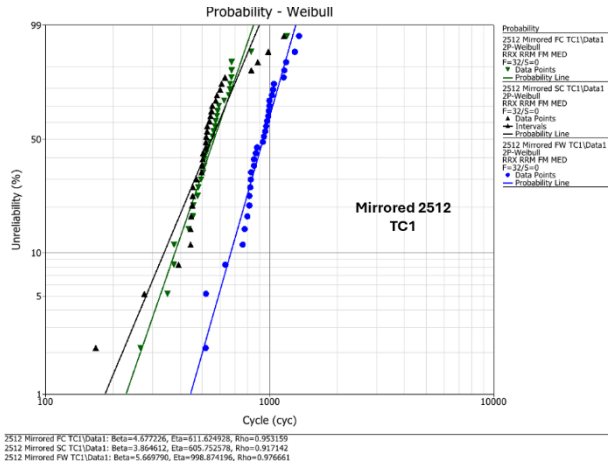

Figure 16. Mirrored, 2512, TC1

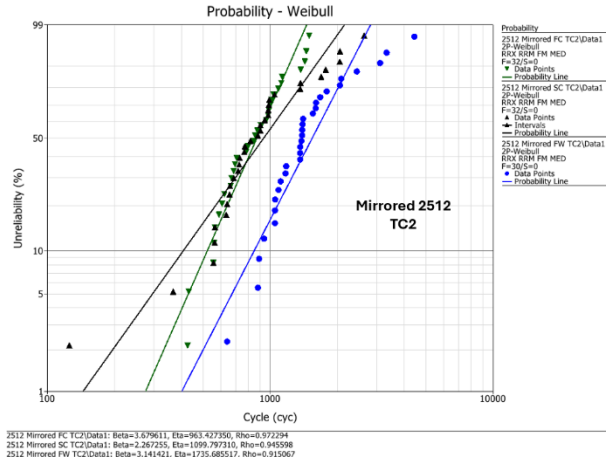

Figure 17. Mirrored, 2512, TC2

The characteristic life from Table 5 shows how close the life is between fully constrained and semi constrained. Although constraints clearly have an influence on component life, it is unclear if the effects of mirroring are overpowering that of constraints. The single-sided 2512 is located exactly at the center of two mounting holes. The difference in life we see for single-sided package is clearly because of the constraints. Expansion of PCB along the length of the package is more critical to the failure of chip resistors as it puts the solder in shear shear. Constraining the axial expansion places the solder under more shear causing the package to fail sooner than the unconstrained packages.

A comparison of the experimental results and the Finite Element (FE) simulation results is presented in Table 6 and Table 7, for BGA and 2512 packages, respectively. Overall, the results were within the general ±2x limit. Solder material was modeled with creep properties using Garofalo model [9]. Life prediction was made using strain energy density model. Die attach for BGA was considered to be stiff and was not modelled. However, it is to be noted that depending on the properties of die attach material, the local CTE mismatch between the interface of solder and the Die/Overmold can impact solder reliability [16]. If the die-attach has a lower modulus, softer die attach, there can be substantial increase to solder fatigue life. However, if the die attach is too soft, the corresponding CTE will be high, which can also negatively impact solder life [17].

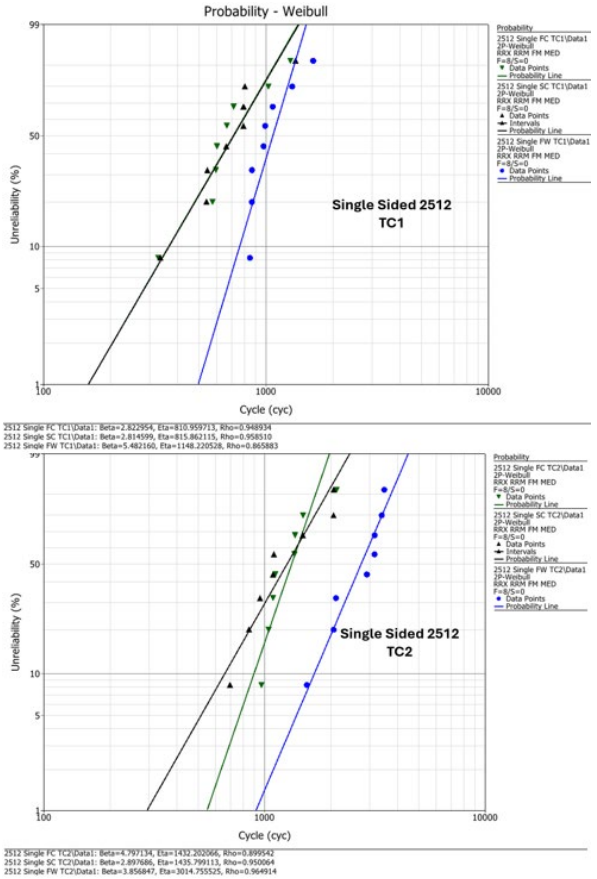

Figure 18. Single-sided 2512, TC1 and TC2

Table 6. Experiment vs FE prediction, BGA.

Structural Condition	Temperature Range	Mirrored	Exp.	FE Prediction
FC	TC1	Yes	217	214
FW	TC1	Yes	426	339
FC	TC1	No	1119	535
FW	TC1	No	1382	1110
FC	TC2	Yes	339	534
FW	TC2	Yes	887	755
FC	TC2	No	1449	1138
FW	TC2	No	3343	2255

Table 7. Experiment vs FE prediction, 2512

Structural Condition	Temperature Range	Mirrored	Exp.	FE Prediction
FC	TC1	Yes	612	481
FW	TC1	Yes	999	812
FC	TC1	No	810	838
FW	TC1	No	1148	1376
FC	TC2	Yes	963	698
FW	TC2	Yes	1736	1672
FC	TC2	No	1432	1684
FW	TC2	No	3014	2841

V. Conclusion

The effect of mounting holes on BGA and 2512 chip resistor on solder reliability was experimentally characterized. Thermal cycling tests were carried out at two temperature ranges namely, (1) TC1, -40°C to +125°C and (2) TC2, +25°C to +125°C. Effect of mounting holes were considered by bolting the test samples on an Aluminum fixture to fully constrain the displacements under Fully Constrained condition. The results from the fully constrained condition were compared with unconstrained board and semi-constrained board where the board was bolted only at the corners. Test data shows that the effect of mirroring is more detrimental compared to constraints with considered BGA samples and was on par with 2512. The effort shows the importance of system level effects in solder reliability. Life from the experiment was also compared with prediction from simulation and were found to be within the ±2x limit.

Acknowledgment

The authors would like to acknowledge the colleagues of Ansys Reliability Engineering Services (RES) team for their support and contributions. Special thanks to Michael Blattau who led the board design effort. We would also like to thank Gil Sharon for his insightful comments on the work and interpretation of the results.

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