The Quarter Factor Prediction of Mold Void Mechanism between Structure Ratio and Molding Gate

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Abstract

The fluid kinematics of epoxy molding compound effect on the flow behavior of transfer molding, melting wave uniformity and the mold void risk in the molding gate and structure ratio were analyzed and the molding resistance was investigated by the simulation and experiment as well in this article. The numerical method in this study was capable of considering the effects location on the melting trap of the void, and also compared with the molding resistance. Due to the variation of molding gate in device design period, the substrate type of molding process validation involves flow ability and molding structure resistance, which caused incomplete filling and popcorn failure. Thus, the prediction of melting wave and mold void distributions is a prerequisite for the reliability analysis of IC packages.

However, it was demonstrated that the molding gate cross-sectional area ratio between gate and first-row package array affected the melting wave contribution, and deviated void across the chip. In addition, the die thickness and components aspect ratio influenced the potential mold void distribution on edge and packages of the entire strip. The result also showed better melting wave contact between fluid welding effects when the aspect ratio about 10%.

Key words

Mold void, incomplete filling, Molding resistance, Molding gate, Mold void prediction

I. Introduction

By integrating IC packaging to meet the increasing demands for high bandwidth memory (HBM) and high-performance computing (HPC), high-density interconnections now exclude bump ratios, chips, and fine-pitch interposers. The back-end molding process is a critical factor in preventing and protecting against external noise and ensuring insulation for the package. Recent literature has demonstrated various encapsulation thickness techniques that alter flow resistance based on mold tool design. L. Yang et al. [1] described mold void results related to different mold heights and minimum mold gap ratios due to flow resistance differences. Additionally, J.-Y. Lai et al. [2] and Y. Zhu et al. [3] noted that dual-side module molding can encounter incomplete filling when the compound of the mold volume exceeds 23%. Wafer-level molding, with varying component ratios, resistance, and Epoxy Molding Compound (EMC), has also been shown to exhibit warpage after molding. ([4]–[5])

Investigating various cross-sectional mold thicknesses and melting resistances, T. Shibata et al. [6] proposed that the critical gap for 2.5D molded interposers be extended to evaluate solder height and warpage. J. L. et al. [7] studied different quantities of silicon dies in each device and compared simulation results with experimental data, allowing for the estimation of mechanical deformation in packaged strips after molding.

In process evaluation, the mold tool design, particularly the gate configuration, is not only a factor in mold void risk but also affects mold flow resistance throughout the molding process. F. Yen et al. [8] and F. Qin et al. [9] examined FCCSP and WLCSP with varying die sizes, bump heights, and pitches. They noted that larger die ratios can result in more pronounced melt wave differences between the center and edge of the package due to molding, especially with longer epoxy molding compound curing times.

In summary, this study assumes that the molding gate and molding resistance are key factors in mold void formation after the molding process. The evaluation considered full strip samples, including mold tool design, package array, and different chip or mold thicknesses. Additionally, the finite element method (FEM) incorporating EMC material properties and resistance ratios was used to directly assess the actual mold void risk.

II. Governing equations

A. Viscosity Model

The epoxy resins must be processed at molding temperature with conversion rate and viscosity changes, the viscosity model which we proposed the Castro-Macosko model [10] to describe the rheological data of resin properties:

$$\eta\left(\alpha, T, \dot{\gamma}\right) = \left(\frac{\eta_0}{1+\left(\frac{\eta_0 \dot{\gamma}}{\tau^*}\right)^{1-n}}\right)\left(\frac{\alpha_g}{\alpha_g - \alpha}\right)^{C_1 + C_2 \alpha} \quad (1)$$

$$\eta_0 = A exp\left(\frac{T_b}{T}\right) \quad (2)$$

$$T_b = \frac{E_a}{R} \quad (3)$$

Where η is the viscosity, α is the reaction conversion, T is the temperature, $\dot{\gamma}$ is the shear rate, τ^* is the model constant and also indicates the shear stress rate, $1-n$ is the pseudoplastic melt slope behavior, $\alpha_g$is the gel point of the degree conversion, and A, E_a, C_1, C_2 are model parameters.

B. Curing Reaction

In our study, the thermoset epoxy molding compound curing status are considered, and the kinetic governing equation with described chemical conversion we used was studied by Kamal and Ryan [11].

$$\frac{d\alpha}{dt} = (k_1 + k_2 \alpha^m)(1-\alpha)^2 \quad (4)$$

$$k_1 = A_1 exp\left(-\frac{E_1}{RT}\right) \quad (5)$$

$$k_2 = A_2 exp\left(-\frac{E_2}{RT}\right) \quad (6)$$

Where k_1 and k_2 are the rate constants of Arrhenius equations, m is empirical constants, E_1 and E_2 are the apparent conversion activation energies, R is the universal gas constant.

C. Cross-Sectional Resistance

The molding process of package flow ability were follow package front view of components resistance. M. Rovitty et al. [12] studied flow resistance between die top and bottom, and we consider 0.35mm and 0.45mm two difference mold thickness of mold void risk evaluation.

A major challenge faced in this approach is to control the A_e cross section area to leverage each components in package, as such as chip, bump or underfill (UF) etc., Fig.1 and Fig.2 indicate the difference sense of sight at A_e

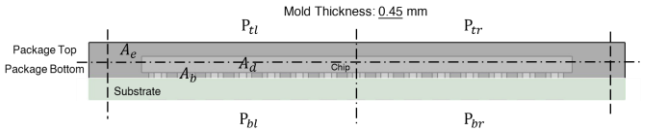


Fig. 1. 0.45 mm mold thickness cross section area.

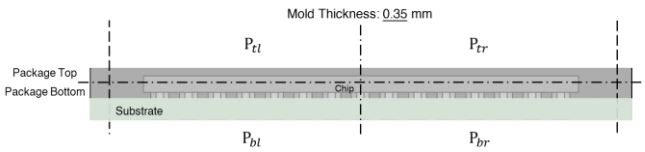


Fig. 2. 0.35 mm mold thickness cross section area.

Where A_e is the epoxy molding compound cross-section area, A_d is die of cross-section area, A_b is bump cross-sectional area, indicate the bump under chip. The P_{tl}, P_{tr}, P_{bl}, P_{br} are the package point-centered quarter factor, L_f is top/bottom leverage factor. , the quarter factor can be describe:

$$P_{tl} = A_e - A_d$$

$$P_{tr} = A_e - A_d$$

$$P_{bl} = A_e - A_d - A_b$$

$$P_{br} = A_e - A_d - A_b \quad (7)$$

Mold flow resistance can be spread multiple wave start from gate, alternatively we assumed the half cross section area of leverage a package for quarter factor is

$$L_f = \frac{P_{tl} + P_{tr}}{P_{bl} + P_{br}} \quad (8)$$

When L_f approaches to 0, indicate leverage factor of the

mold flow balance and mold void welding will worse than 1, the melting performance since worse to better can be describe by

$$0 > L_f > 1 \tag{9}$$

III. Molding experiment and simulation setting

The schematic of simulation model and size was shown in Fig.3, we assumed one pot model for boundary condition, the bump ratio remove some of position as molding gate of transfer speed and welding consideration.

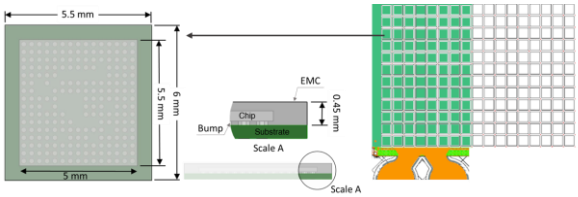


Fig. 3. Strip model and unit package boundry condition.

Moreover, in this preferred that L_f formula to select mold thickness between 0.45 mm and 0.35 mm after cross-sectional resistance calculated, mold thickness 0.45 mm is 0.6 and mold thickness 0.35 mm is 0.8, L_f 0.8 approaches to 1 indicated 0.35 mm shows less mold void in Fig. 4 compared with 0.45 mm was significantly.

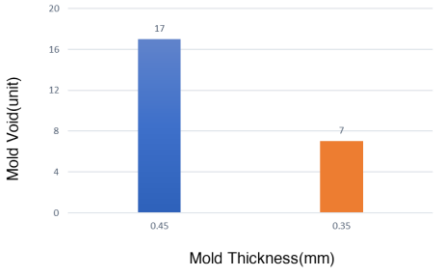


Fig. 4. Strip model and unit package boundry condition.

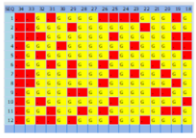
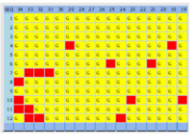
This molding resistance in process condition were suitable for evaluate different structures and before the FEM analysis, this phenomenon main factor include transfer speed, molding recipe for transfer molding process used in this study with common experience setting is listed in Table I.

TABLE I. MOLDING RECIPE SETTING

Molding Temperature	160℃~170℃
Transfer Pressure	9~13 MPa
Transfer Speed	4X, 2X, 1X mm/s
Pellet Diameter	10~14 mm
Pellet height	40~46mm

In this study, two structural models, Model 1 and Model 2, are defined by the die ratios shown in Table II. Yellow indicates the substrate with die attached, while red represents areas without die attached. Additionally, the die bond (DB) process yield for the full strip considers the electrical properties of the substrate and previous process yield losses. The structure 1 DB ratio is 75% and structure 2 is 90%, total EMC volume were employed in this simulation.

TABLE II. SIMULATION/EXPERIMENT MODEL AND RECIPE SETTING

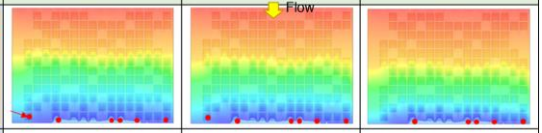
DoE		Structure 1	Structure 2
	Flow ⇩ Die Bond Mapping		
	Die Bond(%)	75%	90%
	Mold Thickness(mm)	0.35	0.35
	Real-External Void(%)	2.6%	0.0%
Gate Velocity Optimization (mm/s)	Cell 1	4X	4X
	Cell 2	2X	2X
	Cell 3	1X	1X

With die Without die

Result Verification

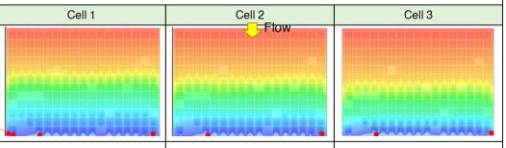
Based on die ratio condition, the potential mold void were trapped at strip vent side area was obviously, the red color is pellet of gate which is filling start position, and blue color of melt front, Table III indicated the end of filling of transfer time in molding process, overall consideration from red to blue are the time scale of mold flow, the transfer speed level in this study was depends on molding machine maximum velocity(mm/s), 1X speed is the common experience in general machine type,

TABLE III. 75% DIE RATIO WITH SPEED COMPARISON.

DoE	Structure 1 Cell 1	Cell 2	Cell 3
Melt Front / Mold Void(sim.)			
Die Bond(%)	75%	75%	75%
Simulation-Mold Void(%)	4.0%	4.0%	3.3%
Real-Mold Void(%)	2.6%	2.6%	2.6%
Transfer Speed	4X	2X	1X

After simulation, the 75% DB ratio results present cell 1 to 3 are the same die ratio of considerations, only transfer speed was designed to investigate the influence of melting, the cell 3 with lower transfer speed were performed to ensure less mold void occurred at strip vent side area, furthermore, cell 2 and 3 are the worst of side rail for mold void remain was shown in Table III.

TABLE IV. 90% DIE RATIO WITH SPEED COMPARISON.

DoE	Structure 2 Cell 1	Cell 2	Cell 3
Melt Front / Mold Void(sim.)			
Die Bond(%)	90%	90%	90%
Simulation-Mold Void(%)	1.6%	1.1%	1.1%
Real-Mold Void(%)	0.0%	0.0%	0.0%
Transfer Speed	4X	2X	1X

In addition, the Table IV results 90% DB ratio have lass EMC volume compare with 75% DB ratio on substrate, the main challenges are the flow performance and structure difference, the result presented that the molding resistance matched the experimental and simulation results well for the mold void risk assessment.

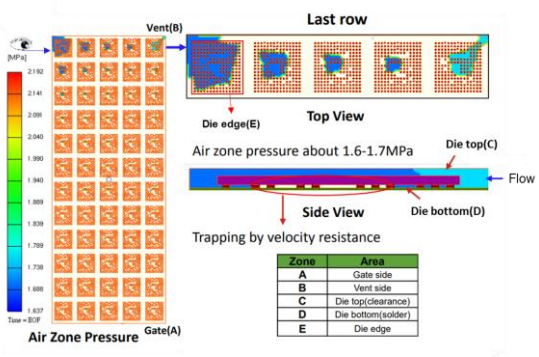


Fig. 5. Air zone pressure trapped remain in strip(MPa)

After potential mold void prediction, the air zone pressure will remain in the package center, also occurred at vent side package in general, the size of air zone pressure was over 20 mil size of a sphere, it was turns out air pressure to visualize the size that needs to be observed, the empty area without EMC filling was shown in Fig. 5 red circle of trapped by velocity resistance side view, this phenomenon started at the first row filling of package and end of vent side package during air trapped, the die top have been demonstrated fast filling performance than die bottom.

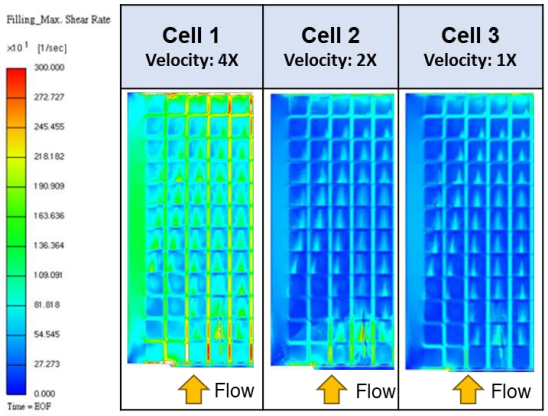


Fig. 6. 0.35 mm mold thickness with speed level comparison.

Apart from the transfer speed of shear rate was shown in Fig. 6, cell 1 showed high shear rate in molding process time scale, and as highlighted in Fig. 6, the simulated shear rate on the speed level of the resistance along the Fig. 5 die top (C) and die bottom (D).

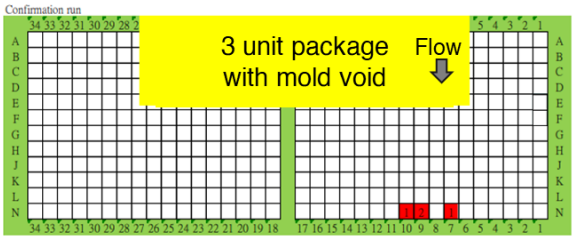


Fig. 7. 0.35 mm mold thickness with speed level comparison, in cell 3 1x transfer speed of molding.

For the measurement after molding process, the strip mold void still occurred in vent side position 7, 9 and 10 shown in Fig. 7, and the results were matched with simulation obviously.

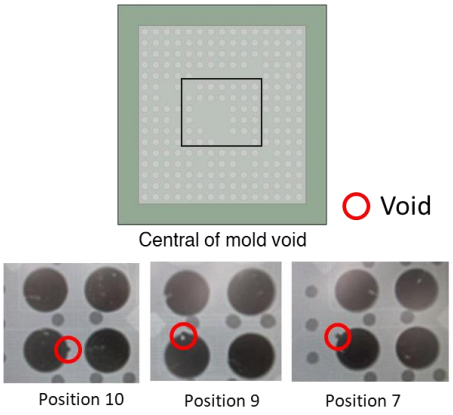


Fig. 8. Mold void occurred in the central of package after reflow by X-ray measurement.

Compare to the 0.35 mm mold thickness 1X transfer speed of X-ray image measurement, the three position 7, 9 and 10 in Fig. 8 shows an exemplary image of mold void distribution in the central of package, highlighting the mold void extrusion area at the bump pitch. The extrusion was subjected to flow pressure and resistance matching L_f and simulation results. The finding agreed with the simulation prediction, which showed the voids found in the solder bump area higher than the package top of the die and bump interface (Fig. 5). After applying the shear rate consideration, the package showed further void contribution, also demonstrating the void quantity of the unit package in the venting location Fig. 5 die top (C) and Fig. 8(7, 9, 10).

Some of the key merits of the design stage of mold thickness and process optimization of molding recipe both are compared to conventional technologies are listed in the following:

1) *Mold thickness:* melt resistance between die top and bottom demonstrated different mold flow capability, 0.45 mm mold thickness affects cross sectional resistance by different dragging force, this mold void performance after simulated 5 unit package left, but 0.35 mm shows only 2 unit package mold void risk, the mold thickness was successfully tested up to the 0.45 mm, which was the minimum of mold void remain of our results showed in Fig. 4, the aspect ratio 0.45 mm and 0.35 mm with P_{tl} are ~5% and ~10% indicate die thickness of molding resistance, 10% has better performance calculated by L_f prediction.

2) *Molding recipe:* transfer molding in this paper work proposed three level speed(molding gate) based on molding machine of plunger velocity, higher speed affects side rail was obviously, 4x speed simulated voids have 6 unit of package remain, and speed 1x have only 5 unit of package left.

3) *Mold void risk assessment:* the formula L_f unbalanced flow capability can be suitable use in the strip to validate internal mold due to the new product invention.

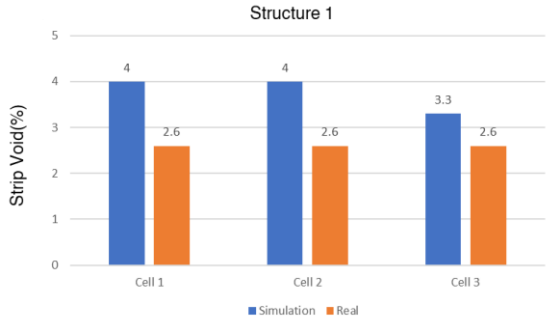


Fig. 9. 75% DB ratio of overall strip void contribution trend organize by test vehicle(real) and simulation.

For the overall mold void in strip ratio for DB 75% was performed in Fig.9 to investigate the trend of test vehicle and simulation, the speed limit is part of the transfer profile and is defined per amount of transferred EMC.

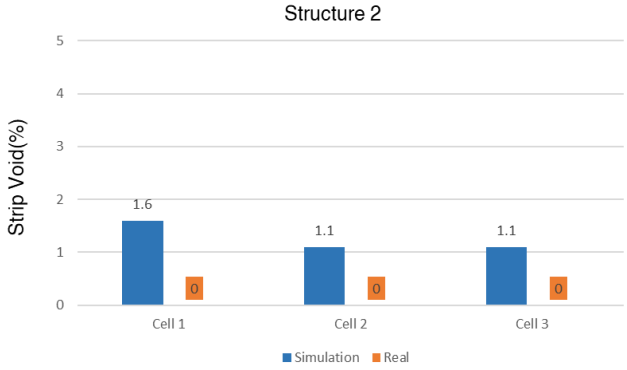


Fig. 10. 90% DB ratio of overall strip void contribution trend organize by test vehicle(real) and simulation.

Moreover, 0.35 mm mold thickness in strip void mapping by test vehicle measurement are shown in Fig. 10 was similar trend with simulation result.

Conclusion

This work presents the prediction, design, and verification of transfer molding mold voids. We particularly focused on optimizing structure and recipe to minimize voids. By refining mold thickness and optimizing the recipe, we significantly reduced the final cost associated with trial and error and improved the design phase cycle. Test vehicle results show that the L_f approaches 1, and a lower speed of 1X achieves excellent reduction in mold voids. This flow performance, demonstrated with FC devices, meets the reliability standards required for solder extrusion applications with stringent mold void criteria.

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