Molded SiP manufacturing with integrated shielding layer for optimized EMI robustness

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Abstract

The functional reliability of microelectronics packages in harsh environment use not only depends on interconnect integrity and thermomechanical robustness, also signal integrity can play an important role for package performance. For industrial/automotive use, the shielding of packages against electromagnetic interference is a key process tep that defines package performance in challenging environments. Within the project AdaPEdge, Fraunhofer IZM, TUB and MST are cooperating to manufacture highly integrated packages using Flip Chip technology and MAP molding technologies for package realization. To ensure optimized shielding of the packages, a test vehicle has been designed that allows the determination of shielding efficiency of molded packages without and with shielding layers created in different technological approaches. These technologies can be applied to single packages and to full MAP areas and include direct metallization on molding compounds, contactless dosing of a conductive layer and laser direct structuring.
As a result, the paper presents the manufacturing of Shielding Efficiency test samples in various technologies, the SE measurements over a wide frequency range for samples with varied shielding layer thickness. The measurements are validated using an analytical model developed in-house and there is good agreement between the measurement and the analytical model. Based on the analytical model, physical effects at the interface of material and in the material are separated and analyzed.
Comprised, packaging boundary conditions and design rules for define EMC-robust packages will be provided that allow an efficient manufacturing of functional SiP packages.

Key words

System in Package, Package Shielding, EMC define, Shielding Efficiency Measurement

I. Introduction

Microelectronics packaging is targeting maximum miniaturization at reasonable cost to make mobile devices even more functional and portable or to integrate ever more computing power into one computing blade to address high performance computing (HPC) in data centers around the world. Methods of advanced packaging, often working on wafer scale do serve this purpose well - e.g. hybrid bonding & 3D integration technologies are used to build such systems. For more specific applications such as industrial electronics, medical or automotive manufacturing, volume is typically smaller and the most advanced packaging technologies are typically out of reach, often for economic reasons as setup cost can hardly be covered by small volume manufacturing. For such cases System-in-Package (SiP) can be a solution combining high performance, high integration density and application adapted reliability combined with acceptable cost.

A SiP can be defined as a package or module that contains a functional electronic system or subsystem that is integrated and miniaturized through IC assembly technologies. Rather than generic IC packaging technologies, development of SiP requires heterogeneous integration of single or multiple chips (such as a specialized processor, DRAM, flash memory), surface mount device (SMD) resistor/capacitor/inductor, filters, connectors, MEMS device, sensors, other active/passive components and pre-assembled package or subsystem [1].

Such SiPs are highly integrated electronic modules for application in a rough environment, be it industrial, automotive or medical. And for all these environments specific standards apply, for automotive applications the well-known standard AEC Q104 “Failure Mechanism Based Stress Test Qualification For Multichip Modules (MCM) In

Automotive Applications" is aiming at the SiP relevant topics, including thermal, thermomechanical and mechanical testing but also refers to electrical testing with a focus on shielding efficiency. [2] In the realm of electromagnetic radiation emittance and resistance the CISPR is defining both measurement procedures and limits. The CISPR16 e.g., defines limits for the magnetic field emissions from 150 kHz to 30 MHz and for electric field components from 30 MHz to 18 GHz. [3] Furthermore, the SiPs need to be robust in an environment where neighboring devices might also radiate and thus cause EMI (Electro Magnetic Interference) - so all basic demands for EMC (Electro Magnetic Compatibility) known from communications/computing applications apply. Within this study the realization of a shielding layer is researched, that can be integrated into a SiP packaging process flow based on MAP molding, that allows not only shielding of the System in Package, ideally with the option of realizing a molded underfill using MUF encapsulants, but simultaneously can be used to integrate an Antenna-in-Package [AiP], serving as an RF interface for communication.

To apply a shielding layer to a package, there is a variety of process options from additive manufacturing processes, as this one [4] just recently presented by Heraeus, via laser direct imaging for encapsulant activation as described in [5] to electroplating as described in [6]. All options do have their individual pros and cons, where for this study a focus was put on availability for medium volume production and a multiple source availability of the respective processes, so PVD (Physical Vapor Deposition) in combination with electroplating was selected for first investigations.

Process development for this study involved overmolding of test PCB carrying antenna structures using various molding compounds and determine moldability, singulate these MAP and develop a process to apply 5-sided shielding with contact to a package ground layer to ensure EMC for e-fields and to determine shielding efficiency for H-fields to select optimum shielding layer thickness. A sketch of the test vehicle can be seen in Figure 1.

Figure 1: Sketch of a test package with 5-sided Cu-Shielding and a backside RF interconnect for testing

II. Theoretical Background Shielding

Harsh environments, especially with a focus on electromagnetic compatibility, can push electrical circuits to their limits or lead to malfunctions. A classic distinction must be made between interference from electric, magnetic and electromagnetic fields.

a. *General Overview*

At low frequencies (typically less than 10 MHz), electro-magnetic fields are not yet capable of propagation and electric and magnetic fields dominate the sources of interference in electrical systems. [7]

Effects at low frequencies (E- and H-field shielding)

For E-field shielding, a housing with a high conductivity (e.g. copper) is usually sufficient, which is connected to ground potential so that no more fields can penetrate the interior. The shielding thickness does not matter. The reason for this is Gauss's law, whereby the shield closes the circuit in the transmitting sense. Such effects are known from a Faraday cage. For this reason, the focus of our analysis is exclusively on magnetic field shielding. Unfortunately, it is not so easy with magnetic fields because magnetic charges are not existential. For this reason, the magnetic field lines can always penetrate through material in the DC case. When the frequency is increased, displacement currents occur in conductive or magnetic materials. According to Lenz's rule, these have the positive property that they escape their cause. This means that magnetic fields can be attenuated or, if the shield for the sensor is closed, the area can be free of magnetic fields. The skin penetration depth can be used as a rule of thumb, because if the material has the same thickness as the skin penetration depth, the field inside has decreased by 1/e.

$$\delta = \sqrt{\frac{\rho}{\pi \cdot f \cdot \mu_0 \cdot \mu_r}} \qquad (1)$$

Electromagnetic shielding

For the sake of completeness, a brief summary of electromagnetic shielding. It is based on both parts (E- and H-fields) which couple into each other via the wave equation. The higher the frequency, the stronger the coupling. For this reason, it can be said that if you have a good shield which completely excludes the H-fields and only has a small electrical opening, these shielding effects can be neglected. In the case of non-idealities, as is classically found in realistic setups, they naturally have an influence and must also be analyzed. Within the publication there is of course an influence and it will be considered in the detailed discussion.

b. *Analytical Modeling magnetic shielding*

The magnetic shielding of a plane metal sheet of infinite extent in quasi near-field environments such as this can be approximated. The formula of Moser [8] can be simplified if several assumptions are valid. One is that the antenna is electrically small, resulting in a constant current distribution. Another is that the distance of the probe from the radiating element is much smaller than a free space wavelength. In the frequency range relevant to this research, two models are used. They differ in the skin penetration depth that qualifies

the shielding as electrically thin. Both were developed by Bannister [9][10].

These theoretical considerations led to the design of the two test vehicles. The longer magnetic dipole's length of 20.8 mm falls below one eighth of the highest radiated frequency of 2.4 GHz.

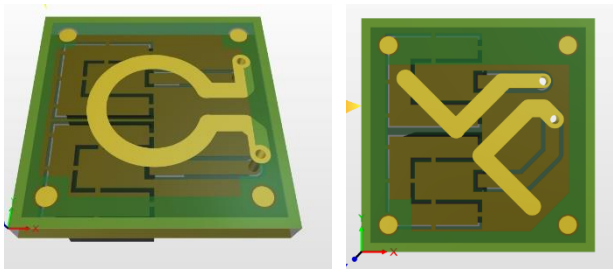

Figure 2: Antenna structures for shielding efficiency measurements on carrier substrate; left: magnetic dipole, right: electrical dipole

III. Experimental

Test Module Manufacturing

The reference package addressed in this study is a PCB-based QFN with SMD/FC components that is overmolded to protect the components and to increase package reliability. Reference package sizes are in the range from 6x6 to 12x12 mm², with a full MAP strip measuring 205x70 mm² and containing 3 MAP areas with a usable size of 53x53 mm². The test package footprint was set to 10x10 mm² and a 4x4 package matrix per MAP area was used. The design is depicted in Figure 3.

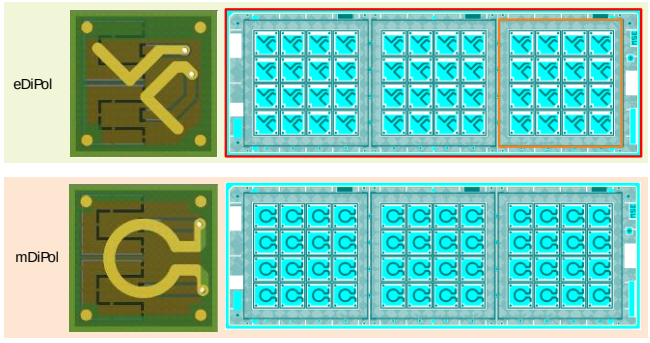

Figure 3: PCB Strip design for both design variants, both containing 4x4 packages per MAP area with 10x10 mm² footprint each.

Within the project, this strip can be used for both encapsulation process variants, transfer molding and compression molding, while compression molding is the preferred process for the investigations described here.

The process flow for sample manufacturing targeting a compression molding process started with incoming inspection of the substrates and singulation into individual MAP areas, drying, compression molding and subsequent postmold cure, package singulation, shielding layer application by 5-side metallization and finally a RF-plug assembly on package backside followed by outgoing inspection and a handover to the SE analysis. This flow is depicted in Figure 4.

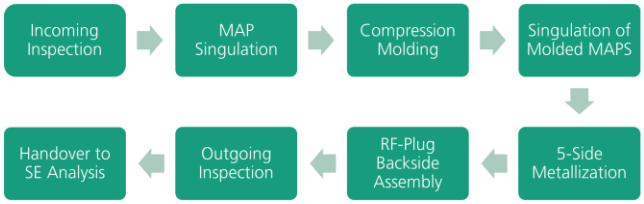

Figure 4: Process Flow Overview for Compression Molded Samples

For overmolding the samples a selection of compression molding compounds has been used, combining granular and liquid compounds with different filler sizes and content and thermo-mechanical properties. Three standard molding compounds showed filler sizes > 25 µm, two compounds for MUF had a maximum filler size of 5 µm and one granular compound with larger fillers and a thermal conductivity of ~ 5 W/mK were selected for evaluation. Material properties are depicted in Table 1. For these molding compounds moldability, molding homogeneity and the suitability for direct metallization have been used as ranking criteria.

Table 1: Molding Compounds used for MAP molding and metallization evaluation

EMC	EMC A	EMC B	EMC C	EMC D	EMC E	EMC F
Type	Liquid	Liquid	Liquid	Liquid / MUF	Liquid / MUF	Granular/ Hi-TC
Filler Content [wt%]	89	88	85	78	84	87
Max. Filler Size [µm]	> 40	55	25	5	5	25
E-Modulus [GPa]	22	22	19	13	14	27,4
CTE α1/α2 [ppm/K]	7,5 / 33	8 / 34	10 / 41	12 / 77	13 / 31	15 / 54
Tg [°C]	165	165	150	190	154	170
Cure	10 min @ 125 °C 60 min @ 150 °C	10 min @ 125 °C 60 min @ 150 °C	10 min @ 125 °C 60 min @ 150 °C	10 min @ 125 °C 60 min @ 150 °C	8 min @ 120 °C 60 min @ 150 °C	10 min @ 120 °C 60 min @ 150 °C

Overmolding was performed using a Towa universal molding system set for compression molding with a 200 mm diameter compression mold tool. MAP area PCBs were attached to a thermal release tape on a carrier substrate and overmolded at typically 125 °C and a postmold cure was applied at recommended PMC conditions. After molding the single packages were separated by laser cutting and handed over for shielding layer realization.

5-sided shielding metallization

For realization of a 5-sided metallization, acting as an efficient shielding, a new process flow was developed (Figure 5) for the efficient handling of smaller manufacturing volumes. First a PCB without copper was structured by mechanical milling to create cavities for package assembly.

Application of a tacky and sputtering as well as electroplating resisting tape on one side of the PCB frame allows for assembly of the singulated packages into the cavities of the PCB frame. After assembly of the packages sequential sputtering of two thin layers Ti (100 nm) / Cu (300 nm) took place where the Cu acts as seed layer for electrical Cu thickness enhancement by electroplating to thicknesses in micrometer range. For evaluation of the influence of the Cu thickness regarding shielding efficiency two Cu thickness ranges were targeted, 10–15 µm and 25-30 µm. After electroplating the packages were singulated and provided for preparation for electrical testing of the shielding efficiency. This sample stack-up and process sequence allows for electrical contact over the whole substrate and all sides of the assembled packages so that a 5-sided metallization of single packages could be realized.

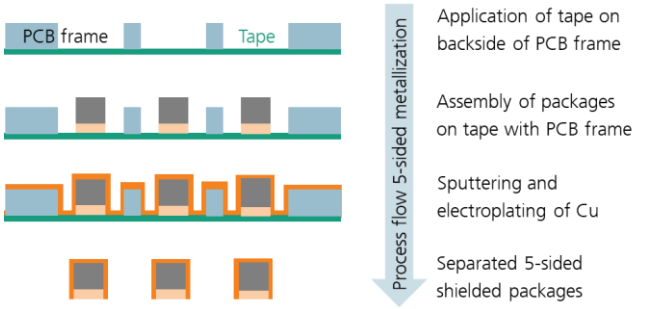

Figure 5: Process flow for 5-sided metallization process steps

For the future manufacturing of shielded packages an alternative flow is considered that replaces sputtering for the application of a seed layer by a direct metallization process based on Pd activation and subsequent Cu metallization.

Shielding efficiency measurement setup

The achieved shielding effectiveness was evaluated using a 3-axis table in combination with a SPEAG TDS near-field time domain probe.

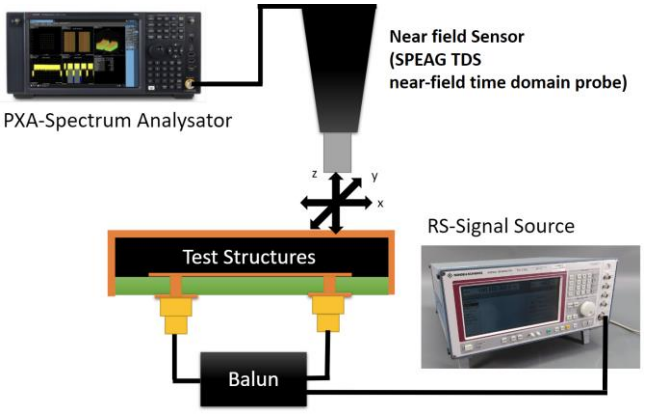

Figure 6: Measurement setup for shielding effectiveness measurement

IV. Results

MAP molding feasibility

Overmolding of MAP area PCBs was shown to be feasible. Nevertheless, EMC flash was observed on some samples. Due to through-hole vias in the PCB, mold compound can be pressed through the vias during compression molding and deposited as flash on the other side of the substrate (Figure 7).

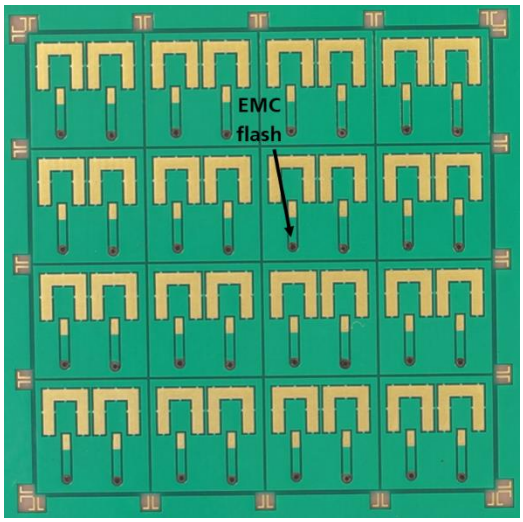

Figure 7: Camera image of an overmolded MAP area PCB with EMC flash on top of the through-hole via pads

To avoid flash, it is necessary to have a non-warping substrate and a good adhesion of the substrate to the thermal release tape. The choice of molding compound, taking into account the maximum filler size and viscosity of the epoxy resin is critical. Alternatively, the design of the overmolded substrate must be modified so that there are no through-hole vias or slots through which the EMC could flow.

Homogeneity of deposited metallized layer

To verify the thickness variance of all 5 metallized sides, cross-sections of samples of each thickness and mold material variant were prepared and then examined under an optical microscope. The examination showed that a uniform layer of the target thickness was achieved in the mold material area. However, in the circuit board area, strong topographies of the applied metal layer were observed, caused by protruding glass fibers of the circuit board material. The individual packages were separated by laser cutting. It should be possible to avoid this effect by selecting a suitable separation process, e.g. sawing or changing the laser parameters, or by changing the package concept so that also the side walls of the overmolded PCB are covered with EMC. In addition, a decrease in layer thickness was observed in the side area of the 5-sided metallization, which can be explained by the distribution of the electric field lines. Due to the resulting shading in the lower area, the film thickness decreases continuously towards the bottom. One way to

reduce shading is to increase pocket dimensions of the board frame.

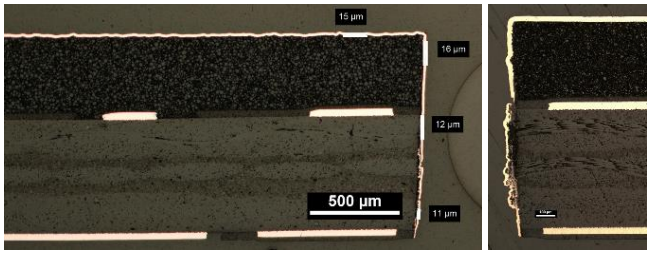

Figure 8: Cross-section of deposited metallized layer left: good sample; right: sample with protruding glass fibers

Adhesion strength of 5-sided direct EMC metallization

For a first quantitative orientation of the adhesion strength between the EMC package surface and the shielding metal stack-up a cross cut testing derived from DIN ISO 2409 was performed. Challenge for this test is the rather small size of the package of 10x10 mm². For layer thicknesses up to 50 µm a 6x6 line cut pattern is recommended, for testing the samples were predried for 30 min @ 120 °C and the cut pattern was applied using a fresh cutter knife. A polyimide tape, with an adhesion strength of 2-3 N/10 mm, was firmly attached to the top of a single package. Adhesive strength was evaluated by quickly pulling off the tape. The results of this test are categorized by ISO in 6 levels, where 0 indicates no removal of metallization, 1 indicates detachment of flakes of the metallization at the intersections of the cute (less than 5% area) and 5 indicates full removal of the metallization.

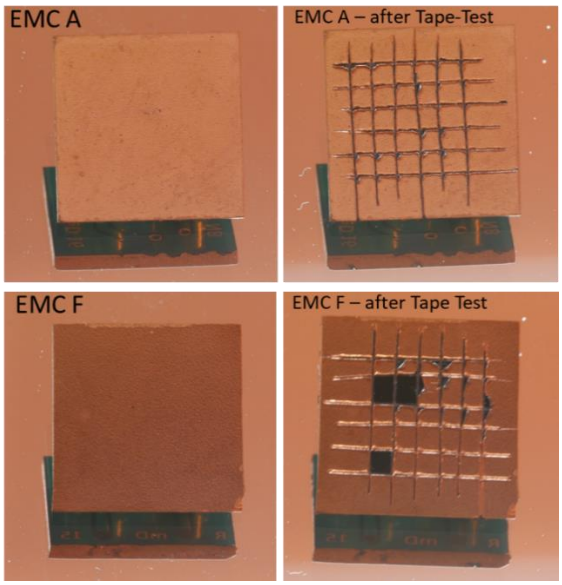

Figure 9: Images of molded and metallized packages prior to tape test (left) and after tape testing (right) revealing excellent adhesion = level 1 for EMC A (top) and reduced adhesive strength = level 3 for EMC F (bottom).

During tape test, only metallization on molding compound A showed excellent adhesion of the topside metallization, while reduced adhesion was observed for all other EMCs. The adhesion of the metallization layer on the side wall has also been evaluated by tape testing and is varying from good to poor. The lower adhesion there is most likely resulting from a non-ideal separation process quality, where glass fiber stubs are forming a rough surface and where adhesive tape residues, i.e. remains of the tape used to hold the packages in place during the metallization process, are reducing adhesive forces.

Technology variation dependent shielding efficiency measurements

The SE was calculated by subtracting the frequency dependent radiated power of an electrically small dipole from the fully molded and/or shielded test vehicle.
This accounts for the non-linear reflectivity of the antenna. The probe distance to the radiating element is 1.5 mm. For the shielded and molded probe 0.5 mm is covered by the mold and shielding layers. The measured magnetic field can be observed in Figure 10. The results show only a small but increasing deviation from the model from 10 MHz to about 800 MHz. Above this frequency, the deviation from the model increases. This can be explained by the non-ideal shielding geometry and fields penetrating through the fabrication defects at smaller wavelengths.

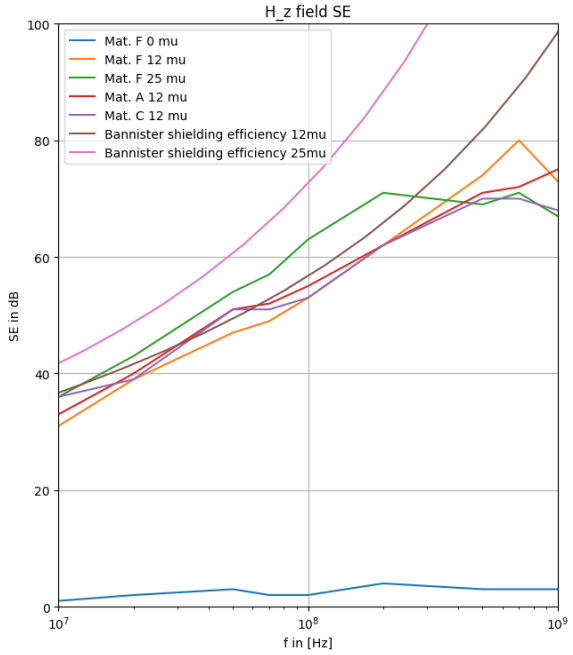

Figure 10: Magnetic field attenuation relative to a unshielded antenna. Both simulated with two different shielding thicknesses as well as multiple mold material technologies as well as with and without shielding.

The test vehicles, which are not shielded by copper but only by the mold, show only a very small attenuation of 3 dB. Different mold materials also have little effect on the attenuation of a shielded test vehicle. Varying the shielding thickness shows the predicted improvement until the experimental results begin to deviate from the model at about 800 MHz for 12 µm of shielding thickness and 200 MHz for 25 µm shielding thickness. The radiation limits presented in the CISPR16 for magnetic field emissions define various quasi-peak values for three distances (3 m, 10 m and 30 m). At 10 MHz the shielding virtually moves the protected circuit nearly 27 meters away from the disturbance.

V. Conclusion

The study demonstrated the feasibility of overmolding MAP printed circuit boards as a key process for the manufacturing of highly integrated system in a package. Shielding layer application compatible with this process was developed for small volume manufacturing and the shielding efficiency was measured for a variety of technological variants, yielding a sufficient shielding efficiency for the targeted application. This metallization process is also the basis for future integration of additional functionality into molded packages as e.g., an integrated antenna based on a structured metallization on package level.

In addition, the adhesion strength of the 5-sided direct EMC metallization varied, with excellent to good adhesion on the top side but poorer adhesion on the side walls, possibly influenced by surface structure and deposition process. This underscores the need for further investigation into long-term adhesion and the selection of appropriate EMCs for effective shielding.

Finally, shielding effectiveness measurements showed only minor deviations at lower frequencies, but significant deviations above 800 MHz due to non-ideal shielding geometry and manufacturing defects. Adjusting the shielding thickness provided improvements, but the deviations from the model increased at higher frequencies.

Overall, while the study confirms the potential of overmolded packages with 5-sided metallization for improved electronic packaging, it also underscores the need for continued refinement of process techniques and materials to achieve optimal reliability and performance.

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