Using a Novel Co-Design Prototyping Approach for System-in-Package Devices

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Abstract

System technology co-design (STCO) is the critical process of optimizing the interface between integrated IC device(s), package, and printed circuit board (PCB) at the early stages of product design and development. STCO can avoid poor system planning which could otherwise impact cost, yield, and performance. This paper focuses on the challenges and opportunities of STCO for system-in-package (SiP) and multi-chip package (MCP) solutions, which use a combination of wire bond and flip-chip die as well as SMT (surface mount technology) passive components. A scalable methodology is presented that uses Xpedition Substrate Integrator, a software tool for single-die ASIC and 2.5/3D packaging that automates the optimization of the system-level netlist, to achieve robust floorplanning and connectivity efficiency for SiP co-design. Compared to manual methods, this specialized workflow on typical SiP designs reduced up to 10-14% decrease in net congestions, leading to improvements in form factor, cycle time, and performance.

Key words

System co-design, System-in-Package, Xpedition Substrate Integrator, planning.

I. Introduction

System technology co-design (STCO) is a critical piece of product design and development where a complex semiconductor system is partitioned or disaggregated into smaller partitions that can be designed asynchronously and concurrently. Although cost, yield and performance take center stage throughout the design process, many of these challenges can be traced back to the interface scheme developed at those earliest design stages of the system comprised of IP macros, integrated IC device(s), package, and printed circuit board (PCB). Once these components are combined into a single product, the full system netlist will have a strong influence on the physical design implementation. Poor planning in any one of these domains, without the context of the entire system, can result in higher layer counts to resolve route crossings, degraded electrical performance, and missed opportunities for overall product efficiencies. In addition, challenges in the form of power integrity, signal integrity, thermal performance, warpage, and mechanical stress can emerge. Co-design workflows focus on facilitating and analyzing the tradeoffs surrounding these types of optimizations at the earliest development stages where the opportunities are greater. Moreover, they enable the optimal development process for each partition of the design without over-constraint. However, the data for all the partitions must come together during package planning. Thus, to capitalize on these opportunities for optimization in today's modern ecosystem of semiconductor IP suppliers, customers, fab-less chipmakers, etc., the reality of co-design often includes prototyping multiple and complex product SiPs and product SiP line scenarios within critical time windows when the requirements and standards for those next-generation technologies are being established.

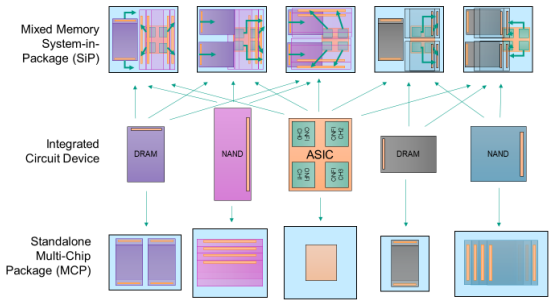

Fig. 1

II. CURRENT CHALLENGE

A. Retrofitting ECAD Workflows for Co-Design

Today, ECAD tools such as Cadence Allegro Package Designer and Xpedition Package Designer are primarily used for single product design execution to bring a set of requirements to a final deliverable for backend assembly processes. By design, the software makes it difficult to conveniently change data related to form factor, netlist, and routing, commonly required for co-design efforts. Thus, using a standard ECAD workflow to execute typical co-design would result in cumbersome process steps at a deeper abstraction level than necessary. Moreover, conducting multiple prototype scenarios simultaneously can further complicate co-design objectives in these tools. Even if you are able to employ design reuse methodologies to overcome some of these inefficiencies, ECAD tool workflows completely breakdown with no standardized solution to co-optimize across prototypes based on a set of global metrics (see Fig. 2).

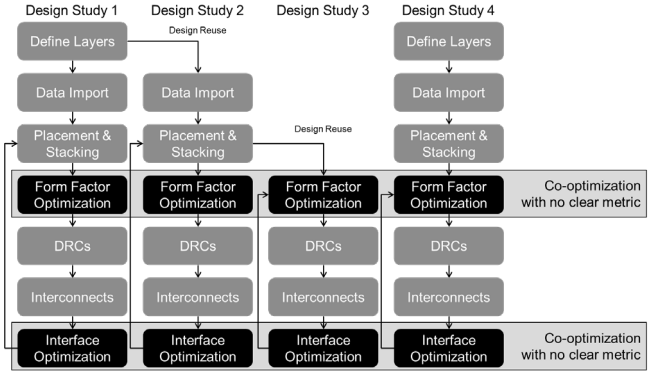

Fig 2.

B. Co-design EDA Landscape

New software prototyping/planning tools such as Xpedition Substrate Integrator are commonly shown to improve co-design flows by automating the unraveling of the system-level netlist specifically for single-die SoC and 2.5D/3D package solutions which make use of IP macros, chiplets, Through-Silicon-Via (TSV), and other advanced technologies due to their high pin count, heterogeneous integration, and complexity. However, the highest volume memory products use a combination of wire bond and flip-chip (Direct Chip Attach) die as well as SMT passive components to provide system-in-package (SiP) and multi-chip package (MCM) solutions in the industry (shown in Table I). These tools are missing standardized workflows and, in some cases, key functionalities to properly address real-world memory packaging applications, forcing many engineers to fall back on traditional ECAD software not suitable for co-design.

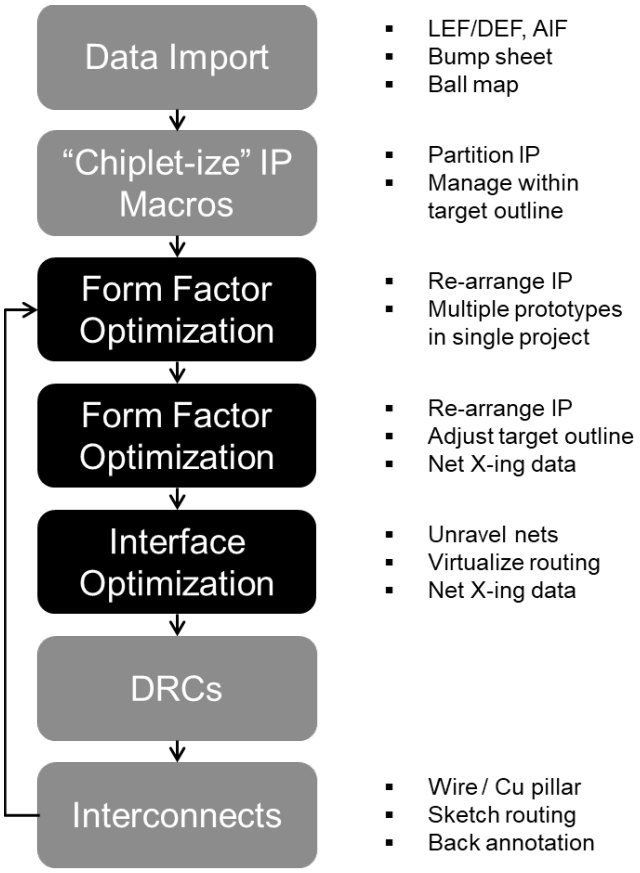

Fig. 3

C. Unique Co-design Complexity of SiP

System-in-package co-design transcends the critical effort of single device floorplanning and subsumes concurrent optimization, or co-optimization, with paired IC devices of different technologies, applications, and attachment types (i.e., wire bond, flip-chip, etc.). Additionally, to create diverse product line roadmaps, a single ASIC device will be integrated with a variety of memory devices in several package combinations as shown in Fig. 1. Similarly, these individual devices will go into their own standalone MCM package which have different product requirements to meet. Thus, optimizations to SiP packages during the co-design stage must occur across 100s of configurations, translating to 10,000s of i/o.

TABLE I

	HBM	uMCP	DRAM	ASIC
Interconnect	TSV	DCA + WB	WB	DCA
No. of IC	4 – 8	17	1	1
Footprint	110mm^2	117mm^2	82.5mm^2	289mm^2
Integration	Heterogeneous		Homogeneous	

III. SOLUTION

Our specialized workflow (shown in Fig. 3) was developed in Siemens Xpedition Substrate Integrator (XSI) to not only

enable package design engineers working on SiP to break into co-design EDA software, but also leverage those enhanced automations tailored to chiplet applications and be truly efficient and data-driven with co-optimization trade-offs with key length-based electrical metrics.

A. Create ASIC IP Chiplets

There are different ways to create chip-level data in XSI. One of the most common at this stage is using a spreadsheet format. EDA formats such as LEF/DEF are also supported and generally recommended. These formats enable a better integrated experience between design software suites.
The ASIC device usually consists of IP macros that form the whole floorplan and come pre-integrated as a bump map. As long as we know which bumps belong to each macro, XSI lets us divide the ASIC and show it at this abstraction level. By separating IP macros like this, we can follow the standard chiplet workflows in the tool and easily optimize each block separately. At the same time, the blocks and target die shadow can be grouped together and moved as a single device. This approach helps us find the best form factor and floorplan for the ASIC in the next steps.

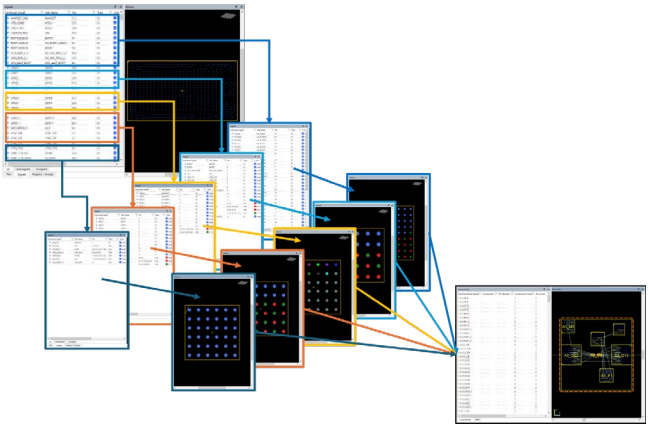

Fig. 4

B. Form Factor and Configuration Co-Optimization

Our optimization goal was to reduce the metrics of net crossing and total net length, which are built-in features of the tool. By improving these metrics, we can achieve smaller substrate sizes and fewer layers, and enhance performance. The first custom element we introduced to create this specialized workflow was our method of co-optimizing across multiple studies. Current standard flows only allow optimizing within a single system. To overcome this, we combined all studies into one XSI project environment. We developed custom TCL automation to support this effort in XSI, as this capability was almost non-existent before. The benefit here is that any optimization done on one study, such as net cross reduction, IP arrangement, or bump adjustments, will synchronize across the other studies for more analysis or optimization. This allows us to better comprehend trade-offs at the whole portfolio level.

C. Capturing Wire Bond and Route Crossings

The most efficient design is not always achieved by only optimizing the metrics of net crossings and net length based on the relative locations of pins. Crossings can occur when doing wire bonds and routing traces to avoid bumps. For our application, it is crucial to account for these physical aspects of the design, especially for wire bond where there are usually no alternatives to undo or fix crossings. XSI's ability to import ODB++ data, which captures this information, was one of the reasons we chose it as the tool for our flow.

D. Package Route Planning

In some cases, we can solve crossings by using trace routing. XSI virtual route planning feature allows us to investigate these options. A key feature of virtual route planning is that we can enter lines and space requirements that can then show us the exact size of our routing channel. This feature helps us to know and deal with real-estate issues within our target form factors.

IV. RESULTS

In our co-design use case, we utilized XSI for trade-off analysis to optimize floorplan configurations for our next-generation ASIC in mNAND applications. Table II presents comparative data on two distinct floorplans (Floorplan 1 & Floorplan 2). Floorplan 1 served as the benchmark, while Floorplan 2 incorporated IP macro rearrangements, resulting in a reduced die size. Our goal was to quantitatively demonstrate the efficiency improvements in terms of die size reduction and package routing.

Also in Table II, we assessed these efficiencies against seven early-stage prototypes (1 – 7) from our product roadmap where in which the device floorplan was integrated with the larger SiP solution. This evaluation was critical to determine if any prototypes were adversely affected by Floorplan 2. Our team applied the specialized workflow discussed to systematically analyze the net crossings as the primary metric to determine package routing efficiency.

A. Analysis A

Analysis A looked purely at pin-to-pin crossings without capturing physical design elements such as wire bonds and trace routing, offering a rapid preliminary assessment. We observed that Floorplan 2 yielded a 13.27% average decrease in net crossings among the initial prototypes.

B. Analysis B

Analysis B introduced Prototype 2, a cost-reduction variant not considered in Analysis A. This inclusion revealed that Floorplan 2 had a distinct impact on routing efficiency, triggering the team to conduct a deeper study.

C. Analysis C

Finally, Analysis C focused on adapting Prototype 2 to Floorplan 2. Through strategic die stacking and placement, as well as wire bond and routing optimizations, we further minimized crossings. This led to a 14.01% efficiency gain for Prototype 2 and an overall increase to 14.26% for Floorplan 2.

TABLE II

ANALYSIS A	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**OVERALL**
Floorplan 1	732	N/A	941	1643	829	1729	1863	10709
Floorplan 2	644	N/A	768	1548	725	1642	1419	9288
Improvement %	-12.02	N/A	-18.38	-5.78	-12.55	-5.03	-23.83	-13.27
ANALYSIS B	1	2	3	4	5	6	7	OVERALL
FLOORPLAN 1	732	885	941	1643	829	1729	1863	10436
FLOORPLAN 2	644	1010	768	1548	725	1642	1419	9344
IMPROVEMENT %	-12.02	+14.12	-18.38	-5.78	-12.55	-5.03	-23.83	-10.46
ANALYSIS C	1	2	3	4	5	6	7	OVERALL
FLOORPLAN 1	732	678	941	345	829	1729	1863	8931
FLOORPLAN 2	644	583	768	288	725	1642	1419	7657
IMPROVEMENT %	-12.02	-14.01	-18.38	-16.52	-12.55	-5.03	-23.83	-14.26

V. CONCLUSION

The challenges inherent to system-in-package can uniquely be demonstrated by considering the standalone products of each device as well as the mixed technology products. Understanding that co-optimization must occur across the entire spectrum of products is the blind spot in today's EDA co-design landscape.

With XSI, we can fill several gaps by leveraging automation designed for advanced packaging as outlined in this paper. Here we have established a reproducible framework which makes co-design in this technology space more efficient.