

Ultra-low Loss Build-up Film Dielectric for Advanced Packaging

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Abstract

This paper introduces a novel low-loss film dielectric material and describes the performance of the material. As the demand for faster, smaller, and more energy-efficient electronic devices continues to surge, the IC substrates must have the capability of meeting the stringent requirements, especially to support high speed signal transmissions. As the signal frequencies increase, the importance of reducing dielectric loss is getting more critical in enhancing the performance of IC substrates. However, achieving ultra-low loss characteristics in build-up dielectric materials remains a formidable technical challenge, hindered by the inherent limitations of traditional epoxy-based materials. This paper introduces a novel build-up dielectric material that addresses the technical limitation of the conventional materials. Leveraging advanced material design and process technology, the new dielectric film material offers ultra-low electrical loss characteristics with robust reliability performance and standard manufacturing processes compatibility. The unique material design bestows extremely stable electrical performance at higher temperatures. Signal transmission measurement demonstrated that the new material exhibited approximately 40% lower transmission loss compared to the conventional material. The superior characteristics make the dielectric material ideal for advanced packaging in high performance computing, telecommunications, and evolving automotive applications.

Key words

Build-up material, Low loss, High speed, Signal transmission, High performance computing

I. Introduction

The integrated circuit (IC) substrate industry stands at a critical juncture, driven by the continuous advancement of high-speed digital applications and emerging technologies such as artificial intelligence (AI), the Internet of Things (IoT), and autonomous driving. Developing new materials that meet the high-performance standards of advanced semiconductor devices is essential for advancing these technologies. Among these materials, ultra-low loss build-up dielectric films play a pivotal role in enhancing the speed, reliability, and functionality of IC substrates, thereby fueling innovation and driving the evolution of electronic systems. In recent years, the demand for faster data processing speeds, greater bandwidth, and increased energy efficiency has led to major changes in the IC substrate industry, necessitating the development of novel materials that can meet the demands of high-performance computing. A key challenge here is minimizing signal loss within IC substrates, which depends on dielectric materials with ultra-low loss characteristics [1, 2].

The technical challenges associated with achieving ultra-low loss build-up dielectric films are complex and involve various aspects, including material design, fabrication

processes, and performance optimization. Traditional dielectric materials, such as epoxy resins, while widely used for their mechanical robustness and processability [3, 4, 5], often suffer from high dielectric losses, particularly at higher frequencies and temperatures. This inherent limitation significantly hinders the development of IC substrates that can support ultra-fast signal propagation for advanced semiconductor devices.

To overcome the challenges, this paper introduces a novel build-up dielectric film material (Material Z) tailored to the specific needs of high-speed digital and AI-related applications. Based on the advanced material design principles and process technologies, the new material demonstrates ultra-low loss characteristics while maintaining mechanical robustness and compatibility with existing manufacturing processes. Through a comprehensive analysis of material properties, performance metrics, and reliability considerations, this paper highlights the transformative potential of Material Z in enabling the next generation of IC substrates for the era of high-performance computing, telecommunications, and evolving automotive applications.

II. Material Design

Developing ultra-low loss build-up dielectric films requires chemistry and material processing approaches based on a deep understanding of the fundamental properties needed for advanced IC substrates. This chapter explores the principles and strategies for designing a new material (Material Z), focusing on the principal factors that affect their performance in high-speed digital and AI applications. Key design parameters are, 1. Electrical properties, 2. Mechanical properties, and 3. Thermal stability.

First, as the electrical properties, the dielectric constant (D_k) and loss tangent/dissipation factor (D_f) are crucial for dielectric materials. The dielectric constant determines the material's ability to store electrical energy, while the loss tangent measures the energy dissipation as heat. For ultra-low loss applications, a low dielectric constant and loss tangent are essential to minimize signal attenuation and power consumption, especially at high frequencies. Achieving such characteristics requires specific design and engineering of the molecular structure. Conventional epoxy-based materials have limitations in reducing D_f , because of polar functional groups as an artifact of polymer curing reactions. To overcome the technical limitation, Material Z applied a new curing system with a lower polarity structure based on polyphenylene ether (PPE). Our team has synthesized a new PPE chemistry that can be dissolved in standard organic solvents, such as cyclohexanone, ethyl acetate, and methoxy propyl acetate [6]. The new PPE enabled the fabrication of ultra-low loss dielectric film by solvent-based processing. Solvent-based processing involves dissolving the PPE polymer and fillers in a solvent to form a uniform solution, which is then cast into thin films and dried to remove the solvent, leaving a solid dielectric layer. This method allows precise control over film thickness and composition, ensuring uniform electrical properties. To achieve ultra-low loss characteristics, the polymer matrix was reinforced with silica fillers.

Table 1. Properties of film dielectrics

Cured Properties	Material Z	Conventional epoxy-base
T_g [deg. C]	190	170
CTE α_1 [30-100 deg. C]	18 ppm/K	17 ppm/K
Young's Modulus [GPa]	10	12
D_k @10GHz	3.1	3.4
D_f @10GHz	0.0015	0.0045
Water absorption [%]	0.05	0.5

Second, thermo-mechanical robustness, such as high glass transition temperature (T_g), low coefficient thermal expansion (CTE), and high modulus, is crucial for reliability

of IC substrates. Material Z has promising thermo-mechanical properties that ensure high reliability of IC substrates (Table 1), due to the mechanical reinforcement of the polymer by silica fillers. Figure 1 shows the cross section of Material Z to display the highly uniform distribution of filler particles in the polymer matrix.

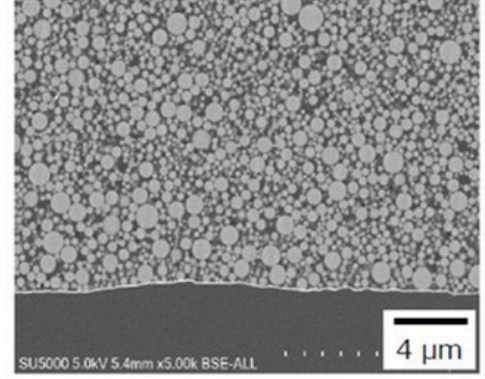


Figure 1. SEM cross section of Material Z

Finally, thermal stability is another critical factor, particularly for applications in high-performance computing and automotive electronics, where substrates are exposed to elevated temperatures. The material must maintain its dielectric properties and mechanical integrity across a wide temperature range to ensure consistent performance and reliability. As illustrated in the previous section, Material Z has quite robust thermo-mechanical performance. Additionally, measurements of dielectric properties for Material Z and a conventional epoxy-based low loss material were examined over different frequencies and temperatures. First, Material Z and a reference epoxy-based material were fully cured to form free-standing film samples with dimensions of 40 mm in length, 40 mm in width, and 30-35 μm in thickness. Then, 6-7 stack of the free-standing film samples (total thickness around 200 μm) were attached to a balanced type circular disc resonator (BCDR) for measurement of D_k and D_f of the materials at different temperatures (-50 $^{\circ}\text{C}$, 23 $^{\circ}\text{C}$, 50 $^{\circ}\text{C}$, 100 $^{\circ}\text{C}$, and 150 $^{\circ}\text{C}$) and at different frequencies (25 GHz and 70 GHz). BCDR method was selected because it is recognized as an accurate method for measuring dielectric properties for low loss dielectrics at high frequency up to 170 GHz [7]. Figures 3 and 4 show D_k measurement data of Material Z (blue) and conventional epoxy (red) over different temperatures at 25 GHz and 70 GHz, respectively. Although a slight D_k increase was detected in conventional low loss epoxy material at 25 GHz (within 0.3) in this temperature range, both materials had highly stable D_k values over the temperature range.

The situation became quite different for D_f values. Figures 5 and 6 are the D_f measurement results of the materials at 25 GHz and 70 GHz, respectively. A significant difference in

material performance is visible here, and Material Z has much higher stability than the epoxy-base low loss material against temperature change. This outstanding stability in dielectric loss makes Material Z extremely favorable for high performance computing, telecommunication, or AI-related applications, because high speed or high frequency data transmission generates excess heat in circuitry which negatively impacts dielectric performance to worsen signal attenuation. Such diverging effect is expected to be minimized by applying Material Z for dielectric layers, instead of epoxy-based materials.

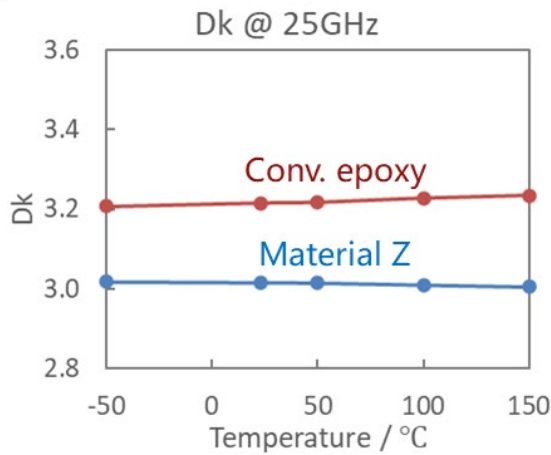


Figure 3. D_k by BCDR at 25 GHz of Material Z (blue) and conventional low loss epoxy (red) versus temperature

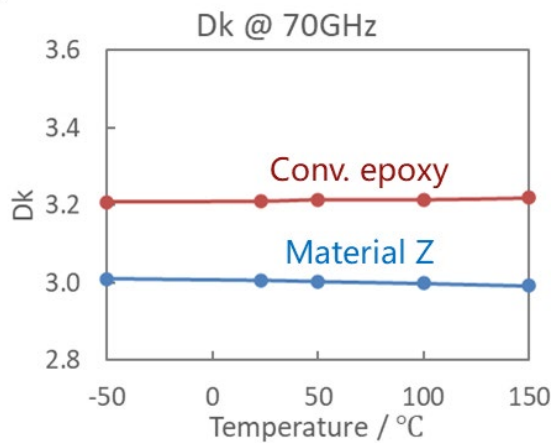


Figure 4. D_k by BCDR at 70 GHz of Material Z (blue) and conventional low loss epoxy (red) versus temperature

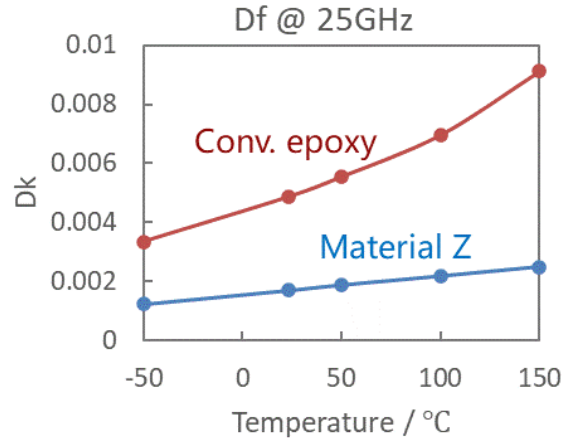


Figure 5. D_f by BCDR at 25 GHz of Material Z (blue) and conventional low loss epoxy (red) versus temperature

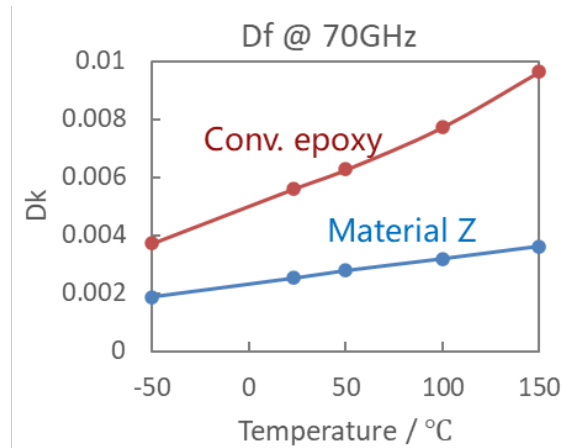


Figure 6. D_f by BCDR at 70 GHz of Material Z (blue) and conventional low loss epoxy (red) versus temperature

The process schematics of Material Z as a build-up dielectric layer is summarized in figure 7. First, MECetchBOND CZ-8101 and CL-8300 are applied to the underlying Cu layer as the pre-treatment of the base substrate for enhancement of adhesion between the Cu and the build-up dielectric layers. Then vacuum lamination is applied to deposit Material Z on the base substrate with CVP-600 from Nikko Materials, and material filling between the underlying Cu circuit structures is completed in this step, followed by the thermal curing of the material at 200 °C for 60 minutes in a nitrogen oven. After the material cure, various laser drilling processes can be applied to form micro-vias to interconnect top and bottom metal layers, and wet or dry desmear processes are applied to clean the vicinity of the

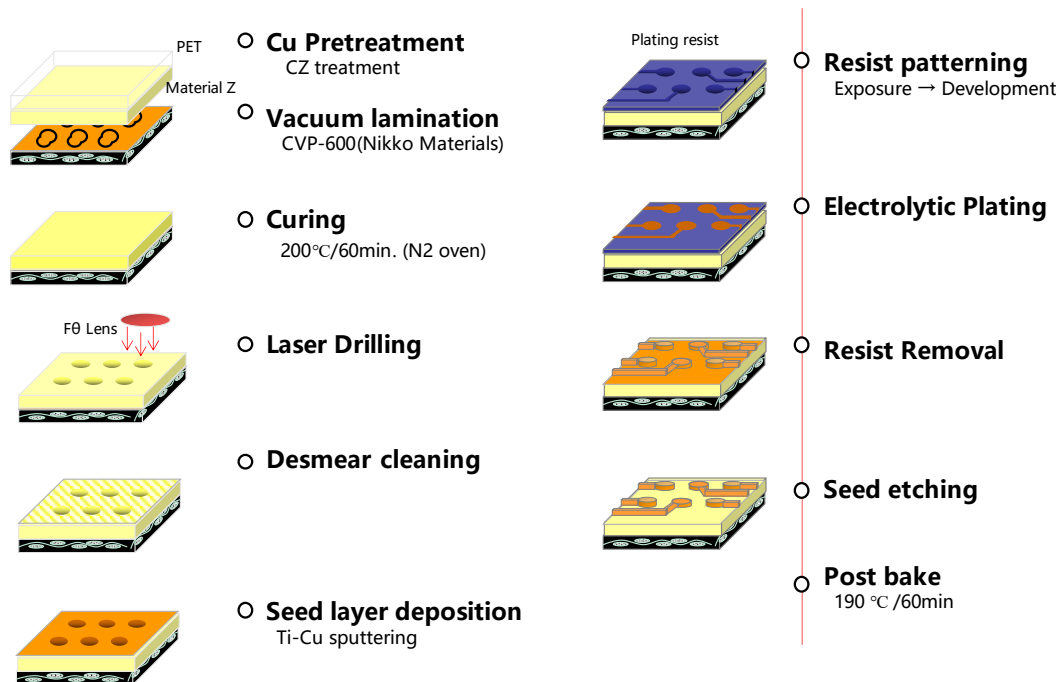


Figure 7. Build-up dielectric process with Material Z

micro-vias. Finally, a semi-additive process, including resist patterning and plating processes, is adopted to complete Cu wiring formation on top of the dielectric layer. Material Z is fabricated in roll format, and figure 8 shows the appearance of the material.

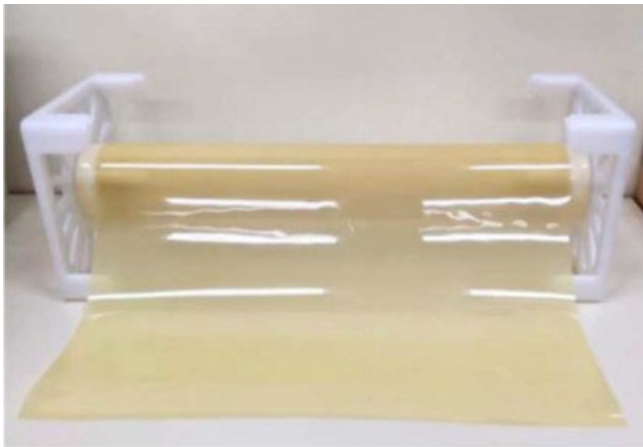


Figure 8. Material Z appearance in roll format

III. Material Performance Analysis

A. Transmission Line Measurement

A detailed analysis of transmission line measurements was conducted to compare the performance of Material Z and the conventional low loss epoxy material. These measurements

offer critical insights into the transmission loss characteristics, highlighting the significant advancements offered by the new material in high-speed digital and AI-related applications.

Sample substrates were fabricated with Material Z and the conventional low loss epoxy as the dielectric layers, then micro-strip line structures were patterned on the dielectric layers by semi-additive process described earlier. Strip line dimensions and substrate design for this measurement are illustrated in figure 9. The substrate dimensions were defined to achieve impedance matching at 50 ohms. The primary metric of interest in this study is transmission loss, which directly affects the efficiency and performance of high-speed signal transmission in IC substrates.

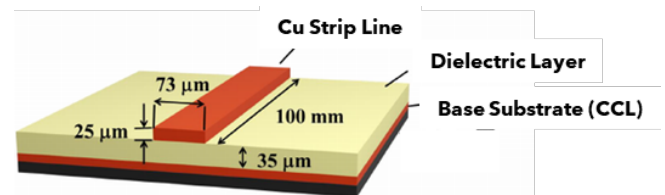


Figure 9. Substrate design for the transmission line test

First, vector network analyzer (VNA) was calibrated using a calibration kit to account for any system-induced errors over measurement frequency range up to 100 GHz. Next, each sample was connected to the VNA, and S-parameters were recorded over the frequency range. Finally, the recorded S-parameters were analyzed to calculate the transmission loss (in dB) for each material. The analyzed S₂₁

data over frequency range up to 100 GHz is summarized in figure 10. In the frequency range of this study up to 100 GHz, micro-strip line with Material Z demonstrated approximately 40% lower transmission loss compared to that of the conventional low loss epoxy material. Previous research on the radio frequency (RF) application of Material Z also demonstrated quite low transmission loss for low-pass and band-pass filter structures [8]. Such substantial reduction in transmission loss is crucial for high-speed and high-frequency applications, as it directly translates to higher signal integrity, lower power consumption, and wider bandwidth capacity.

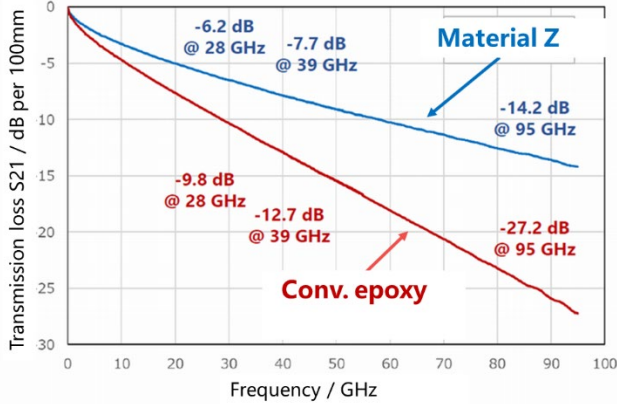


Figure 10. S21 analysis of Material Z (blue) and conventional low loss epoxy (red)

B. Material Reliability

Ensuring the reliability of ultra-low loss dielectric materials is crucial for their adoption in high-performance IC substrates. In this section, reliability of the novel dielectric material was examined through the biased highly accelerated stress test (BHAST) and peel strength measurements. These tests provide comprehensive insights into the material's durability and long-term performance under operational stress conditions.

Test coupons of Material Z for BHAST were fabricated as follows: A 35 μm thick layer of Material Z was laminated on a base substrate and fully cured. Subsequent SAP processes were applied to form 12 μm width line & 13 μm space Cu patterns on top of the dielectric layer. After Cu patterning, another layer of Material Z was laminated on top to encapsulate the Cu patterns and fully cured. A CO_2 laser was then used to form 40 μm micro-vias, and metallization was performed to create interlayer electrical connections. Finally, probe structures were patterned to complete the test coupon fabrication. After the fabrication, test coupons were exposed to the preconditioning with 85 $^\circ\text{C}$, 60% relative humidity (RH) for 168 hours (JEDEC level 2), followed by three times of reflow process at 260 $^\circ\text{C}$. Then the coupons were placed in a BHAST chamber (EHS-221MD from Espec) with 130 $^\circ\text{C}$, 85% RH, and a bias voltage of 12 V was

applied between the 12 μm width line & 13 μm space Cu patterns. Electrical resistance between the Cu patterns in randomly selected 5 coupons were monitored up to 240 hours, and no significant resistance drop was observed for all the tested Material Z coupons (figure 11). This result demonstrates excellent dielectric performance of Material Z against high temperatures and humidity.

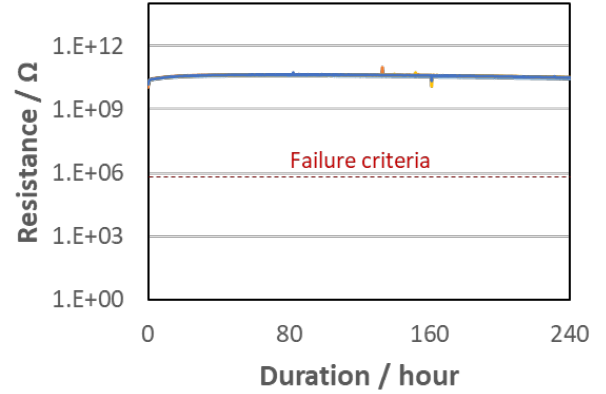


Figure 11. Resistance data of the substrate with Material Z under BHAST condition (130 $^\circ\text{C}$, 85% RH, 12 V)

The 90-degree peel strength measurement was employed to evaluate the adhesion of Material Z and plated copper layer. Test coupons were prepared through the same SAP processes starting from sputtering Ti-Cu seed layer and electrolytic Cu plating to attain 12 μm thick Cu on Material Z. The Cu layer was then patterned into 1 cm width of strips. The prepared samples were clamped into the testing machine and the Cu strips were peeled off at a 90-degree angle with a constant rate of peeling. The lifting force was measured during the peeling, and the peel strength was calculated by dividing the force by the width of the sample strip (1 cm). Excellent peel strength of 8.9 N/cm was achieved, ensuring compatibility with standard manufacturing processes. This makes Material Z an ideal candidate for integration into existing production lines without significant modifications.

IV. Conclusion

This paper presented a comprehensive analysis of a novel ultra-low loss dielectric material designed for advanced IC substrate applications. The advanced material design based on the innovative polymer and fabrication technologies not only achieves ultra-low loss characteristics but also ensures excellent stability of ultra-low loss performance at elevated temperature conditions. Comparison research on the transmission line measurement was conducted. The results highlighted a significant reduction in transmission loss, with the new material exhibiting approximately 40% lower loss than conventional material across various frequency ranges. This improvement is critical for high-speed digital and AI-related applications, as it enhances signal integrity, reduces

power consumption, and supports higher data rates and greater bandwidth. The BHAIST results confirmed the material's exceptional resistance to thermal and humidity stress, with minimal degradation. The peel strength test proves superior adhesion strength, indicating robust mechanical integrity of Material Z.

The superior performance and reliability of the novel ultra-low loss dielectric material make it an ideal candidate for advanced packaging in high-performance IC substrates. Application of Material Z can significantly enhance the speed, reliability, and functionality of electronic systems, driving innovation in fields such as high-performance computing, telecommunications, and automotive electronics.

References

- [1] MD Islam, Y. Fu, H. Deb, MD Hasan, Y. Dong, and S. Shi, "Polymer-based low dielectric constant and loss materials for high-speed communication network: Dielectric constants and challenges." *European Polymer Journal* vol. 200, 2023, p. 138-148
- [2] C. Zhong, W. Chen, W. Kong, S. Yu, J. Lu and R. Sun, "A Comprehensive Study on Signal Integrity of Build-up Film Applied to IC Substrate," 2023 24th International Conference on Electronic Packaging Technology (ICEPT), Shihezi City, China, 2023, pp. 1-5
- [3] S. Tatsumi, "Advanced Insulation Materials for Next Generation Packaging Technology." 2022 IEEE CPMT Symposium Japan (ICSJ), 2022, pp. 111-114.
- [4] P. Karunaratna, K. Chithradewa, S. Kumara, C. Weerasekara, R. Sanarasinghe and T. Rathnayake, "Study on Dielectric Properties of Epoxy Resin Nanocomposites," 2019 International Symposium on Advanced Electrical and Communication Technologies (ISAECT), Rome, Italy, 2019, pp. 1-5
- [5] E. Horiki, I. Suzuki, T. Tanaka, A. Uenishi and K. Shiomi, "Build-up electrical insulation material with low-dielectric loss tangent, low-CTE and low-surface roughness," 2011 IEEE 13th Electronics Packaging Technology Conference, Singapore, 2011, pp. 363-368
- [6] M. Koh et al., "Novel thermosetting low Dk/Df film and its performance," 2022 International Conference on Electronics Packaging (ICEP), Sapporo, Japan, 2022, pp. 63-64
- [7] M. Horibe, Y. Kato and R. Sakamaki, "Electromagnetic Measurement Techniques for Materials and Device Used in 6G Wireless Communications," 2020 2nd 6G Wireless Summit (6G SUMMIT), Levi, Finland, 2020, pp. 1-5
- [8] T. Kakutani et al., "Advanced Low Loss Dielectric Material Reliability and Filter Characteristics at High Frequency for mmWave Applications," 2020 IEEE 70th Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2020, pp. 653-659