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Reliably Thin Electronics

IMAPS 20TH INTERNATIONAL CONFERENCE & EXHIBITION ON DEVICE PACKAGING
FOUNTAIN HILLS, AZ · WWW.DEVICEPACKAGING.ORG · MARCH 18-21, 2024

P-WLCSP Advanced Packaging Enabling Next Generation Medical Device Applications

March 2024

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Ed Prack

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Semiconductor - Industry at a glance

Semiconductor Industry

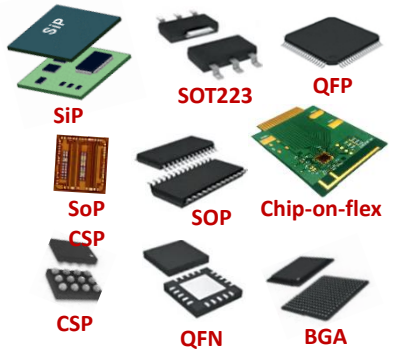
Design

Fab

Fabricated Wafer

Packaging

Cut into Die



Packaged into Chips

Micron, SAMSUNG, intel

IDM

Traditional Packaging

Fabless
Qualcomm, XILINX, NORDIC SEMICONDUCTOR, BROADCOM, HISILICON

Foundry
tsmc, GLOBAL FOUNDRIES, Tower Semiconductor, jstf, SMIC, LA SEMICONDUCTOR, skywater

AP/OSAT
Amkor Technology, ASE GROUP, INTEGRA TECHNOLOGIES

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Medical device Semiconductor prototyping and production

EMS Companies and End Users

Ford, BOEING, CET, SANMINA, MST, Promex

Advanced Medical Device Market

J&J, NEURALINK, Precision, verily, TWENTY/TWENTY, stryker, MERIT MEDICAL

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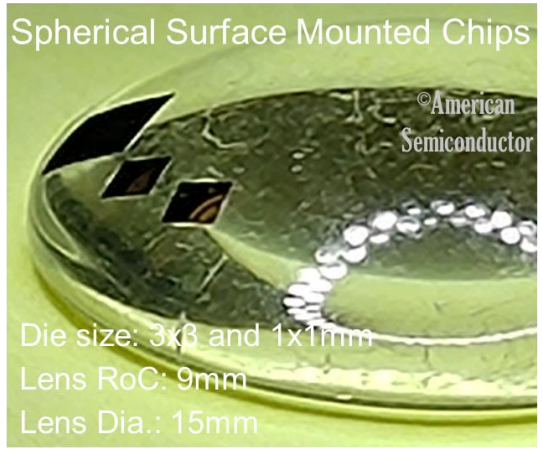
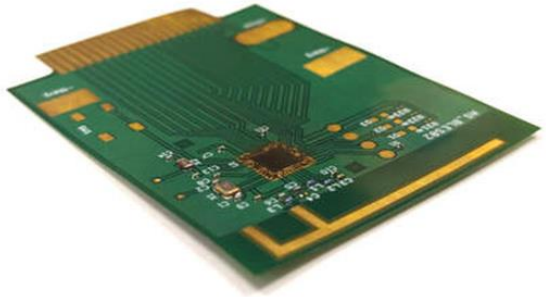
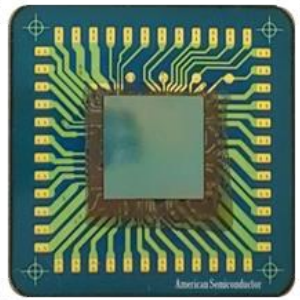
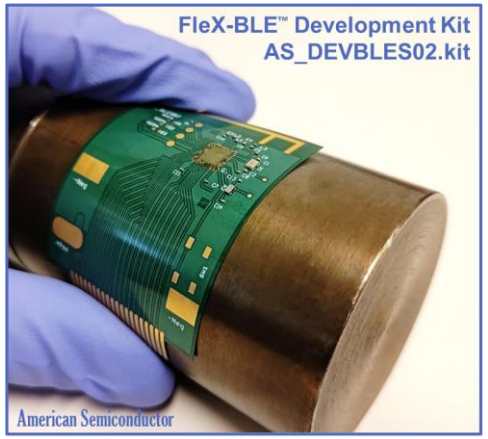
SoP and Chip-on-flex Advanced Manufacturing

Technology to produce flexible hybrid systems (FHS)



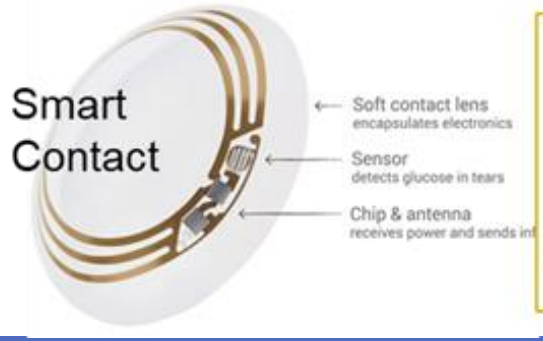


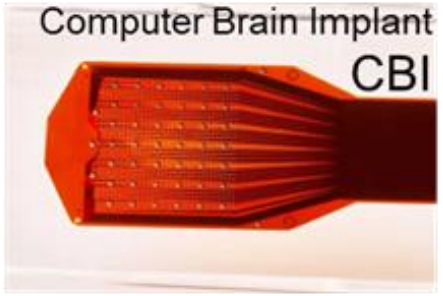




"Do you know that you are the only guys that can do this?" - Razi Haque, Lawrence Livermore National Lab

Next Generation Medical Devices





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Semiconductor-on-Polymer (SoP)

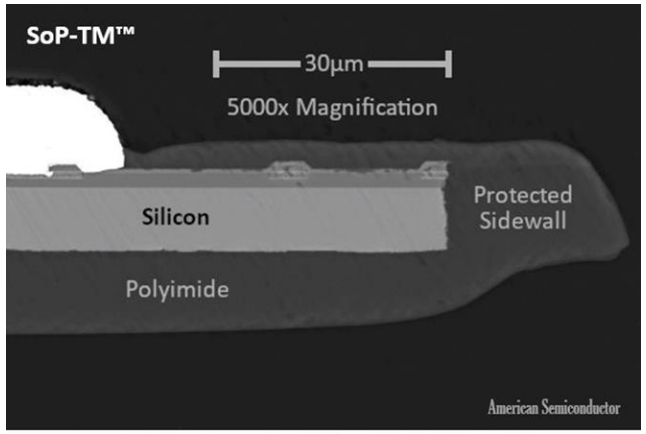
SoP-TM™ 6-side (6S) protected P-WLCSP

- WL 300mm Process – no reconstitution
- Polyimide encasement
- Maskless
- Adaptive process expands the selection of PIs
- Plasma/Laser singulation
- High reliability ENIG bump structure (bump over PI)
- COF Compatible

Unique Med-Tech Benefits:

Ultra-thin package, <30um Tx typical

Physically flexible, <10mm RoC typical



A cross-section view of a SoP-TM™ test die

SoP-TM™ Test Die Samples in case

Early Adopters: ***Medical Device and AR/VR wearables***

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Die Strength Comparison

Static RoC Testing (TEST003)

Manual conformance to RoC mandrel

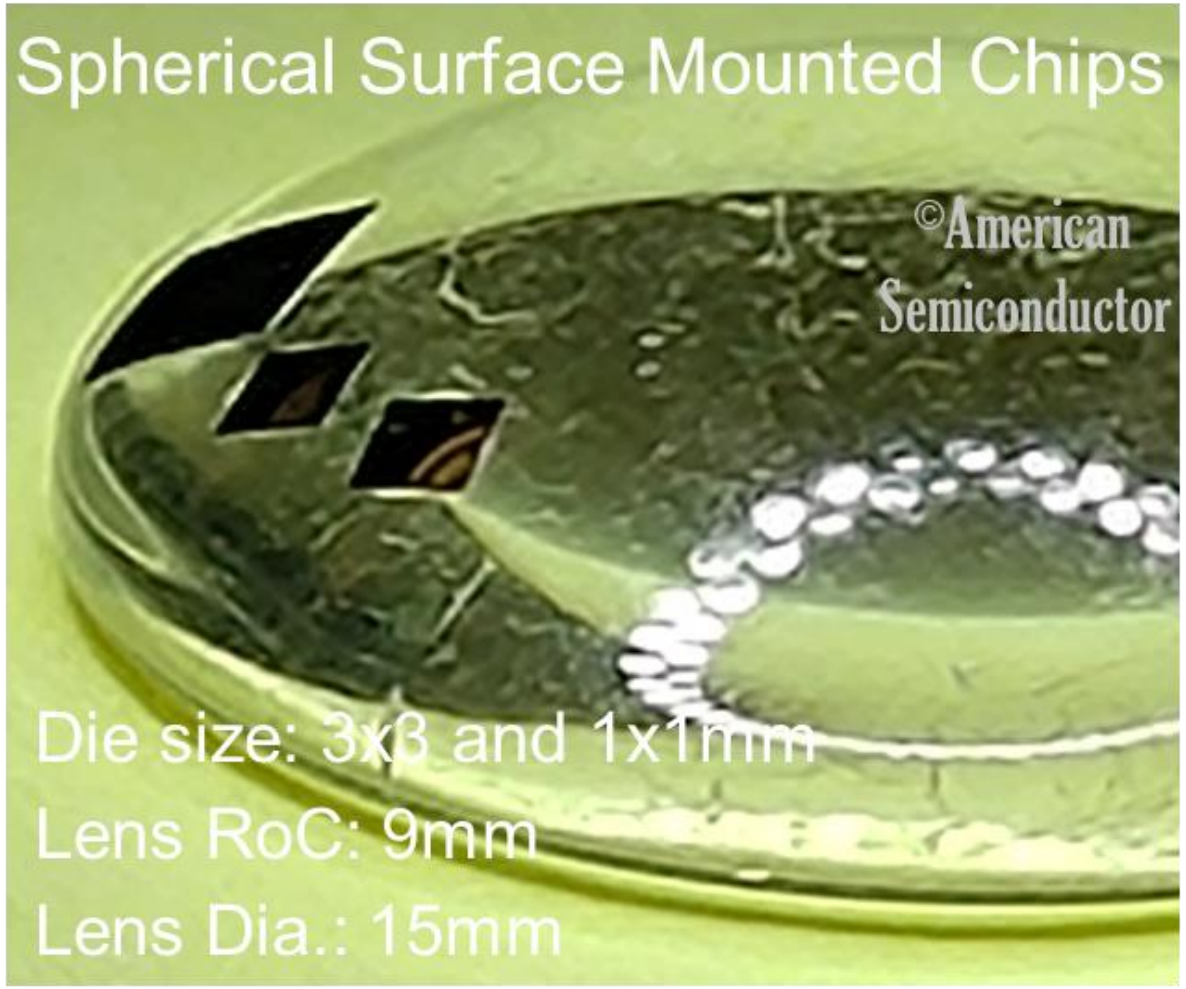
	Process	DBG	P-WLCSP FeX-C				
	Device	Bare Die	IDM-A	IDM-B	Test Die	Fabless A	Fabless A
	Sidewall	Blade	Blade	Blade	Laser	Laser	Blade
	Dimensions	~2x2	~2.5x2.5	~3.8x3.8	~1x1	~1x1.5	~1x1.5
	Si Thickness	100 um	15 um	15 um	12 um	12 um	12 um
RoC	Bend Orientation						
20mm	Perp	P	P	P	P	P	P
	Orth	P	P	P	P	P	P
15mm	Perp	P	P	P	P	P	P
	Orth	X	P	P	P	P	P
12mm	Perp	X	P	P	P	P	P
	Orth	X	P	P	P	P	P
10mm	Perp	X	P	P	P	P	P
	Orth	X	P	P	P	P	P
8mm	Perp	X	X	P	X	X	P
	Orth	X	P	P	X	X	P
7mm	Perp	X	X	x	X	X	P
	Orth	X	P	P	X	X	P
6mm	Perp	X	X	X	X	X	P
	Orth	X	P	P	X	X	X
5mm	Perp	X	X	X	X	X	P
	Orth	X	X	X	X	X	X

	Process	DBG Thin Die					SoP-TM			SoP-TM		
	Device	Bare Silicon - Test Die					Blank Si - Test Die			AS_OPA4505P.fxd		
	Sidewall	Blade					Etch			Etch		
	Size (mm)	5					2			1.5		
	Si Thickness	100 um					12 um			10 um		
RoC	Tag ID / Bend Orientation	8A	8B	8C	8D	8E	7A	7B	7C	W3-C1	W3-C2	W3-C3
20mm	Perp	P	P	P	P	P	P	P	P			
	Orth	X	P	P	X	P	P	P	P			
15mm	Perp	X	X	P	X	X	P	P	P			
	Orth	X	X	P	X	X	P	P	P			
12mm	Perp	X	X	P	X	X	P	P	P			
	Orth	X	X	X	X	X	P	P	P			
10mm	Perp	X	X	X	X	X	P	P	P			
	Orth	X	X	X	X	X	P	P	P			
8mm	Perp	X	X	X	X	X	P	P	P			
	Orth	X	X	X	X	X	P	P	P			
7mm	Perp	X	X	X	X	X	P	P	P			
	Orth	X	X	X	X	X	P	P	P			
6mm	Perp	X	X	X	X	X	P	P	P			
	Orth	X	X	X	X	X	P	P	P			
5mm	Perp	X	X	X	X	X	P	P	P	P	P	P
	Orth	X	X	X	X	X	P	P	P	P	P	P

Innovation - SoP polymerized IC packaging capability that enables hemispherical die assembly

New IC Capability for Ocular Applications

- Hemispherical IC applications
- Package capability applicable to any semiconductor IC
- Polymerization on all 6-sides
- 2 axis bend capability
- Die radius of curvature (RoC) demonstrated to <5mm
- Hemispherical RoC demonstrated for ocular applications at <9mm



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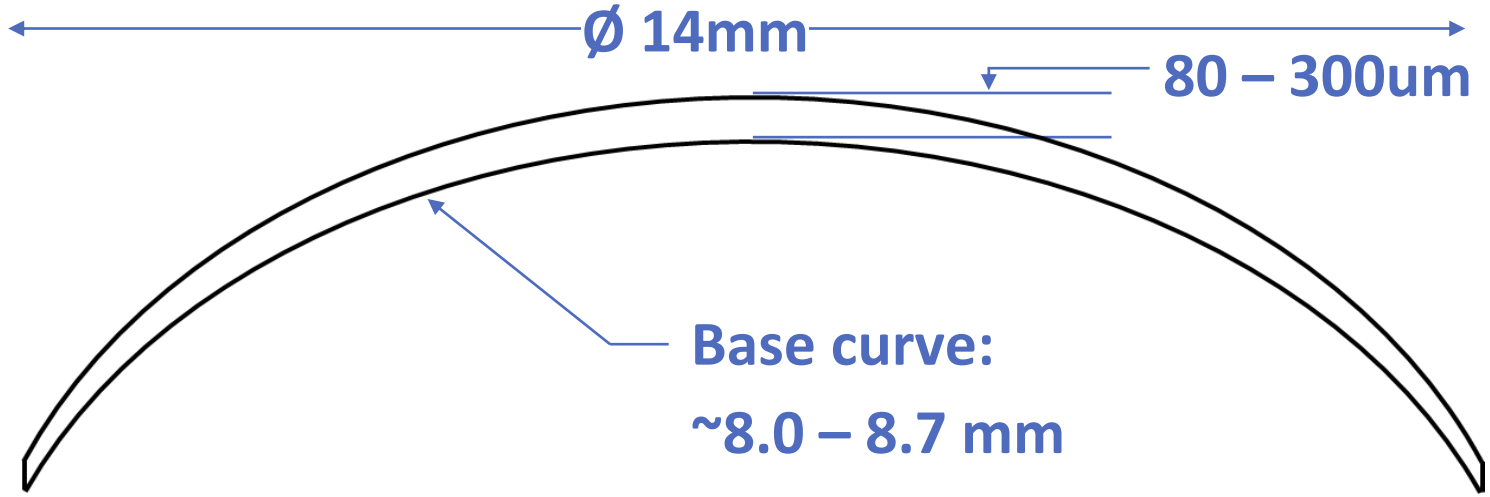
Contact Lens Form-factor

Smart Contact Chips Must:

- Fit in the lens
- Be Bio-compatible
- Bend
- Be Cost Feasible

Applications for Med-Tech physical format requirements are driving Chip-on-Flex assembly requirements



Source: Verily Life Science 2022

Advanced Medical Devices rely on advanced packaging and assembly

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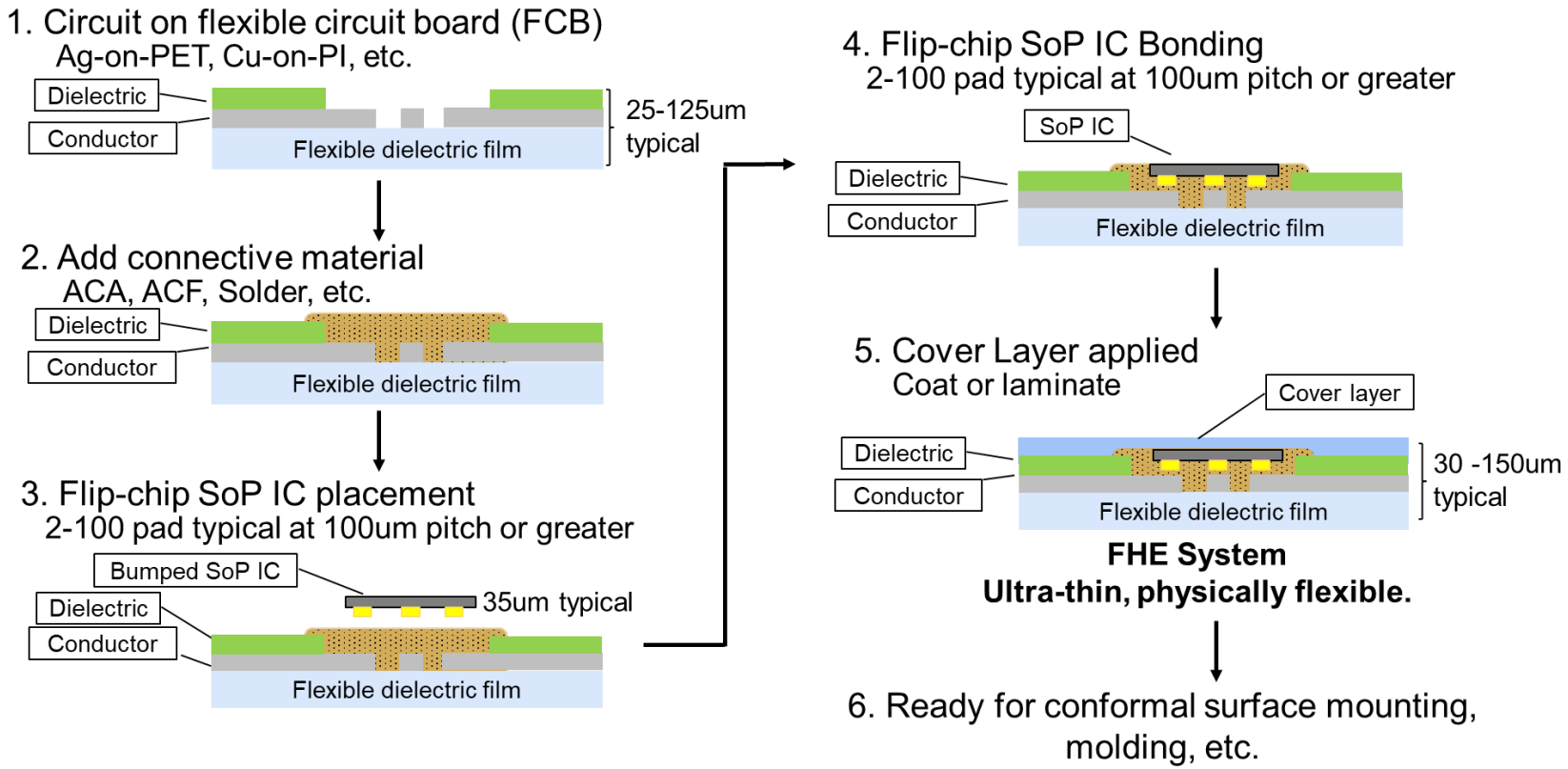
Fine Feature Flexible Flip-chip Assembly

SoP flip-chip and SMT COF

- Direct Interconnect is used to simultaneously complete die attach and die interconnect
- ACA eliminates the need for underfill
- ACA flip-chip is compatible with standard SMT processing
  - Low-temp solder process
  - Capability down to 01005
- 5mm RoC typical

Chip-on-Flex (COF) Advanced flip-chip assembly



Early Adopters: ***Smart Contact, Implanted Sensor, Implanted Wireless, and Catheter Applications***

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SoP and COF FHS Reliability

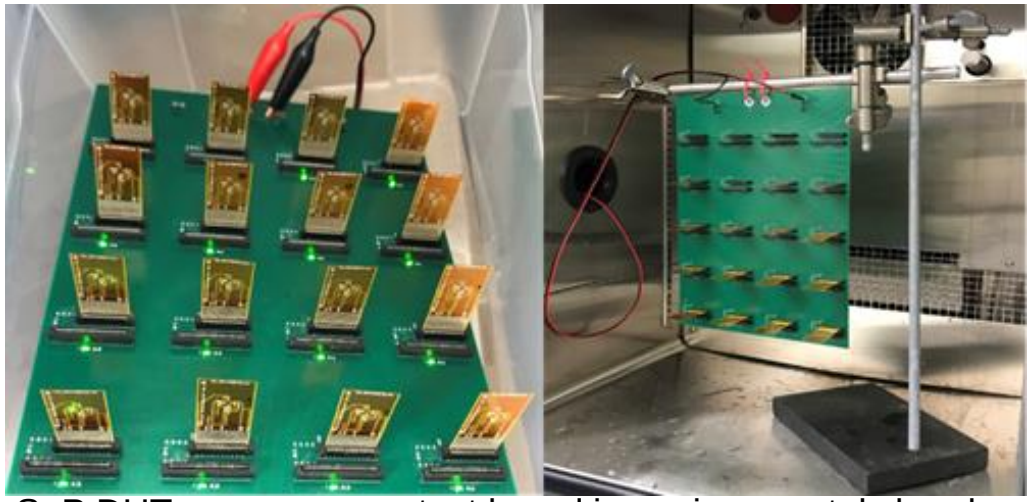
SoP-TM P-WLCSP ADA4505-1

Low Temperature Test (LTOL):
- 168 hours @ -25C, 1atm, n/a RH
- 2.5mV DC bias between VDD and VSS

Low Humidity Test (THB):
- 168 hours @ STP (22C/1atm), <10%RH
- 2.5mV DC bias between VDD and VSS

High Temperature Test (HTOL):
- 168 hours @ 125C, 1atm, n/a RH
- 2.5mV DC bias between VDD and VSS

High Humidity Test (THB):
- 168 hours @ STP (22C/1atm), 90%RH
- 2.5mV DC bias between VDD and VSS



SoP DUT on coupon on test board in environmental chamber

Data Collection: pre and post exposure, with midpoint

- Mid-point: 84 hours functional verification of 30mV p-p Gain
  - ✓ All coupons passed functionality test with 1 coupon showing increased gain.
- Final: 168 hours with full electrical characterization.
  - ✓ No test showed any consistent shift in data compared to post-assembly.
  - ✓ 2 coupons failed, failure mode indicating handling damage

Result: No significant impact from environmental exposer on electrical performance of SoP ADA4505.

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THB/TC Deformation Testing in Harsh Environments

- **Dynamic Harsh Environmental FHE Reliability Testing (DHERT)** semi | FlexTech | ARL
- Program builds on ASI flexible testing

Test	Conditions	ASI Procedure	References
High Temp Life	125°C	ASI TEST008	ISO 10373-1; JESD22-A108
Low Temp Life	-25°C	ASI TEST009	JESD22-A108
ESD	HBM and/or CDM	ASI TEST010	ANSI-ESDA-JEDEC_JS-001 & JS-002
Static Radius of Curvature	Concave/Convex Bend	ASI TEST003	ASTM D522-93a; ISO 10373-1; ISO 7816
Dynamic Radius of Curvature	Concave/Convex Bend	ASI TEST005	ASTM D522-93a; ISO 10373-1; ISO 7816
Axial Torsion	Twist Test	ASI TEST006	ISO 10373-1; ISO 7816
SEM Inspection	Post SoP Conversion	ASI TEST007	MIL-STD-883: M2018
Data Retention	150°C, non-biased	ASI TEST009	JESD22-A117; JESD-A103

- DHERT will provide dynamic bend, twist and stretch in harsh THB environment with in situ electrical testing
  - -70 to 190 C
  - 10 to 98% RH
- Equipment development in progress, due for demonstration Q3, 2024
- DHERT technology developed under this program will be deployed by ASI as a commercial testing service

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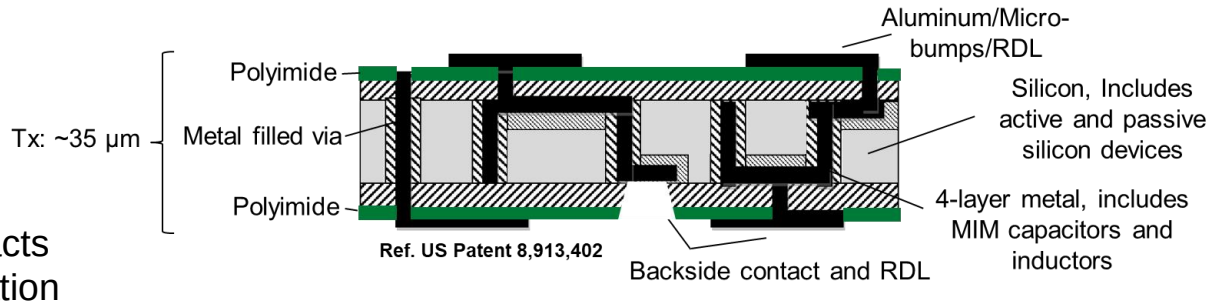
SoP Smart Silicon and Polymer Advanced Substrates

SoP Interconnects: Smart-Si and Fine Pitch FCB (Flexible Circuit Board) Substrates

Embedded Si

- ✓ 300mm process
- ✓ 4-Layer Metal (Al)
- ✓ 130nm Min. Feature
- ✓ With or without Si
- ✓ Front and Backside Contacts
- ✓ SoP – Polymer encapsulation
- ✓ Fully flexible



Nobleflex™ Fine Pitch FCB (Available for R&D)

- ✓ 200/300mm process
- ✓ 3 – Layer Metal (Au or Cu)
- ✓ 1um Min. Feature
- ✓ Front and Backside Contacts
- ✓ PI FCB
- ✓ Fully flexible
- ✓ May be integrated with Embedded Si

- FEOL fabricated as an integrated circuit itself using readily available foundry process
- BEOL fabricated in SoP for ultra-thin and flexible capability, and backside features
- Includes precision resistors, capacitors, inductors
- Capable of including flexible photonic silicon waveguides (US Patent 9,733,428)
- High Density Interconnections between stacked metal layers
- Precise dimension tolerances ease IC bonding and connection
- Semiconductor materials match CTE of silicon ICs
- High density interconnections on both top and bottom surfaces

Summary and Next Steps

Summary:

- SoP-TM P-WLCSP is being adopted for new medical device applications
- Ultra-thin and Flexible capability enables new healthcare advancements
- COF Advanced Assembly required for new flex systems
- Reliability is paramount to new applications
- Continued evolution requires advancements in polymer and silicon substra
- Methods and standards for reliability determination are in development

Next Steps

- Transition from clinical to production volumes
- More Reliability Testing
- Demonstration of advanced substrates for med-tech
- Expand U.S. Capacity for a secure healthcare supply chain

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American Semiconductor - Boise, ID

Member:

ASTN
NSF
Engine

Packaging, Assembly, Test and Related Services

MASIP LLC- Phoenix, AZ

MASIP LLC holistic approaches to products/markets

- Market and materials/process trends (IC pkg focus)
- Manufacturing optimization (FA and rel assessments)
- Material and process development & implementation
- Specific application materials and process assessment

Wide experience:

- Electronics-FAB, packaging and assembly
  - early publications and patents for FI & FO (RCP)
- **Material and development**
  - Implemented 1st 2 PSPSI materials at Motorola
  - IP on materials/processes for WSS/flux/AM
- **Material/interface experience and Rel modeling**
  - Solving failure mechanisms (surface/interfaces)
  - Appling material principles to key areas
    - Reliability modeling, Processing, Materials
- **Optimization of plastic package for high reliability**
  - Materials, processes, interfaces

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Thank You

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