Heterogeneous Packaging Technologies for Chiplet and Memory Integration

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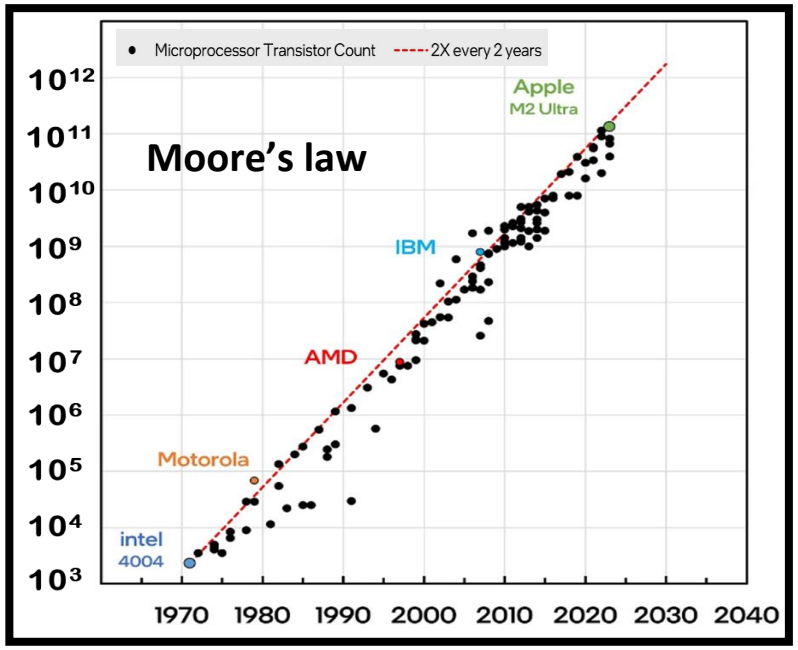
Outline

- Introduction
- Chiplet based heterogeneous integration platform
- Innovative memory integration solutions
- Novel Integrated Stack Capacitors (ISC) integration
- Conclusion

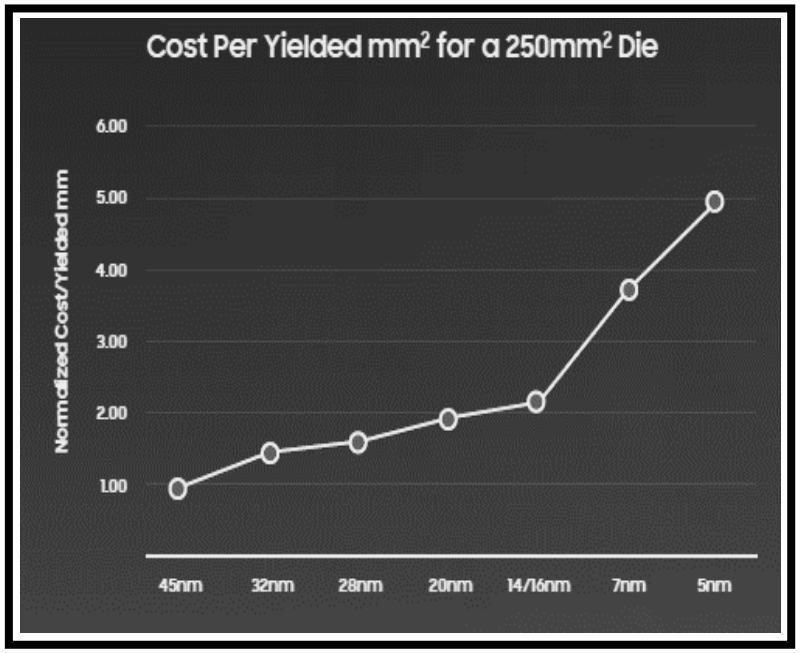
Introduction

Advanced Packaging techniques are utilized to meet the market needs



Moore's law predicts the exponential growth of ICs since 1970s---***Market needs***

https://semiconductor.substack.com/p/the-relentless-pursuit-of-moores



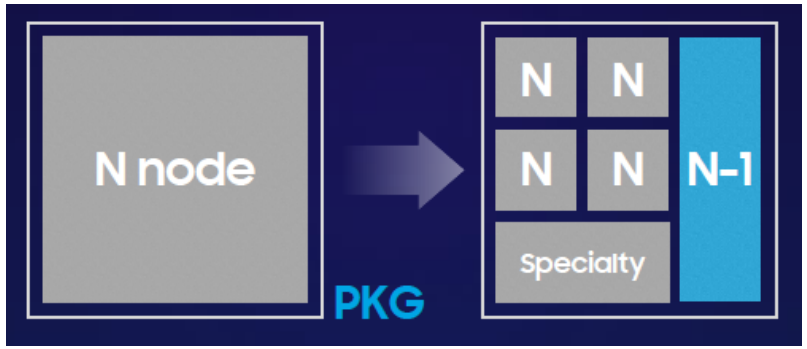
The exponential growth of cost per Yielded mm^2 for 250 mm^2 die ----***Challenges for Si level scaling and yielding***

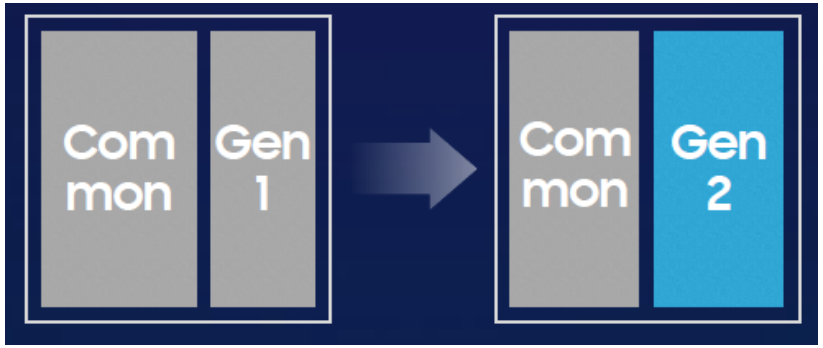
Why Advanced Packaging?

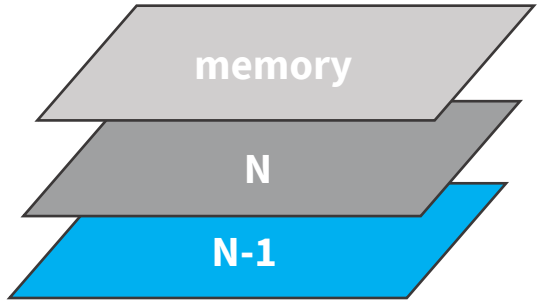
- **Chiplet**
- **Heterogeneous integration**
- **Die stacking**

Introduction

Chiplet; Heterogenous integration; die stacking







High yielding smaller chips and optimal process selection

Modular design, design reuse and mix & match

Die stacking footprint reduction

M. Kang, "Heterogeneous Integration Platform for Next Generation Computing" Sixth Annual Symposium on Heterogeneous Integration, February, 2023.

Introduction

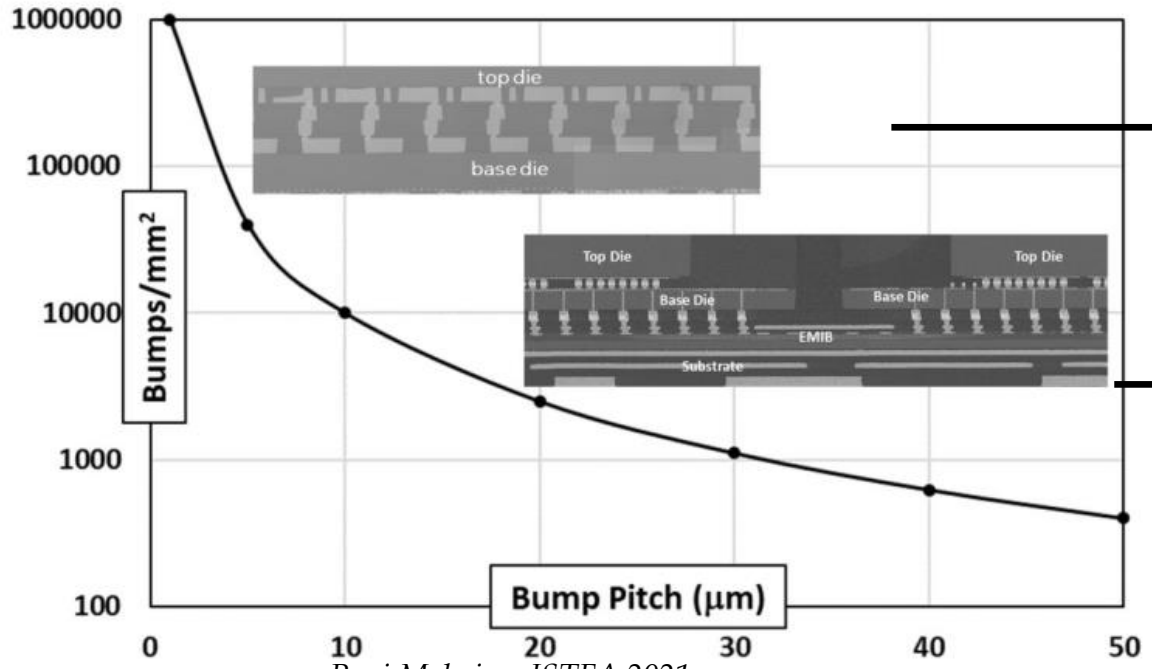
Technical and Logistic Challenges

- **Multi-domain co-design** involving both **power** and **signal** routing
- **Thermal management**
- **Facilitate Industry open platforms and standardizations** for high-speed and low power chiplet D2D communications: Universal Chiplet Interconnect Express (UCIe), Bunch of Wires (BoW), and High Bandwidth Interconnect (HBI) etc.
- **Establish and Clarify Agreements** on Si security and responsibilities in yield, Known Good Die (KGD), product or chiplet quality and reliability.

Y. Li, J. Yang, K. Chatterjee, P. Asrar, S. Jeong, and W. Kim, “Advanced package technologies for chiplet adoption and memory integration in HPC/AI applications”, OCP global summit, Future Technologies symposium, October 18, 2023, San Jose.

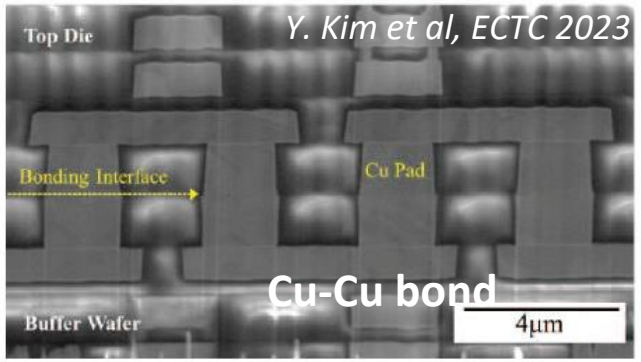
Introduction

Technical and Logistic Challenges

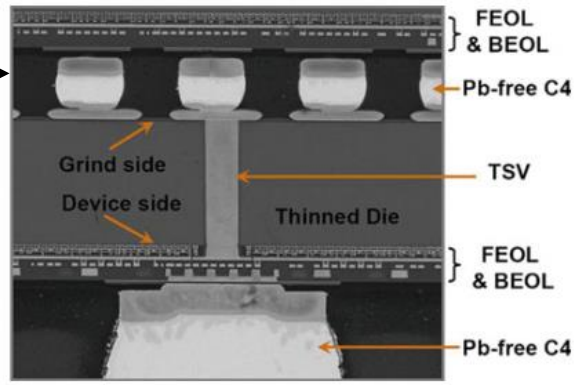


Ravi Mahajan, ISTFA 2021

Hybrid Cu Bonding (HCB)



Thermal Compressive Bonding (TCB)



Solder based

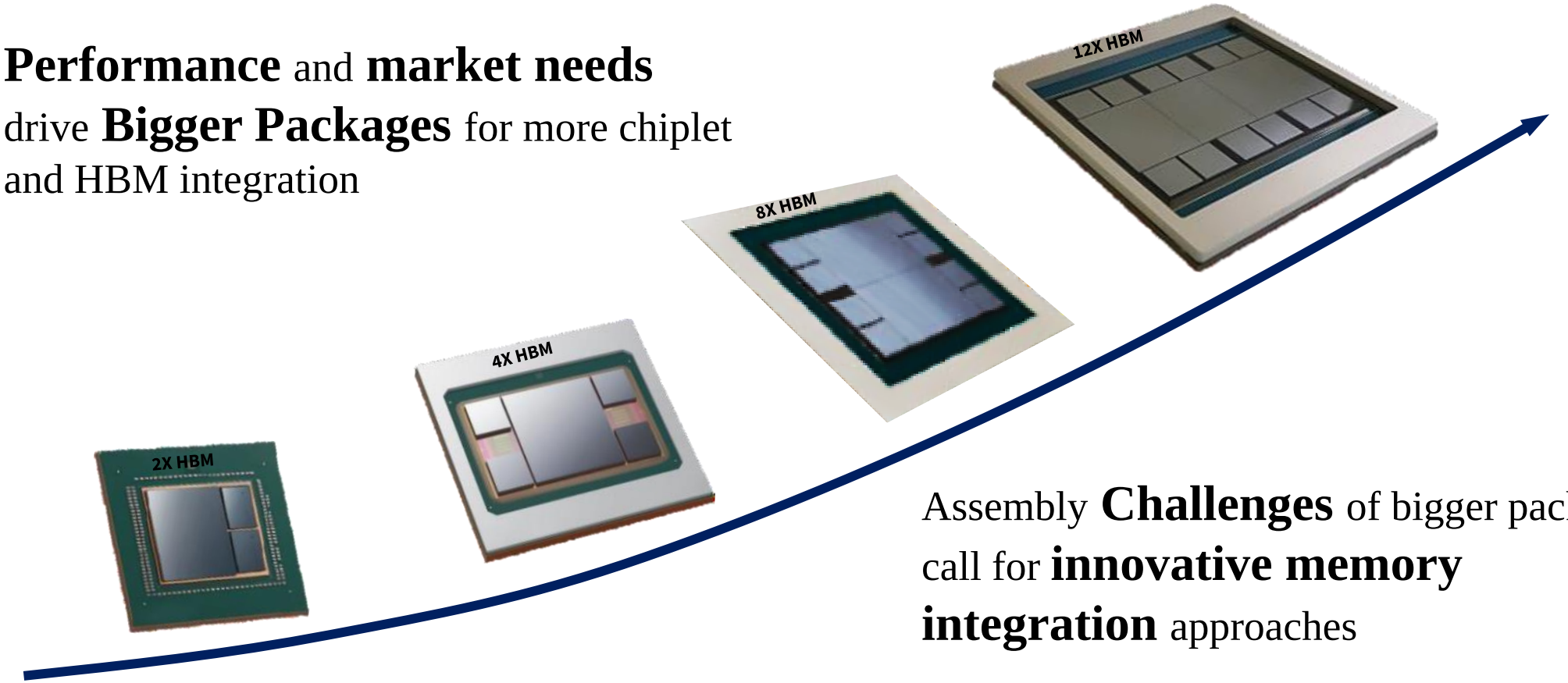
- **D2D interconnect scaling down: HCB replacing TCB**
  - **Tighter bump pitch; smaller bumps**
  - **Gapless –thermal advantages**

3D Microelectronic Packaging: From Architectures to Applications, 2nd edition, Springer, 2021, ISSN 1437-0387

Introduction

Technical and Logistic Challenges

Performance and **market needs** drive **Bigger Packages** for more chiplet and HBM integration

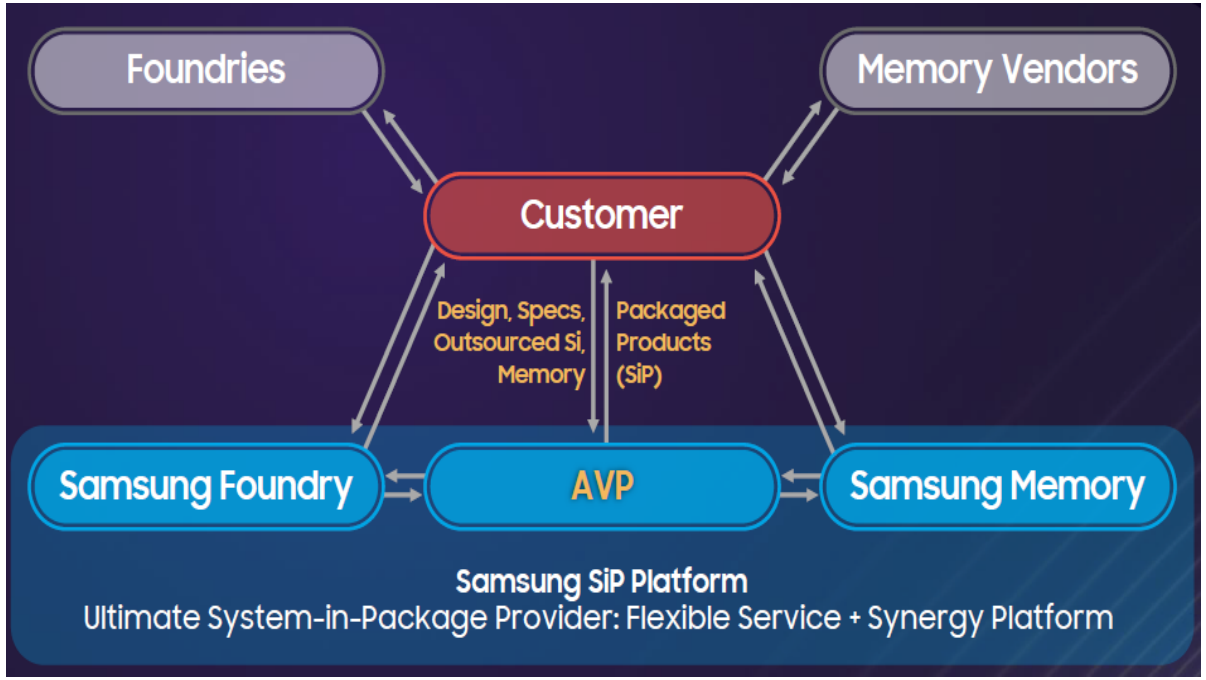


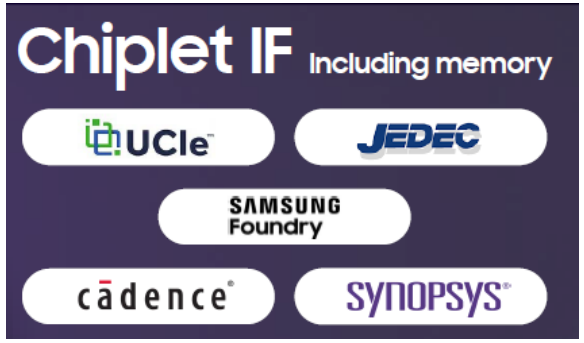
Assembly **Challenges** of bigger packages call for **innovative memory integration** approaches

Y. Li, J. Yang, K. Chatterjee, P. Asrar, S. Jeong, and W. Kim, "Advanced package technologies for chiplet adoption and memory integration in HPC/AI applications", OCP global summit, Future Technologies symposium, October 18, 2023, San Jose.

Chiplet Based Heterogeneous Integration Platform

End to End, Flexible, Synergy, Eco system





M. Kang, “Heterogeneous Integration Platform for Next Generation Computing” Sixth Annual Symposium on Heterogeneous Integration, February, 2023.

Chiplet Based Heterogeneous Integration Platform

Type	Current offering	Roadmap	Pictures
FOPLP	RDL L/S: 5µm;Bump pitch: 90µm; Pkg. thickness: 0.58mm	RDL L/S: 5µm;Bump pitch: 90µm; Pkg. thickness: 0.58mm	
FOWLP	RDL L/S: 2µm;Bump pitch: 90µm; Pkg. thickness: 0.35mm	RDL L/S: 1um; Bump pitch: ≤75um; Pkg. thickness: 0.33mm	
I-Cube S	Interposer size: 3x reticle; # of HBM: 8x; µbump pitch: 40µm; Interposer C4 pitch: 150µm; Package size: 85×85mm²	Interposer size: 4+ reticle; # of HBM: 12x; µbump pitch: 25µm; Interposer C4 pitch: 125µm; Package size: 100×100mm²	

Type	Current offering	Roadmap	Pictures
I-Cube E	Interposer size: 3x reticle; # of HBM: 8x; µbump pitch: 40µm; Interposer C4 pitch: 150µm; Package size: 85×85mm²	Interposer size: 4+ reticle; # of HBM: 12x; µbump pitch: 25µm; Interposer C4 pitch: 125µm; Package size: 100×100mm²	
X-Cube (TCB)	Bump pith: 25µm; Silicon thickness: 40µm	Bump pitch: ≤21µm; Silicon thickness: <40µm	
X-Cube (HCB)	Bump pitch: 4µm; Silicon thickness: 10µm	Bump pitch: ≤3µm; Silicon thickness: <10µm	

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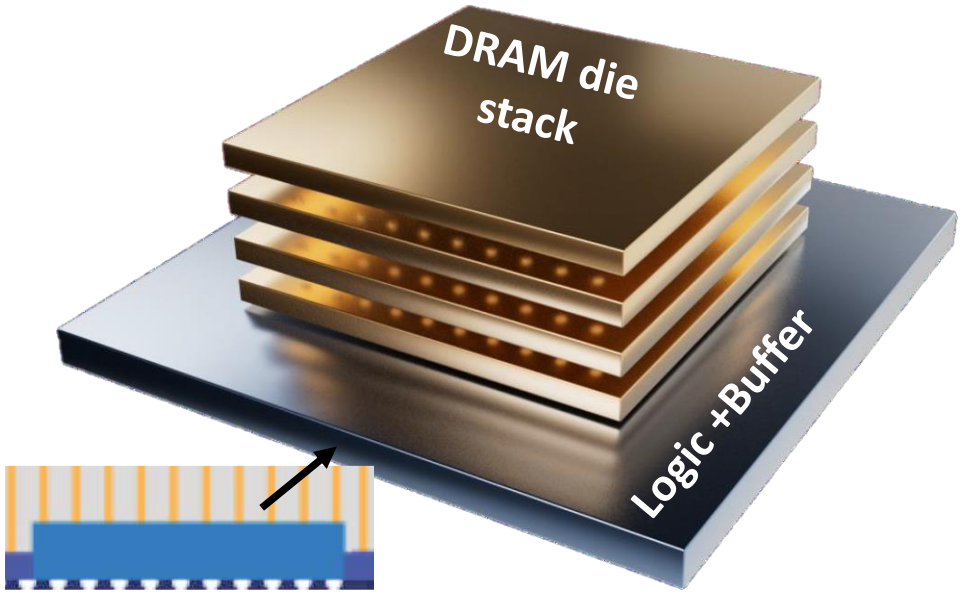
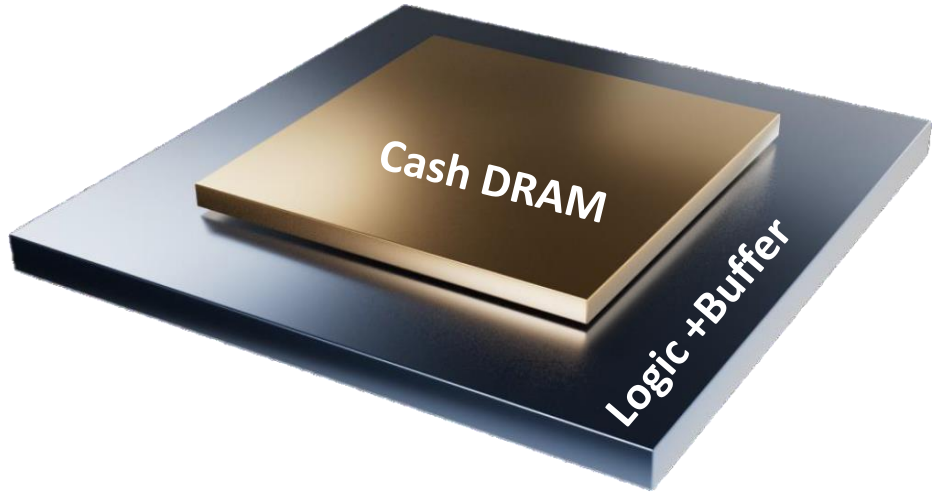
Innovative Memory Integration Solutions

3D Memory Integration



3D custom HBM

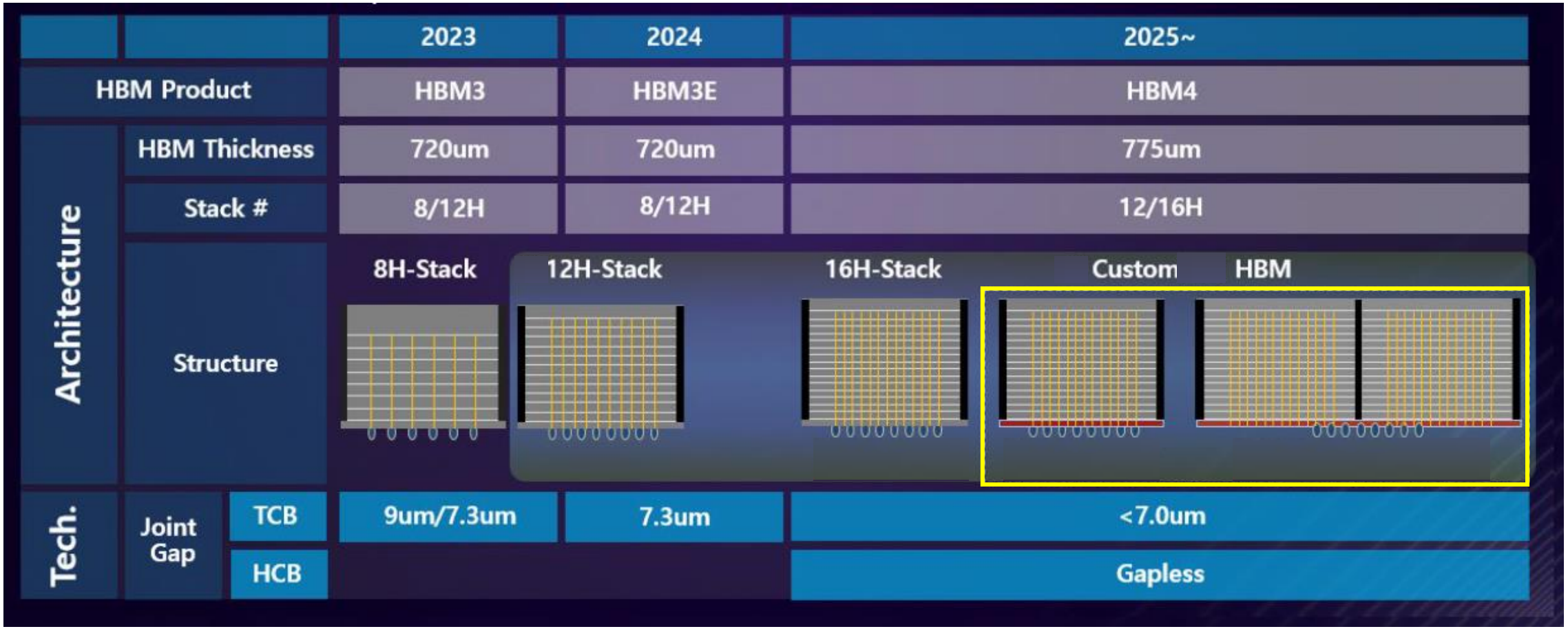


3D Cash Memory

Y. Li, J. Yang, K. Chatterjee, P. Asrar, S. Jeong, and W. Kim, “Advanced package technologies for chiplet adoption and memory integration in HPC/AI applications”, OCP global summit, Future Technologies symposium, October 18, 2023, San Jose.

Innovative Memory Integration Solutions

3D Custom HBM



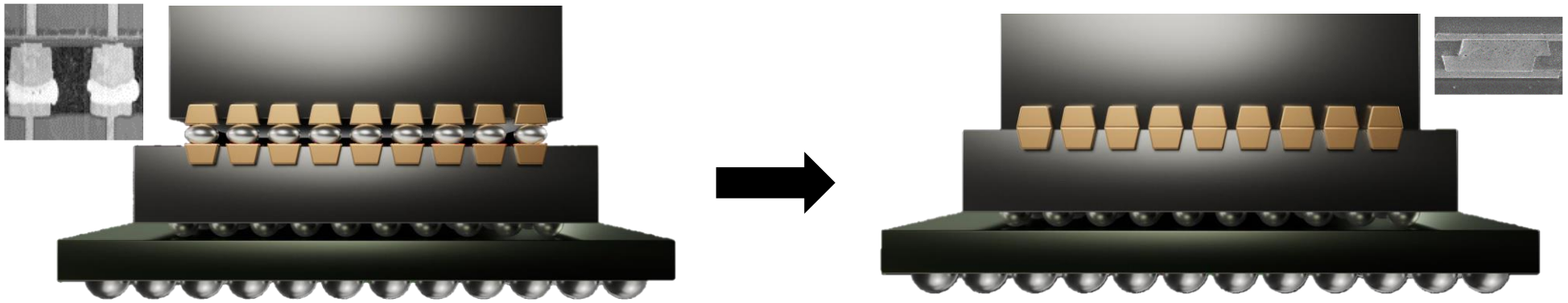
W. Kim, "Advanced Packaging in the Era of HPC and AI" Seventh Annual Symposium on Heterogeneous Integration, February, 2024.

Innovative Memory Integration Solutions

HCB replacing TCB in 3D die stacking

Cu-Cu replacing solder based micro bumps

- ~ **× 100 denser** interconnects
- Up to **× 150 more bandwidth**
- Up to **30% more allowable power**



Solder based micro bump by TCB
>20μm in bump size and pitch

Cu-Cu by HCB
A few μm in bump size and pitch

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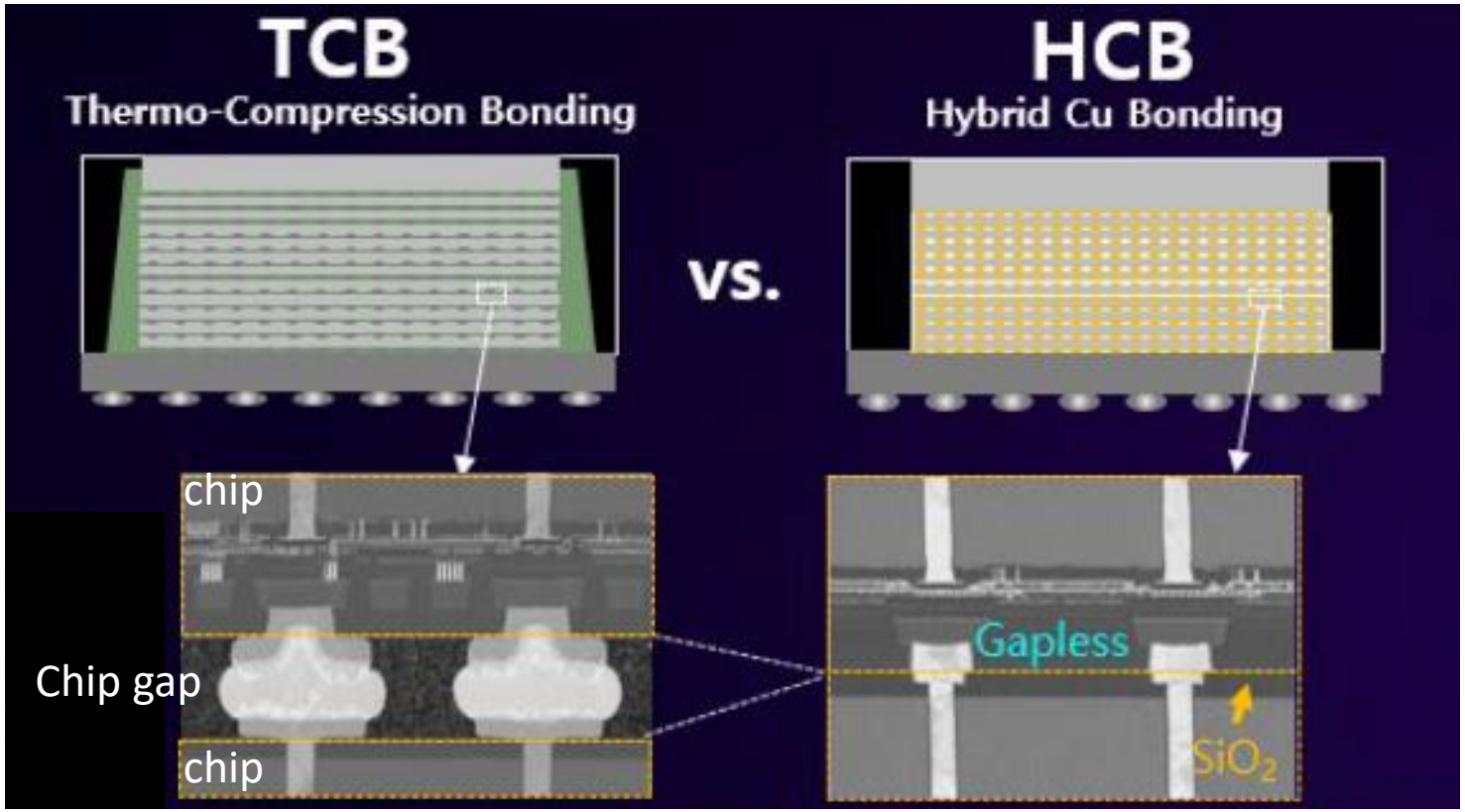
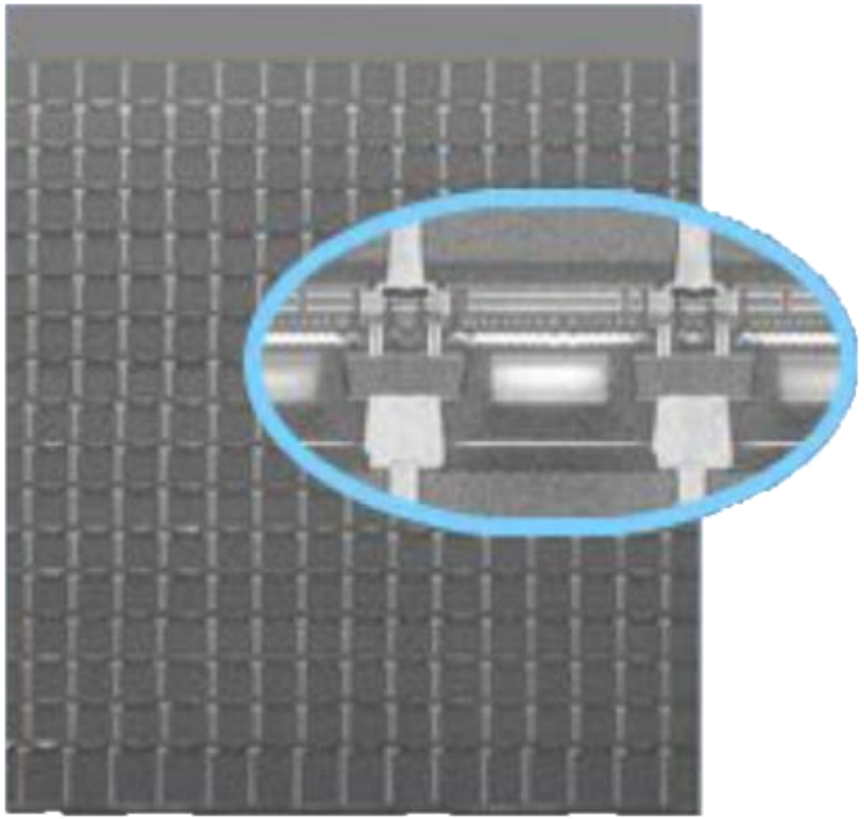
Innovative Memory Integration Solutions

HCB replacing TCB in HBM





16H HBM by HCB

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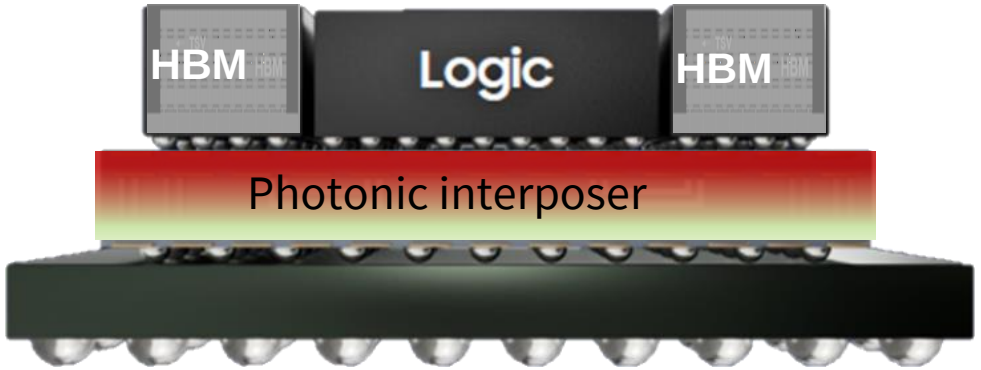
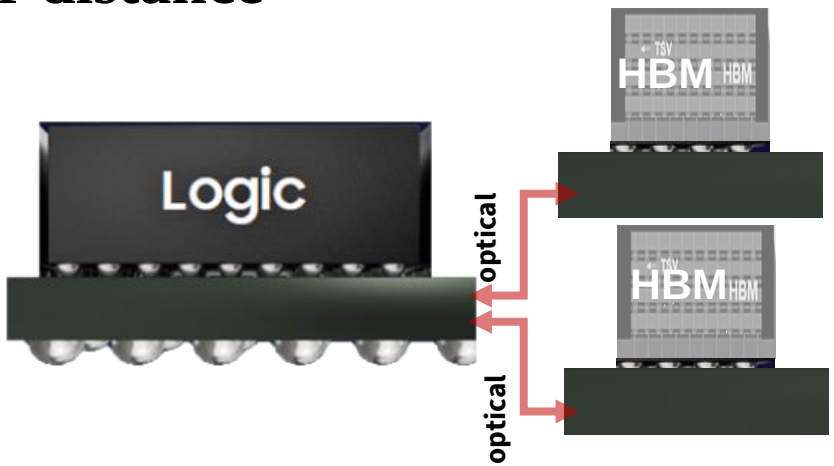
Innovative Memory Integration Solutions

Optical Interconnects could be a promising approach

- **Exceptionally high bandwidth densities**
- **Ultra low power consumption per bit or per distance**



Development trend: Optical interface between HBM and Logic



Development trend: Optical connection between logic and HBM packages

M. Tan, et al " Co-packaged optics (CPO): status, challenges, and solutions", Frontiers of Optoelectronics", 16:1, 2023

N. Pleros et al "Optical Interconnect and Memory Technologies for Next Generation Computing", 2016 18th International Conference on Transparent Optical Networks (ICTON), Trento, Italy, 2016, pp. 1-4, doi: 10.1109/ICTON.2016.7550267.

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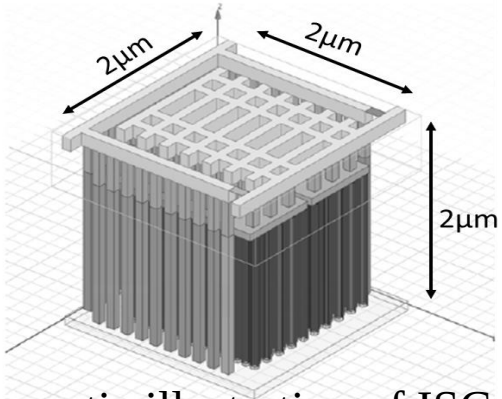
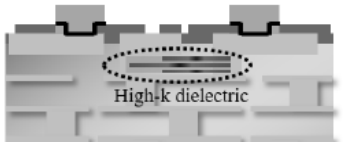
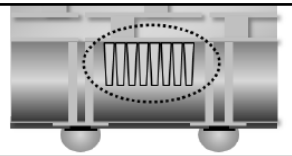
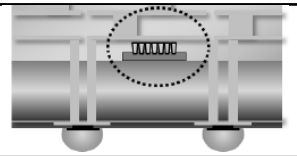
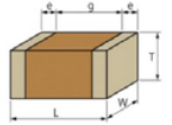
Novel Integrated Stack Capacitors (ISC) integration



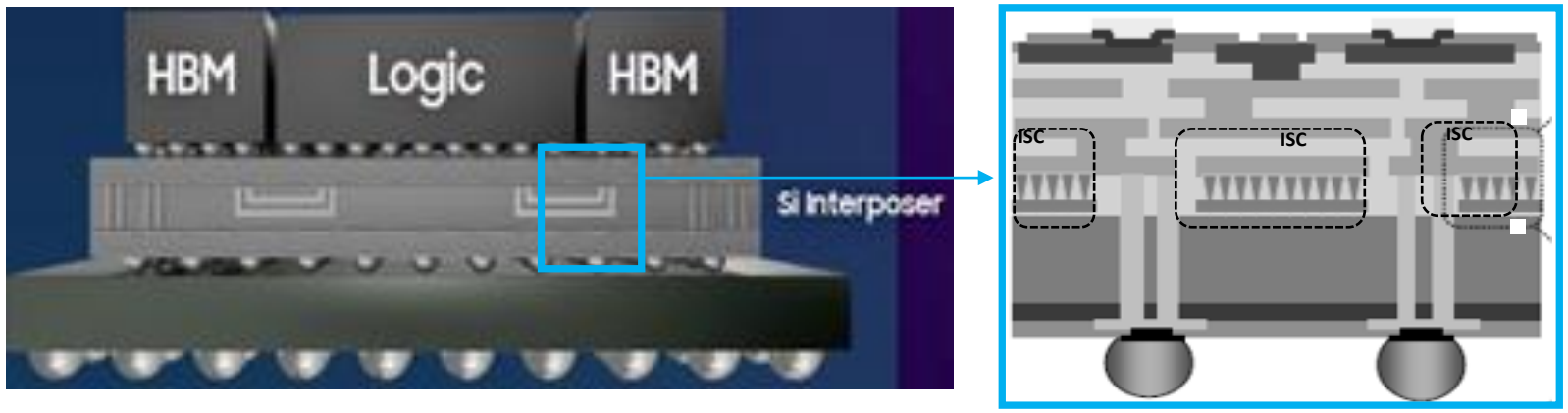
Schematic illustration of ISC with a silicon area of 2×2 µm²

- **High Power demands in HPC**
- **Low impedance Power Distribution Network (PDN)**
- **Capacitors with small form factors, high capacitance density, stable at high T.**

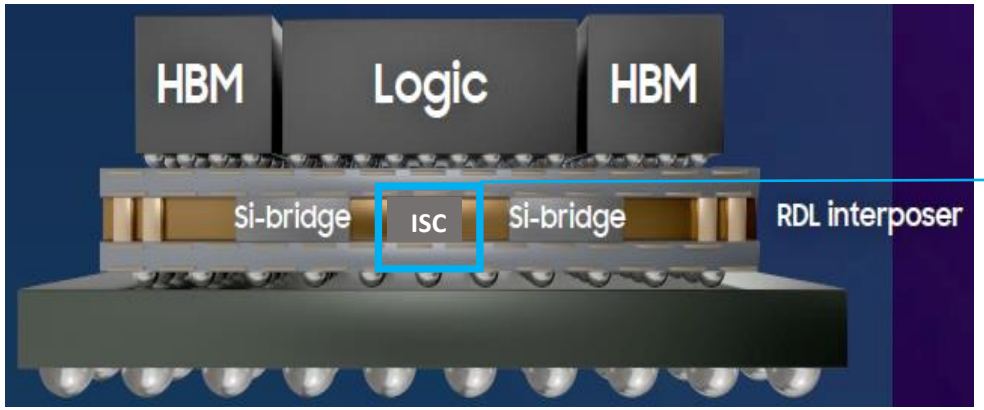
	Metal-Insulator-Metal (MIM)	Deep Trench Capacitor (DTC)	Integrated Stack Capacitors (ISC)	Multilayer Ceramic Capacitor (MLCC)
				
Cap. density	**× 1.0**	**× 7.5**	**× 7.5**	**× 75**
Cap. Height	**≤ 2µm**	**~ 30µm**	**~ 2µm**	**~ 1mm**
Cap. density change with T?	**No**	**No**	**No**	**Drop at high T**

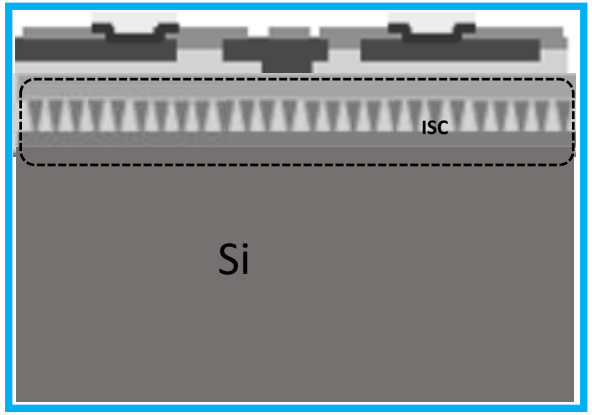
E. Song, D. et al, "Power Integrity performance Gain of a Novel Integrated Stack Capacitor (ISC) Solution for High-end Computing Applications", IEEE 70th Electronic Components and Technology Conference (ECTC), 2020, pp. 1358-1362.

Novel Integrated Stack Capacitors (ISC) integration



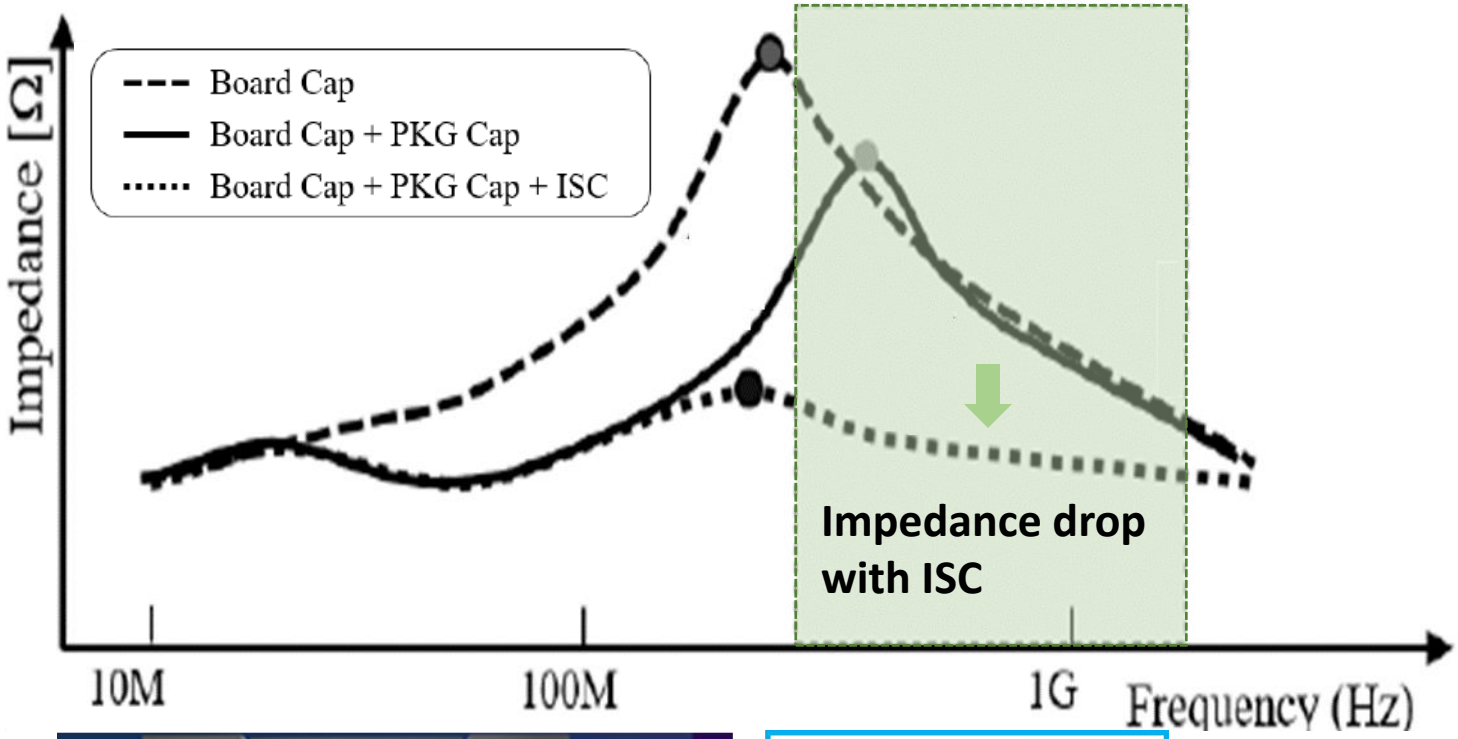
ISC is embedded between metal layers in a Si interposer





ISC die is embedded inside a RDL interposer along with the bridge dies

Novel Integrated Stack Capacitors (ISC) integration



Modeling showing significant impedance drop at high frequency range by adding ISC to Si interposer

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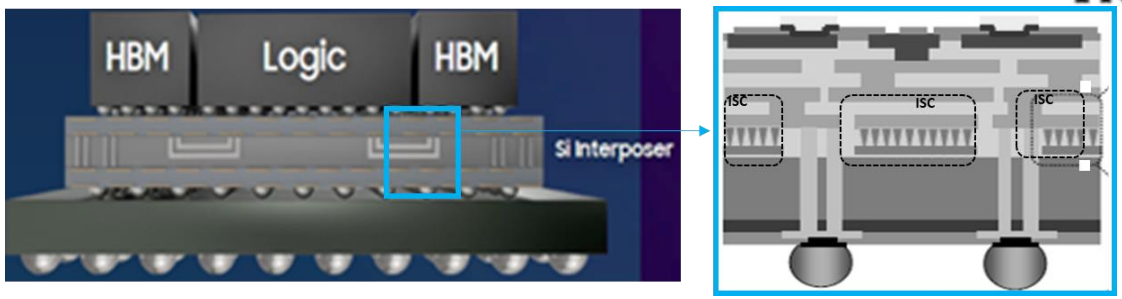

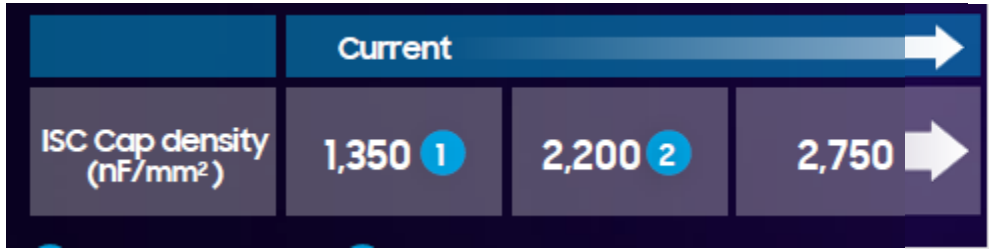

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Conclusion

- **The one-stop advanced package solution for HPC and AI applications**
- **Innovative memory integration solutions**
- **The novel adoptions of ISC into the chiplet based heterogeneous integration platform**