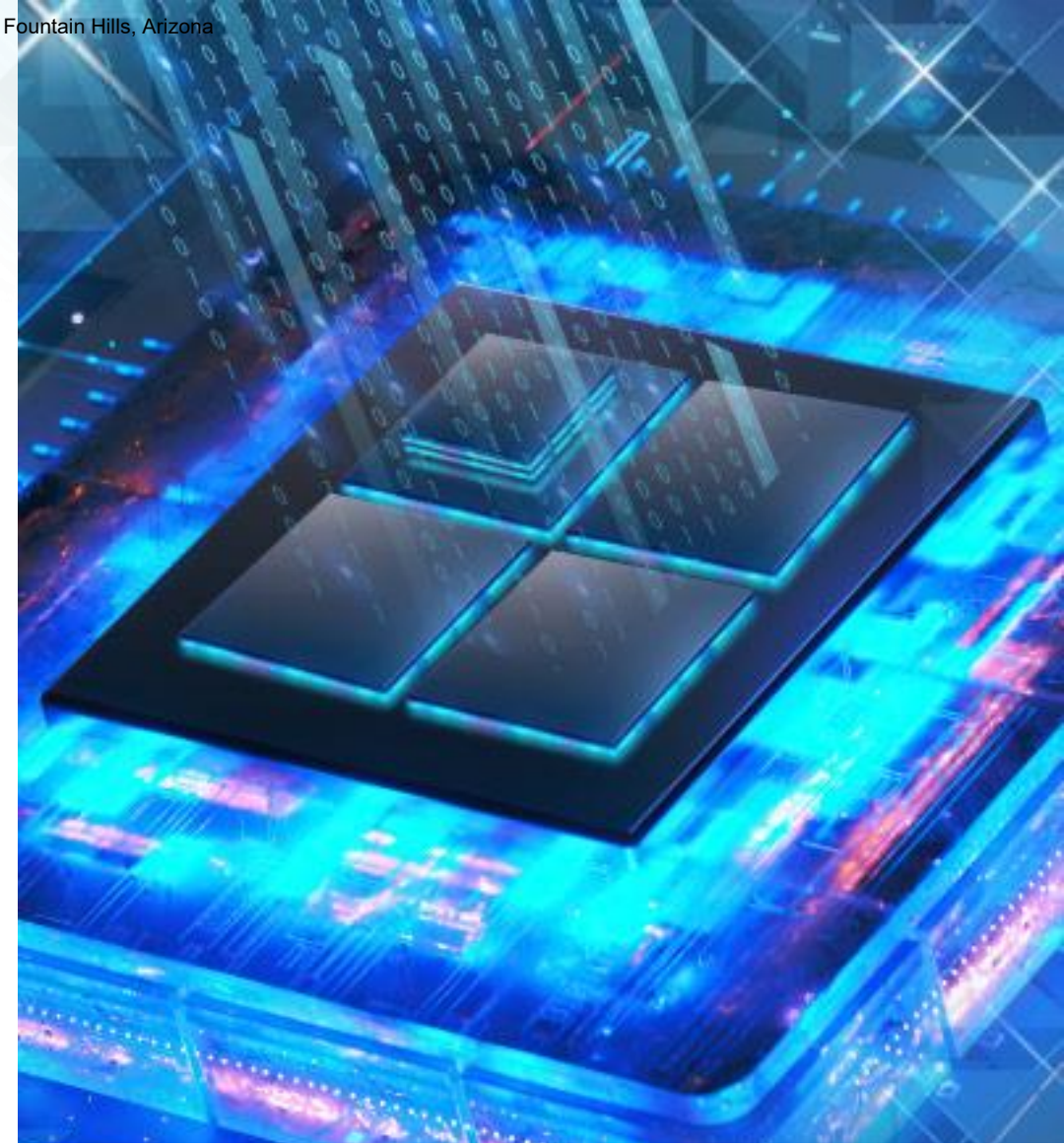
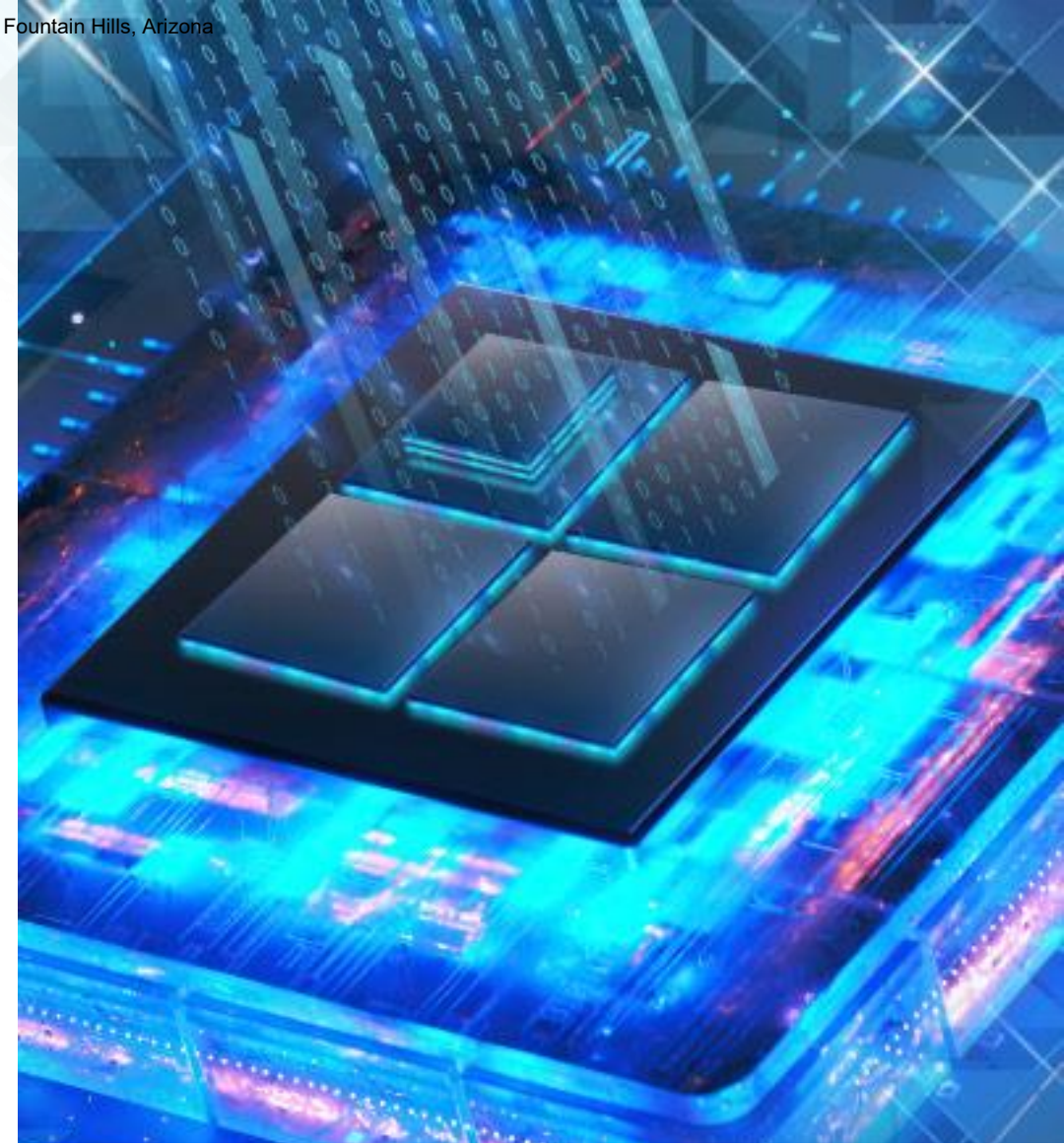
Amkor Technology®

ENABLING the FUTURE





# Building Blocks & Tradeoffs

Mike Kelly | VP, Chiplets & FCBGA Packaging
Dave Hiner | Sr. Director, Package Development
Suresh Jayaraman | Sr. Director, Package Development

# Overview

- Goal: Create critical thinking for the best way to achieve HI integration
- Show next level details that impart real experience and the ability to overcome



# Agenda

1. High Level Trends for Advanced IC Packaging
2. Chiplets Packaging: Getting Started
3. Module-based Products: 2.5D, HDFO, Bridges
4. PADK SmartPackage™ Design Environment



# Compute: Follow the Data

Connected Devices

Internet Gateways

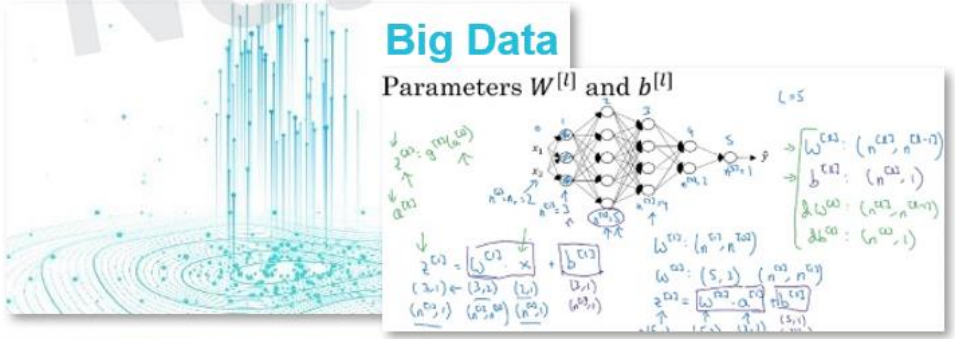
Edge IT

Data Centers

Huge Databases Created

Embedded Systems

Data Center: AI Teaching

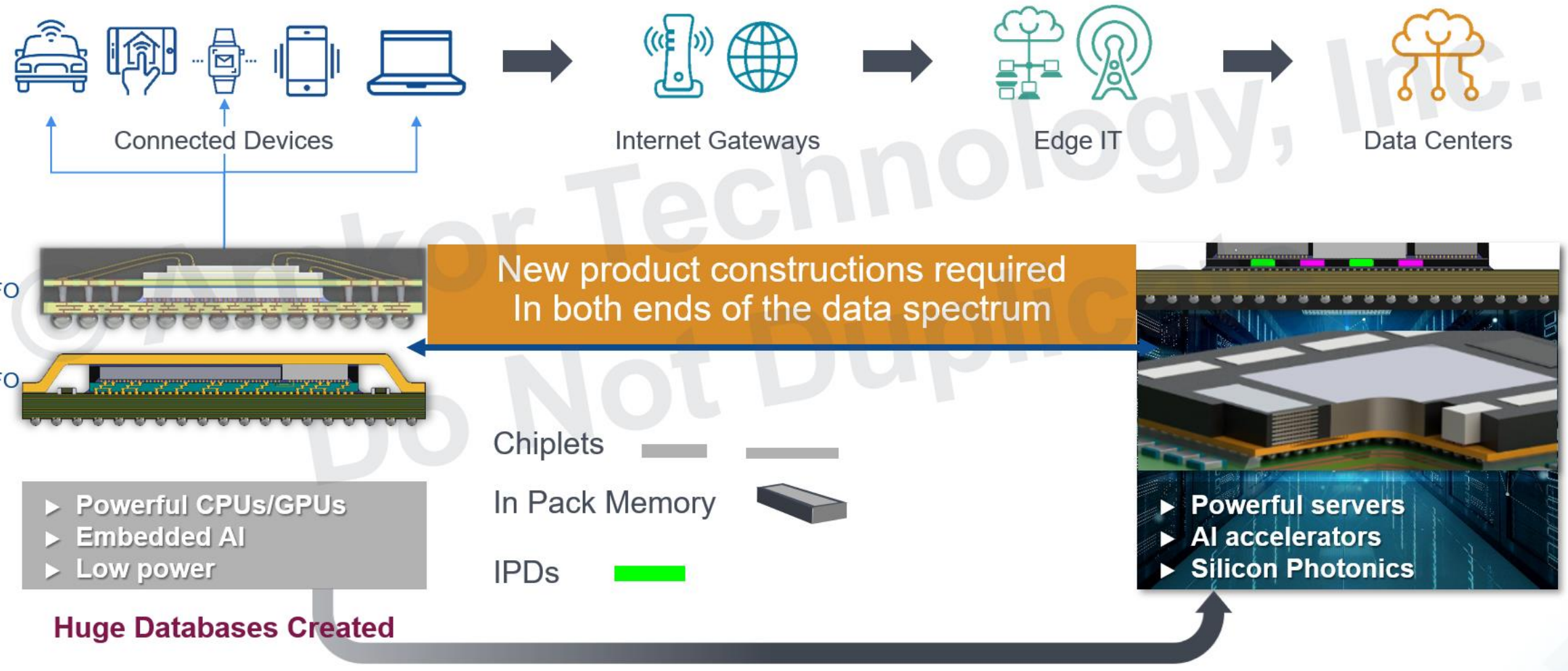






# Compute: Follow the Data







# Trends



# Compute Product Trends & IC Package Implications

| | |
|---|---|
| **Higher memory BW** | ▶ Memory co-located in package |
| **High wafer costs**<br>**Finer market targeting** | ▶ **Chiplets:** Create silicon die that can be reused |
| **More silicon content** | ▶ Larger package sizes, pushing **100 x 100 mm** |
| POWER<br>**More electrical**<br>**Power delivery** | ▶ More embedded passives |
| POWER<br>**Higher total power** | ▶ Improved thermal power dissipation solutions |

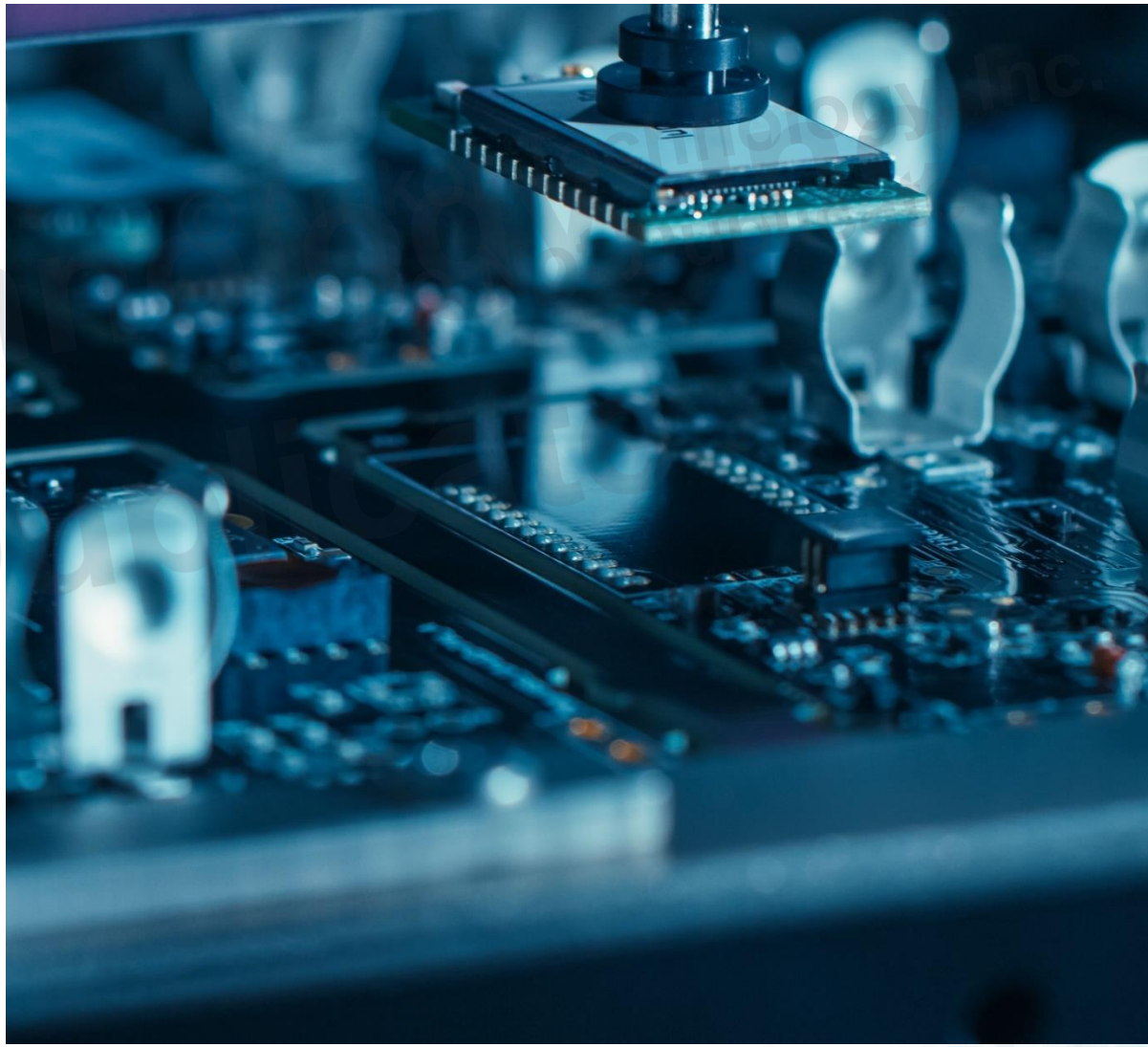




# Advanced Packaging: Major Advances

- Growing adoption of chiplet-based products for 2-D layouts
- Power Delivery Network (PDN) emphasis and creative use of deep trench capacitors (DTC)
- Higher power and use of metal-type TIM materials
- Use of larger package substrates
- Use of Cu-hybrid 3D stacking on the high end

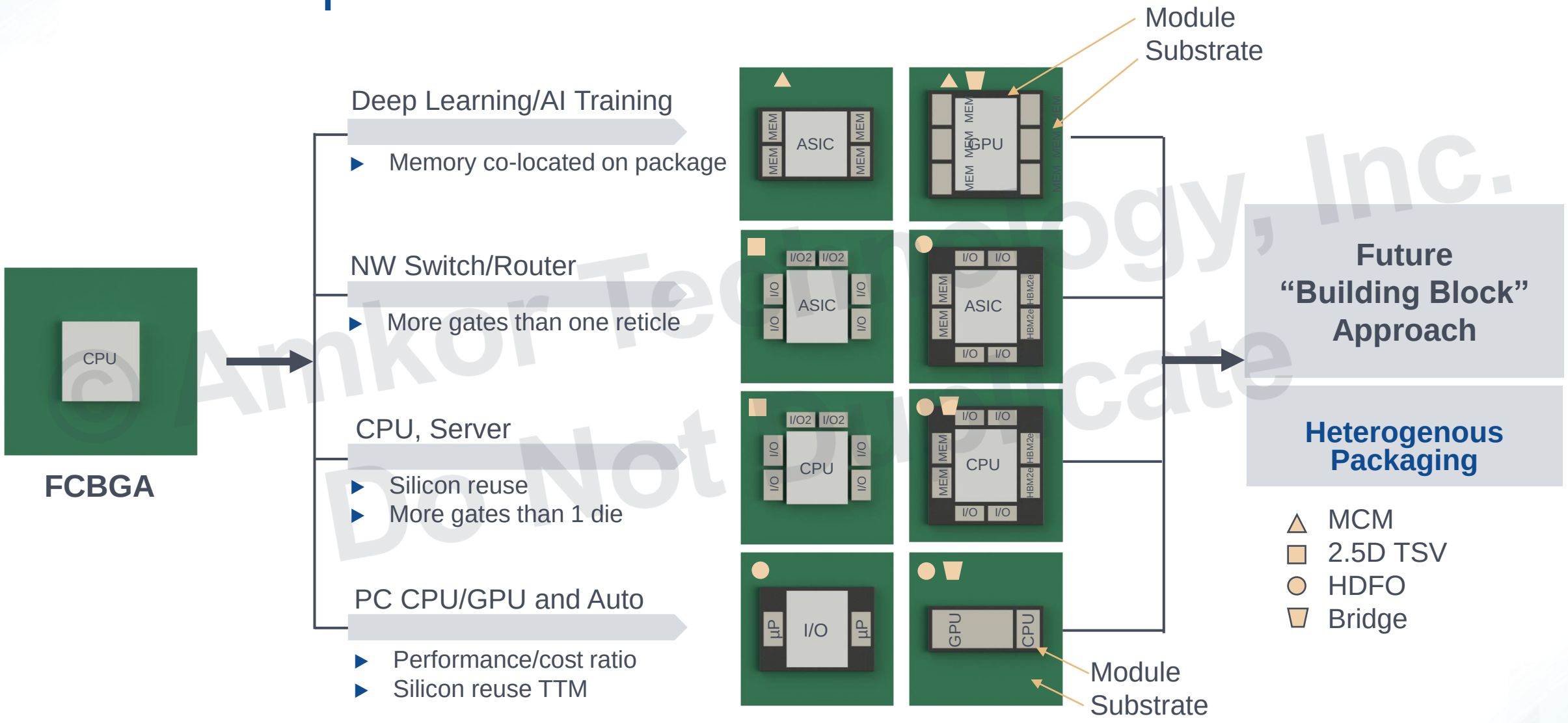






# Trends: Chiplets







# Solutions



# Package Construction Tradeoffs

## Die-to-Die Interface Requirements

- Total die-to-die BW
- Line speeds
- Latency
- Bump pitches
- L/S, layer count
- Dielectric layer

## Power Delivery Requirements

- V = L di/dt
- Power/current
- Bypass caps
- Capacitance
- Lower L construction
- Cap locations & value

## Module Size Substrate Requirements

- Number & size of die
- Module warpage
- Defect density = yield

## Power Dissipation Requirements

- Operating frequency
- Clocking strategies
- Power density
- Theta $J_c$

**Module Definition**

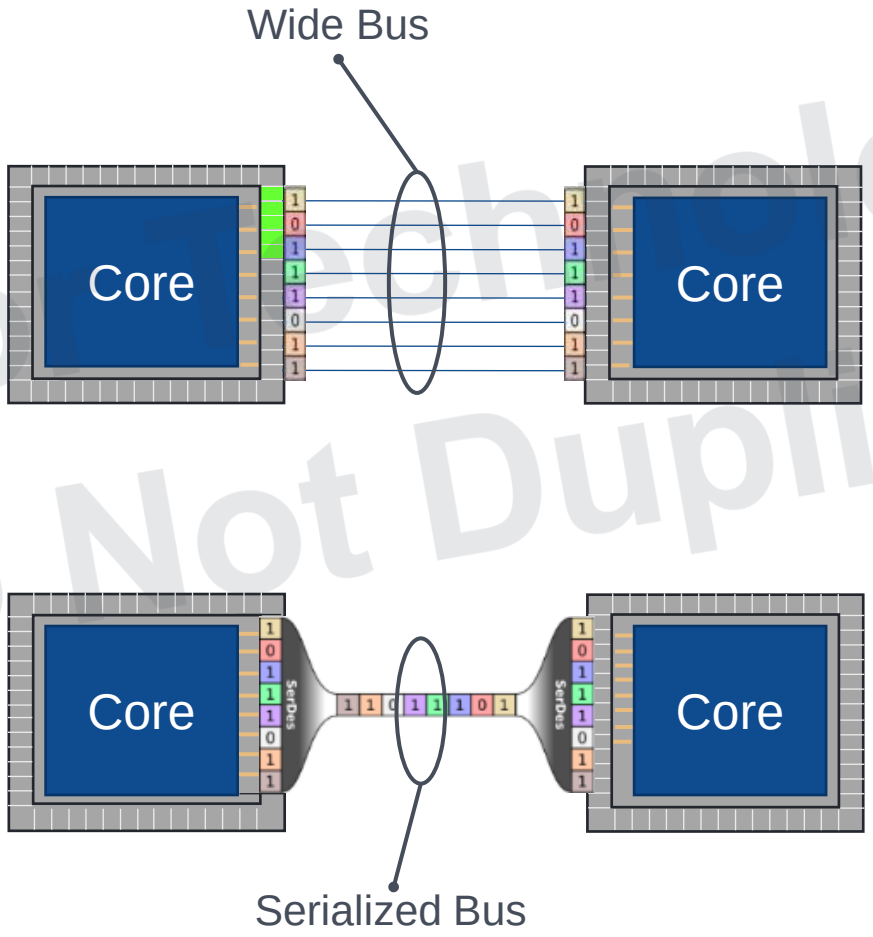




# Trends: Die-to-Die Interface (Bandwidth)

- Parallel interfaces
  - More physical wires
  - **Lower latency**
  - Lower power
- Serial interfaces
  - Fewer physical wires
  - Higher latency
  - Higher power




- Module based
  - One physical wire/bit
  - Each I/O driver is small
  - **HDFO / S-Connect**
  - **2.5D TSV**
- MCM
  - Many bits per wire pair
  - Large I/O driver area





# Universal Chiplet Interconnect Express (UCIe)

## UCIe

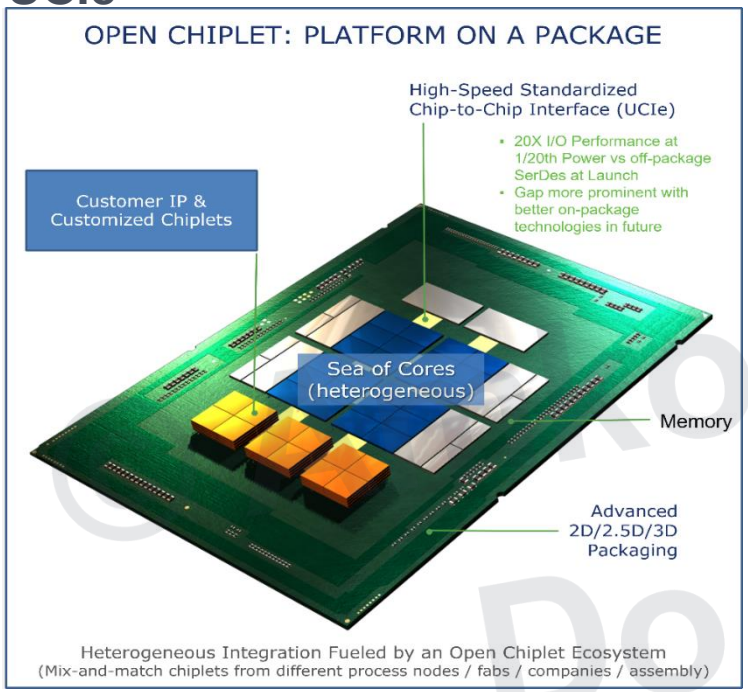
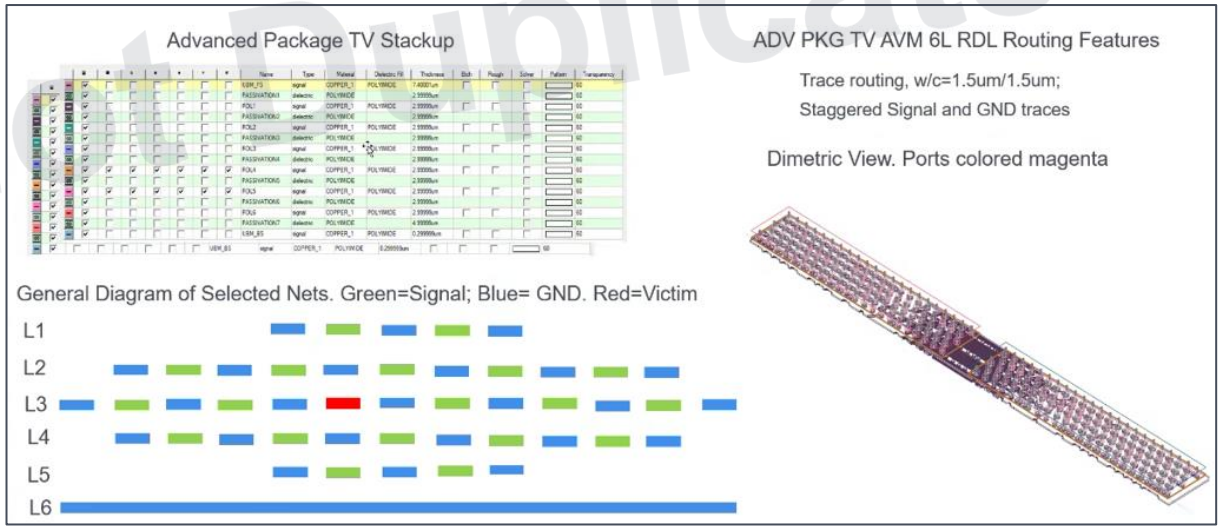



*image courtesy www.eetimes.com

- UCIe is an open industry standard, multi-protocol, high bandwidth (up to 32GT/s per lane), die-to-die (Chiplet), interconnect that standardizes inter-die communication on-package
- Amkor's HDFO technology will support the "UCIe Physical Layer (bus interface)" full frequency and time-domain simulations including RDL fabrication tolerances



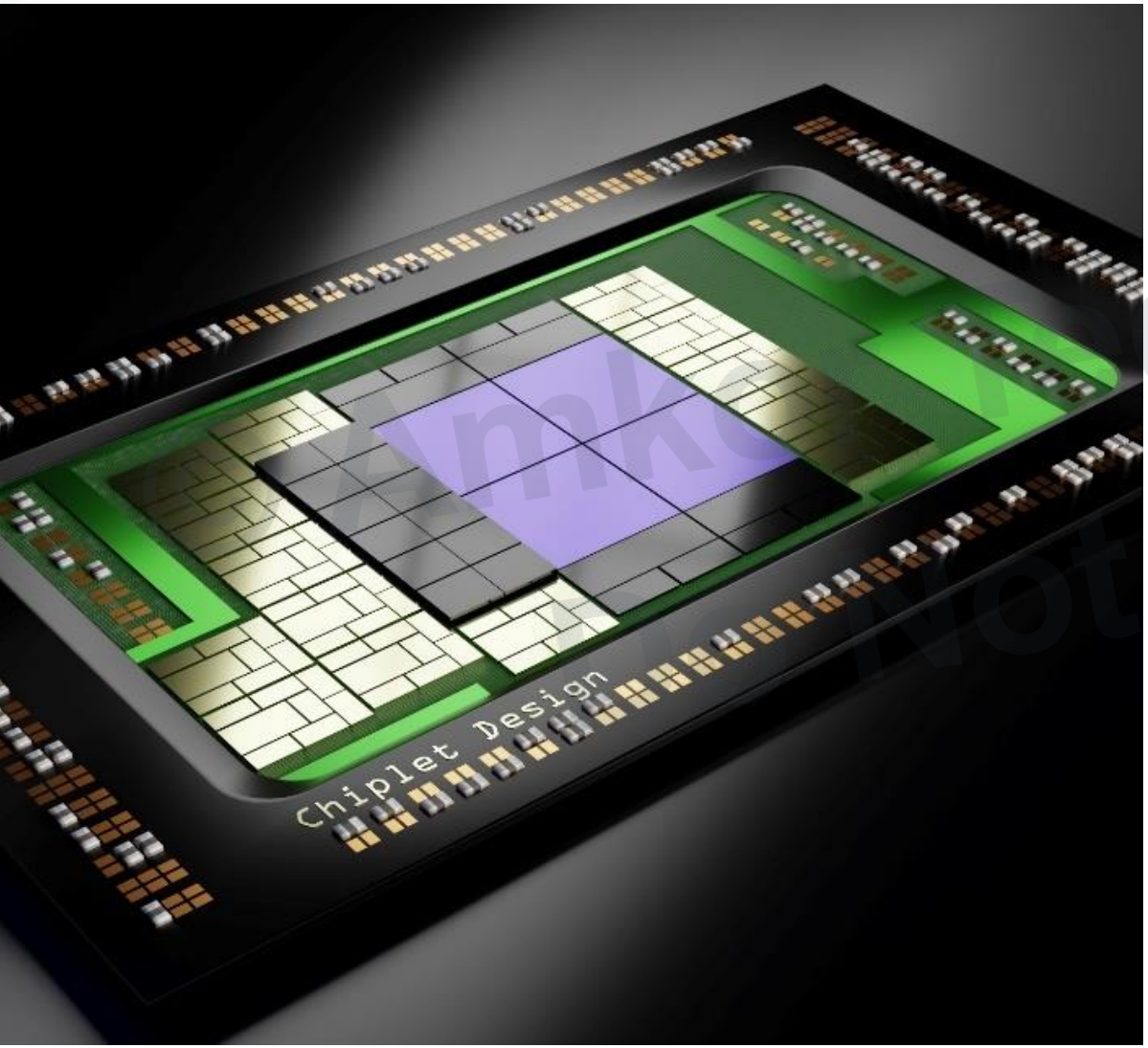




# Chiplet Advantage: Getting Started

## Package Perspective




- Decide on the Die-Die Interface
  - Required L/S to get signal/power routing accomplished
  - Layer count
- Select Die-Die Interface Construction
  - Substrate, HDFO interposer, Silicon bridge or interposer
  - Dies-Last or Dies-First
- Electrical analysis
  - Signaling: Check interface construction selection
  - Power Delivery: Bypass cap technology and location
- Dissipated Power
  - If lidded package: Polymer or Metal TIM
- Design and fabricate test-vehicle for full functional verification and reliability qualification





# Die-to-Die Interface Requirements

**Die-to-Die Interface**

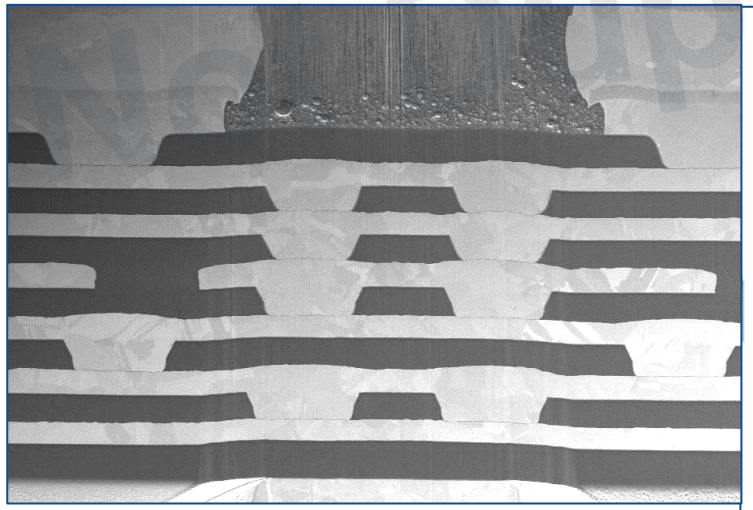
- Total die-to-die BW
- Line signaling speed
- Latency
- Bump pitches
- L/S & layer count

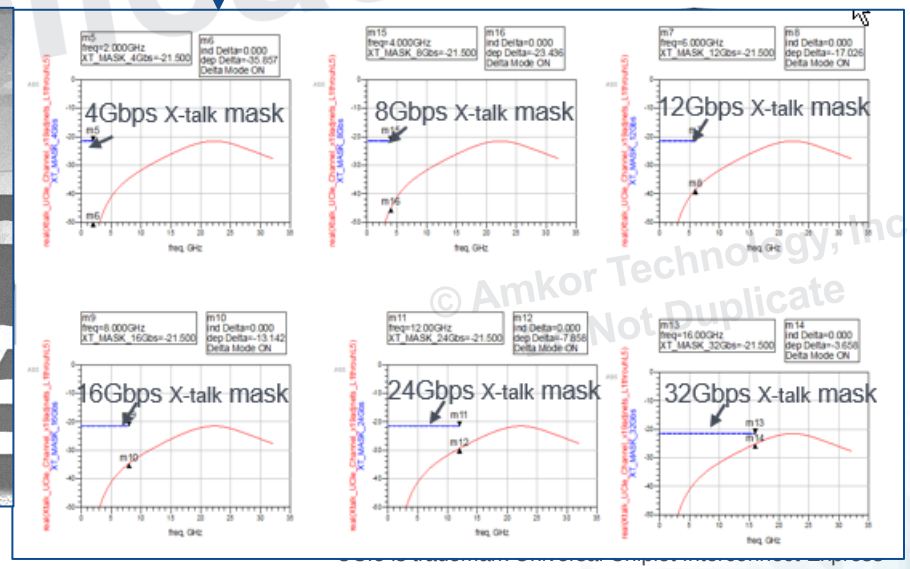
**Module Definition**

| Die-to-Die Interface | Requirements | |
|---|---|---|
| L/S | 2 µm | <1.5 µm |
| Layer count | 4 Layers | 3~4 |
| Bump pitch | 45 µm | <55 µm |
| **Construction** | **RDL – Cu/PI** | BEOL (Si) |
| **Signaling Rate** | 8, 12, 16, 32 Gb/s | |

UCIe™ Universal Chiplet Interconnect Express

OPEN Compute Project









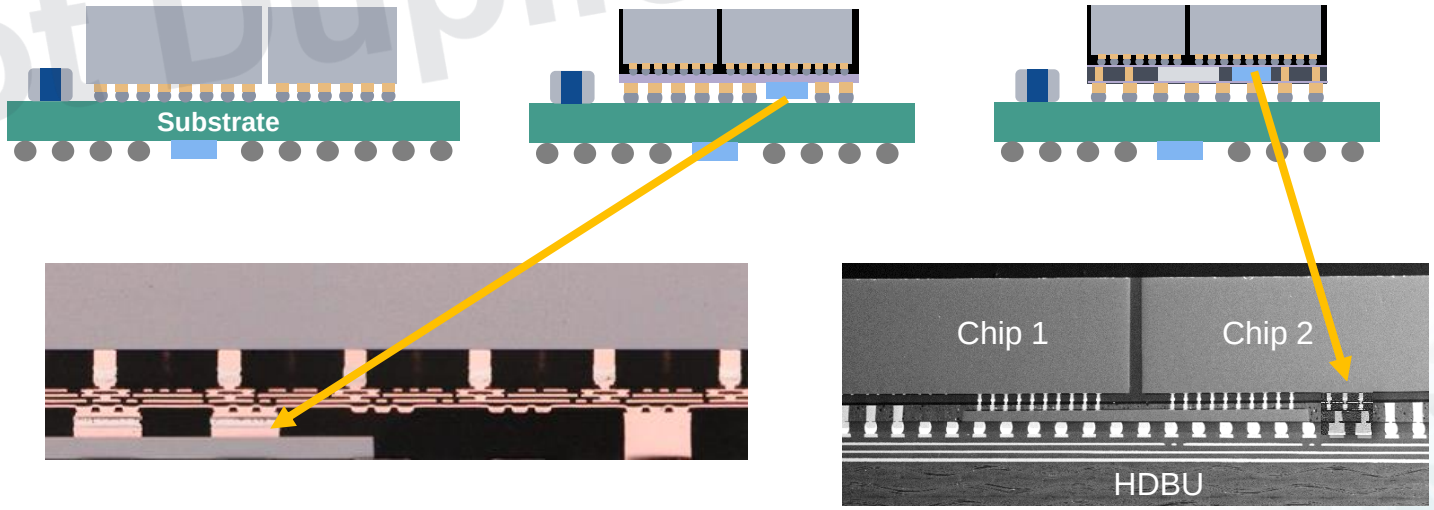
# Power Delivery Requirements

**Power Delivery**

- V = L di/dt
- Power supply strategy
- Proximity to the die
- Cap locations & value

**Module Definition**

| Requirements | | | |
|---|---|---|---|
| Passive type | | DTC type | DTC type |
| Distance to die edge | mm range | >50 µm | >50 µm |
| Distance to die core | mm range | **40**~80 µm | **20**~60 µm |
| Terminal pitch | 0.5~1.0 mm | <0.1 mm | <0.1 mm |
| **Construction** | **Flip Chip BGA** | **RDL Interposer** | **Bridge Interposer** |
| **Package Type** | | | |

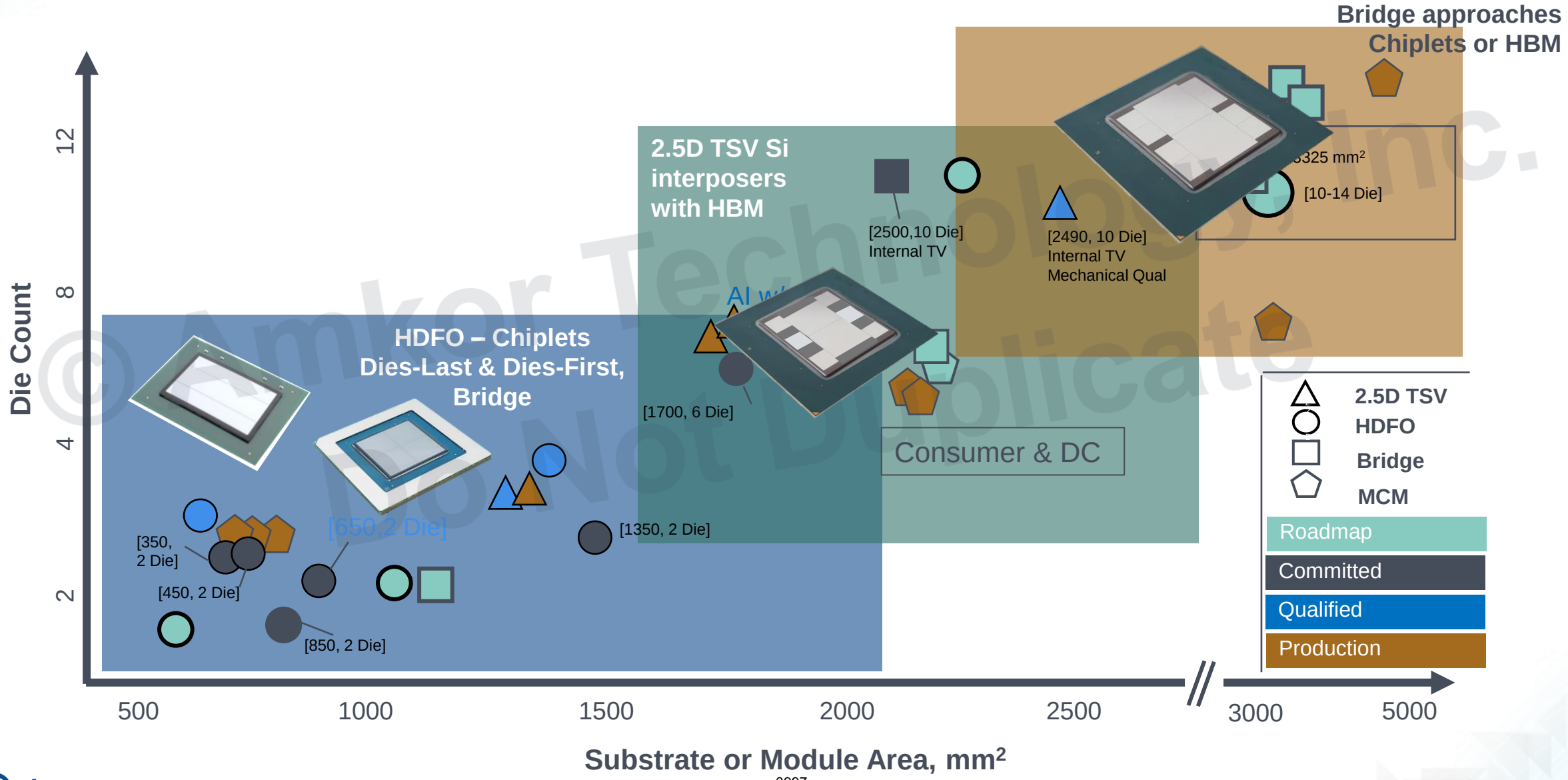






# Package Types for Heterogeneous/Chiplets



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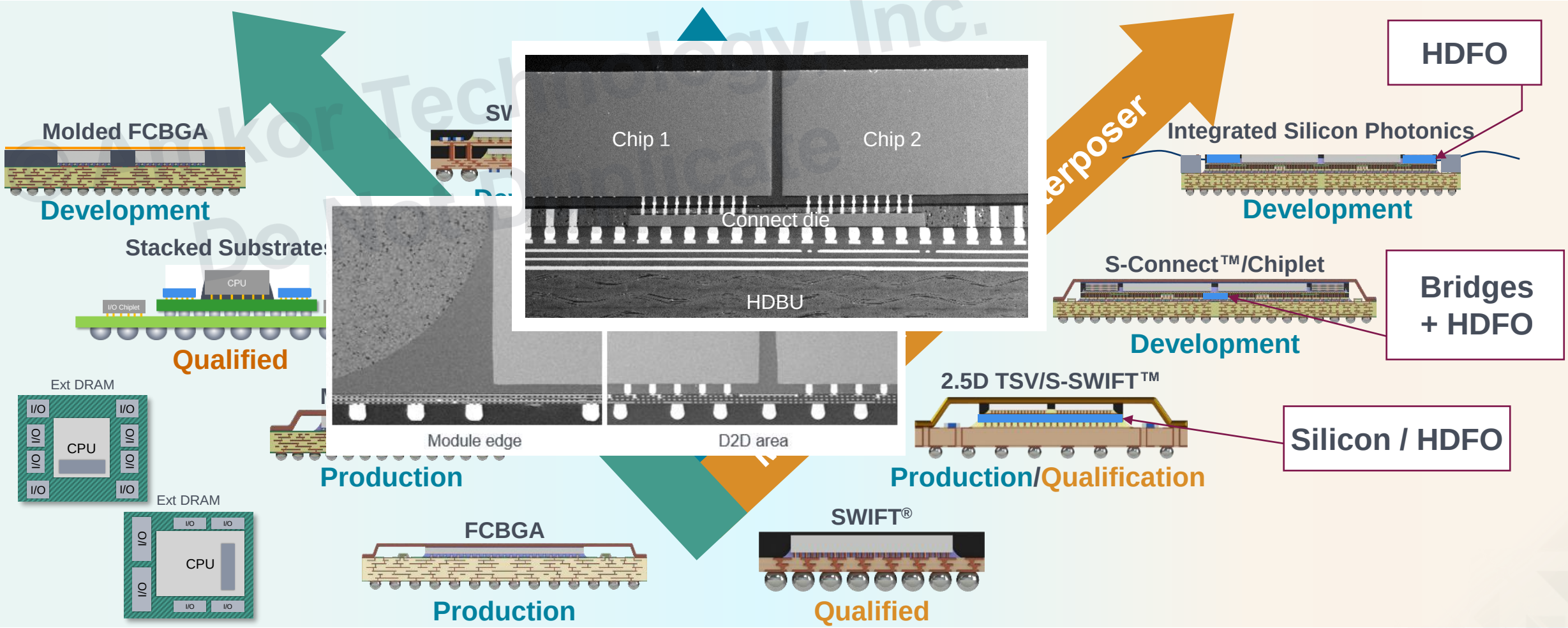
# Solutions: Chiplets HI Integration Paths







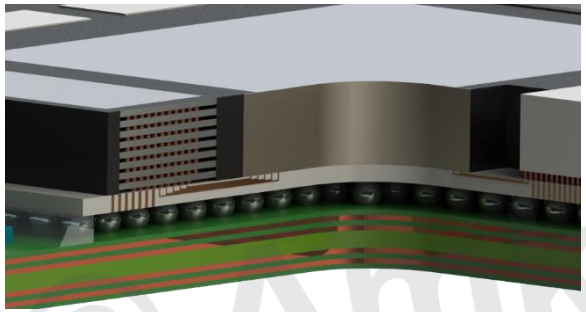

 

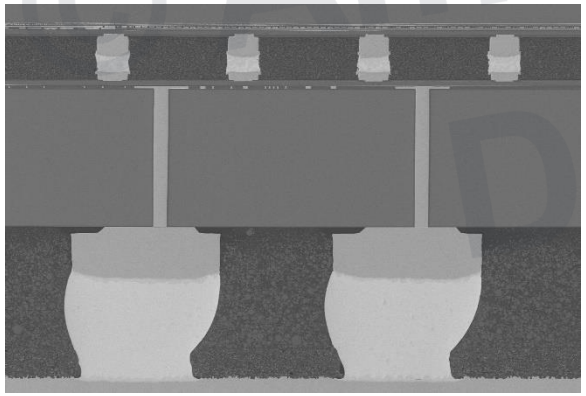
# Modules: 2.5D TSV Silicon Interposers



# Si Interposer Solutions (2.5D TSV)





| | |
|---|---|
| Package | ▶ Up to 85 mm body<br>▶ Dominated by ASIC + HBMx |
| Top Die | ▶ ASIC (5 nm, reticle size), 2x chiplets<br>▶ Up to 8x HBM (2/2E/3) |
| Interposer | ▶ Up to 3x reticle size<br>▶ Front and backside finish (MEOL) |
| Assembly | ▶ CoW |
| Reliability | ▶ STD FCBGA MSL4, TC'G' 1000x, uHAST 264 hrs, HTS 1000 hrs |
| Design | ▶ Full interposer design rules available |





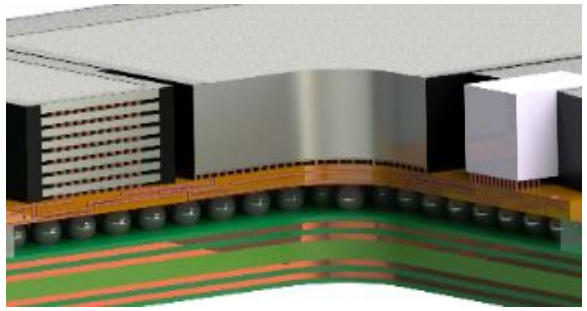
 

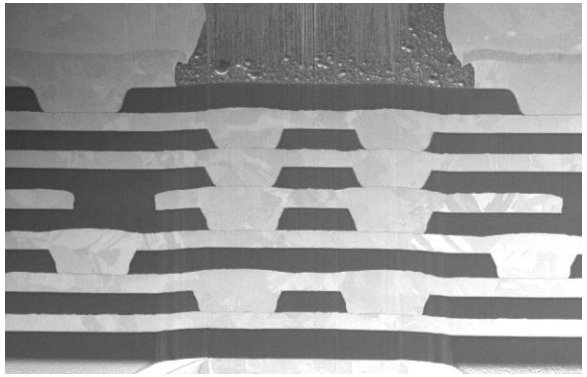
# Modules: HDFO (Substrate SWIFT™ [S-SWIFT™])



# HDFO (RDL) Interposer Solutions (S-SWIFT™)



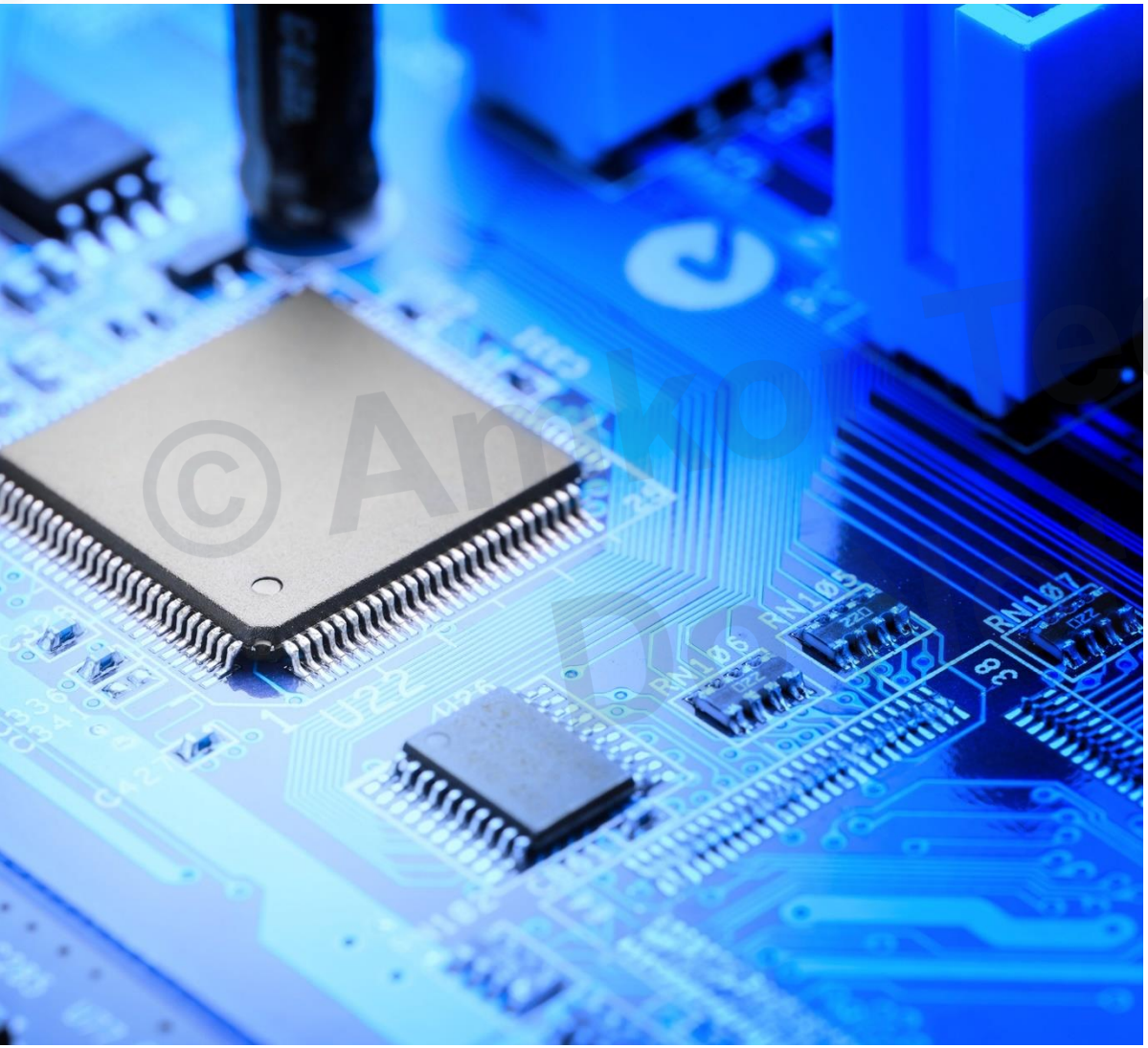


| | |
|---|---|
| Package | ▶ Up to 85 mm body<br>▶ Stiffener and lidded |
| Top Die | ▶ Chiplets (chip-first/last config) |
| Interposer | ▶ Up to 3x reticle size (~2500 $mm^2$)<br>▶ Front and backside finish (MEOL) |
| Assembly | ▶ CoW |
| Reliability | ▶ STD FCBGA MSL4, TC'G' 3000x, uHAST 264 hours, HTS 2000 hours |
| Design | ▶ Full interposer design rules available |



# HDFO Offerings



- Amkor offers both dies-first and dies-last process flows
- Current demand is dominate by dies-last product constructions
- We expect more demand for dies-first in the future as minimum bump pitches shrink for the die-die interfaces and bump pitch range stays large

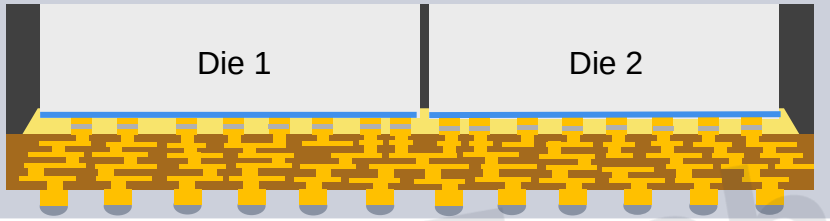
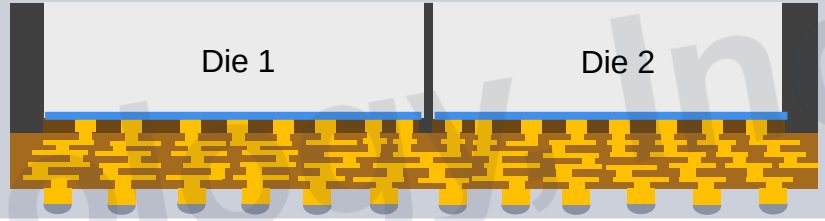




# S-SWIFT™ Dies-Last & Dies-First

## Structure and Features

| | S-SWIFT™ Dies-Last | S-SWIFT™ Dies-First |
|---|---|---|
| Structure |   |   |
| ASIC interconnection | Solder joint | RDL via plating |
| HBM bearing | Available | Not, available now |
| KGD loss issue | Less sensitive | More sensitive |
| Cost | Baseline | Lower cost |
| RDL layers | 2-6L qualified | 2L qualified |
| ASIC bonding | Face-down bonding | Face-up bonding |
| Die to RDL gap | Underfill | Passivation/Mold |
| Top Die Bumping | Baseline | More flexible |

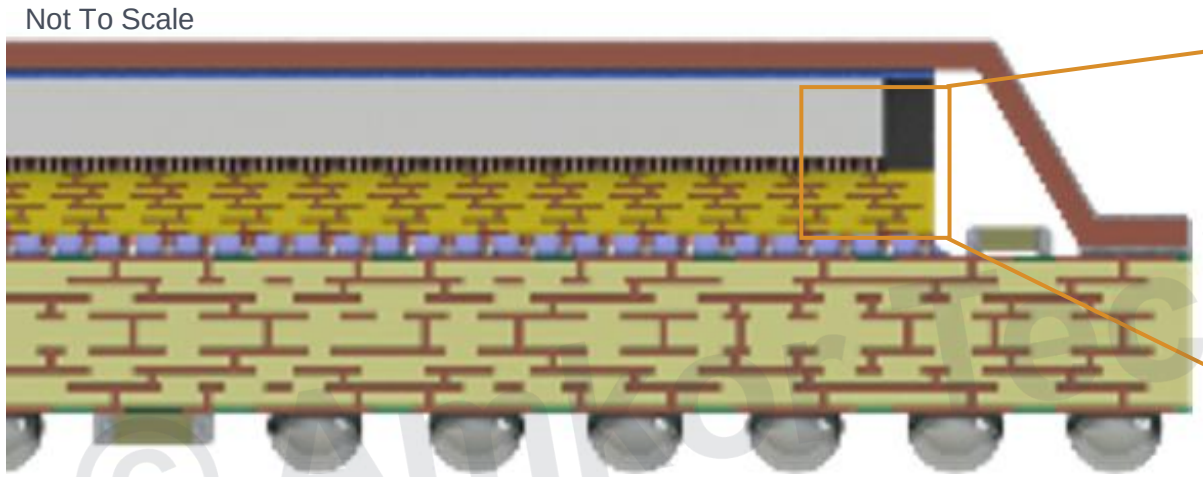


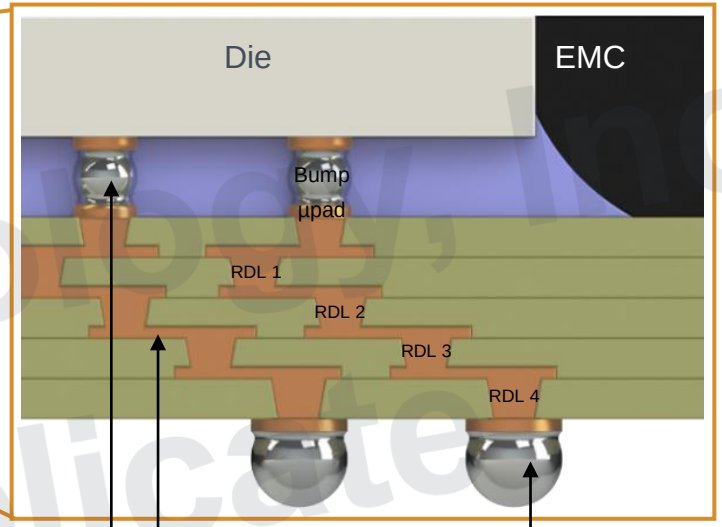


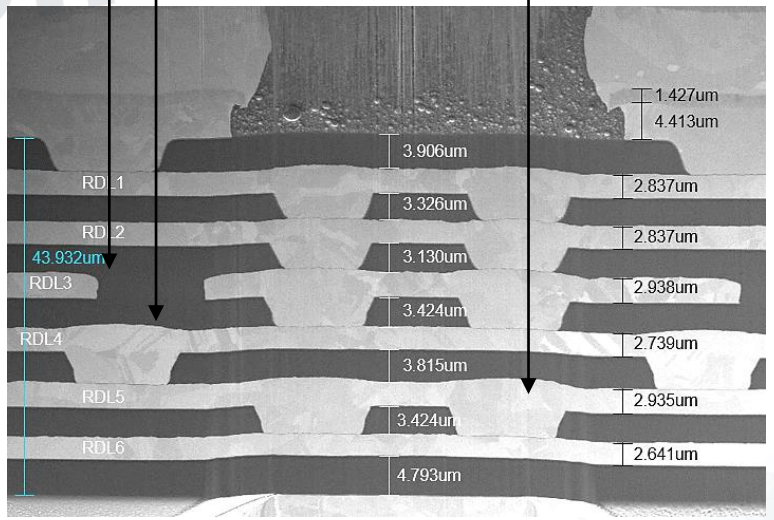
 

# High Density Fan-Out (HDFO), Dies-Last (S-SWIFT™)

Not To Scale






- Multi dies & HBM integration in fan-out module
- Multilayer copper and organic dielectric RDL
- 2 µm line/space capability, 2~6 layers
- 3 µm nominal Cu line height
- 3 µm nominal PI between Cu
- Flexible solution
  - Fine pitch support for L1 down to 40 µm pitch
  - Plated Cu pillar or LF solder for L2 bumps

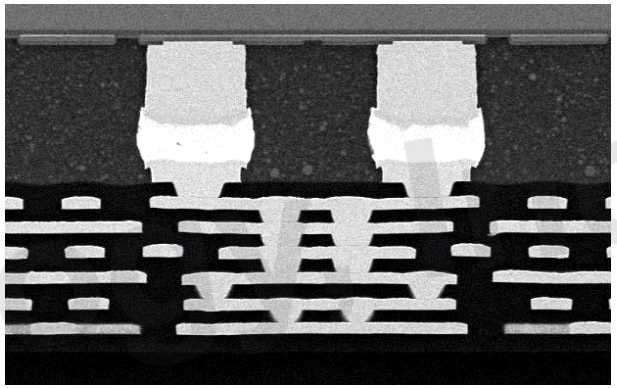




# HDFO Dies-Last: Reliability Performance

- S-SWIFT™ with 6L RDL
  - Package 51x51 mm/Module 27 x 27 mm
  - 4 chiplet dies 150 $mm^2$
  - 6L RDL with 2/2 µm L/S
  - 110 µm C4 BP



| Test Item | Test Condition | Read Point | MR | LAB |
|---|---|---|---|---|
| MSL4 | 30℃/60%RH 96H | 245℃ x3 | Pass | Pass |
| TCB | -55℃/125℃ | x500, x850, x1000 | Pass | Pass |
| | | x1500, x5000 | Pass | Pass |
| TCG | -40℃/125℃ | x500, x850, x1000 | Pass | Pass |
| | | x1500, x5000 | Pass | Pass |
| uHAST | 110℃/85% RH | 264 hrs | Pass | Pass |
| HTS | 150℃ | 500 hrs, 1000 hrs | Pass | Pass |





# Dies-First



# Amkor S-SWIFT™ Dies-First

- Generally used for smaller modules and packages
- **Typical** Package features
  - Module sizes: 300-600 $mm^2$
  - Die size: 40-120 $mm^2$
  - Bump Pitches: 30-50 µm
  - Line/Space: 2 µm L/S minimum


| Test Item | Test Condition | Read Point | Results |
|---|---|---|---|
| MSL3 | 30℃/60% RH 192H | 245℃ x3 | **Pass** |
| uHAST | 130℃/85% RH w/precon | 192 hrs | **Pass** |
| TCG | -40℃/125℃ w/precon | 1000x (and 2000x) | **Pass** |
| HTS | 150℃ | 1000 hrs (and 2000 hrs) | **Pass** |





# Modules: S-Connect™ Development Status



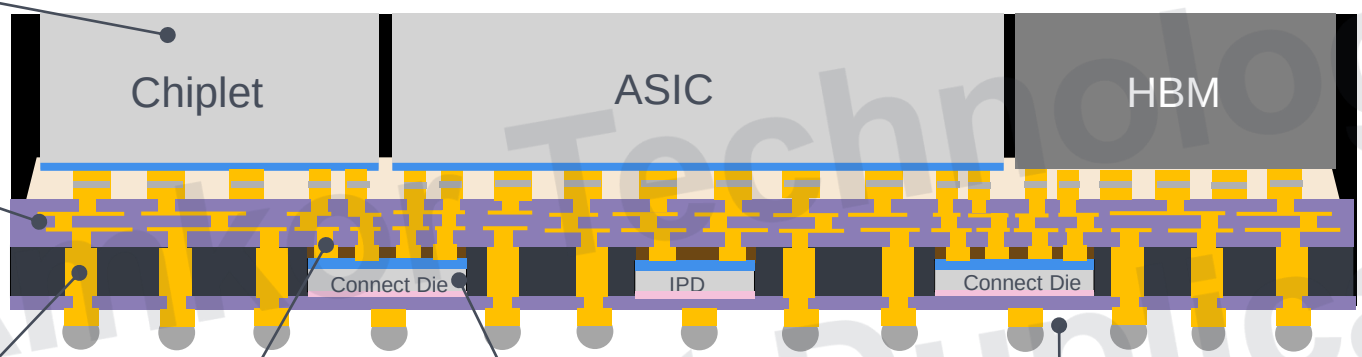
# Bridge Die Interposer Solutions (S-Connect™)

D2D gap
- 70 µm
- 50 µm (Available)

RDL L/S
- 10/10 µm
- 5/5 µm (Available)

RDL via diameter
- 10 µm
- 9~7 µm (Development)

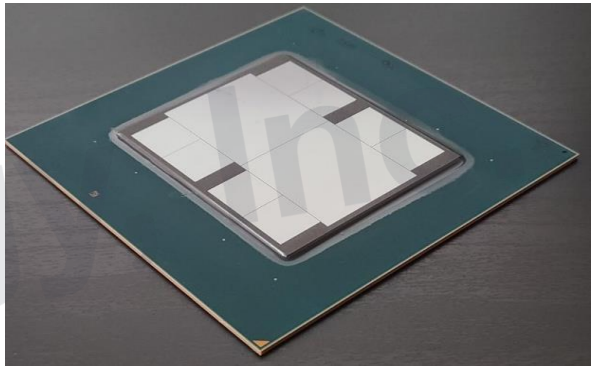
Cu tall pillar pitch
- 150 µm
- 127 µm (Development)

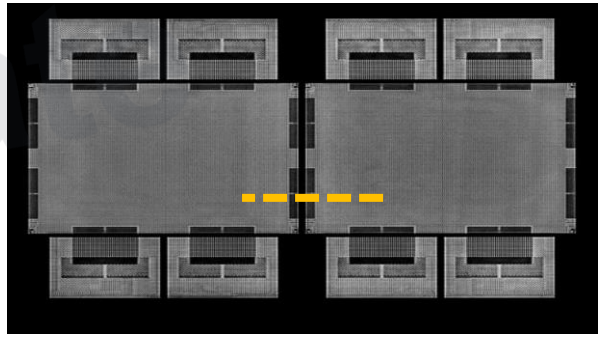


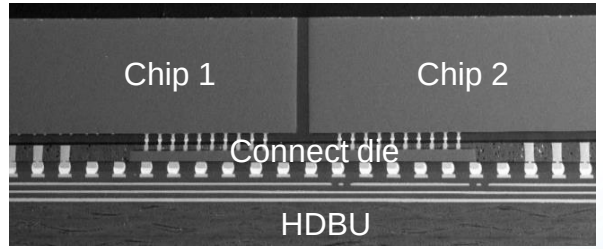

Connect area pitch (Chip last option)
- 55~50 µm
- 40 µm (Available)

Bridge die thickness
- 80 µm
- 50 µm (Development)

C4 CuP pitch
- 150~130 µm
- 120~110 µm (Available)











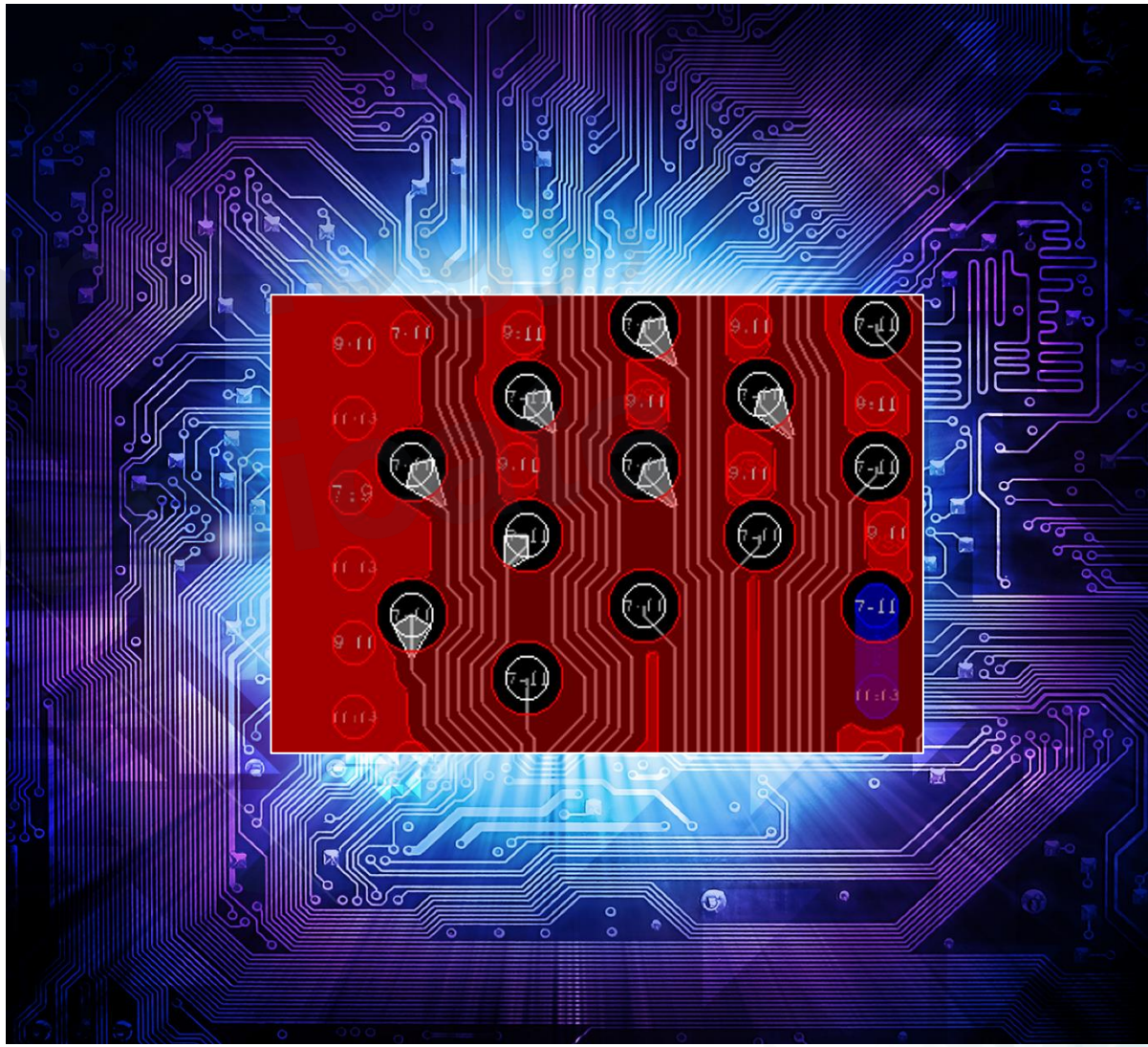

# SmartPackage™ PADK



# Amkor's SmartPackage™

- Amkor's SmartPackage™ offers
  - Customized heterogenous design experience
  - Full connectivity verification, DRC and assembly optimization
- Amkor is a package development and assembly leader enabling
  - Pathway for assembly requirements to be built into the SmartPackage™
  - Value of assembly verification earlier in the package design process

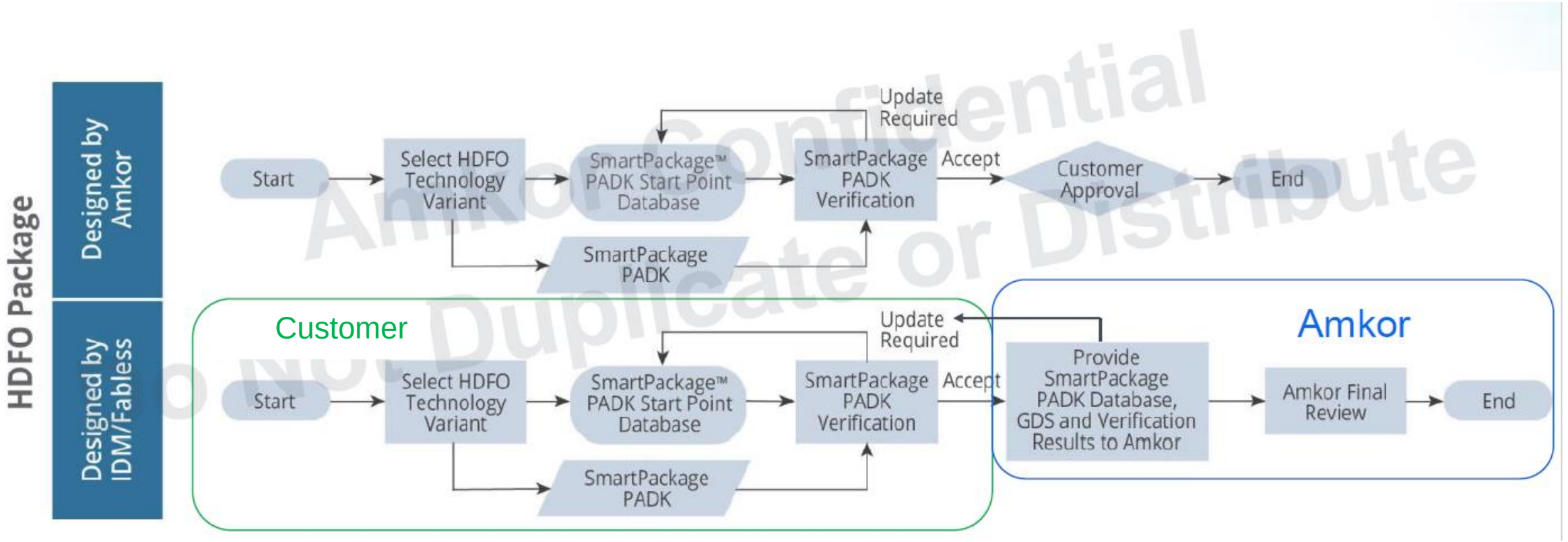






# Amkor's SmartPackage™







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# Thank You