New Innovative Way to Verify Package Connectivity

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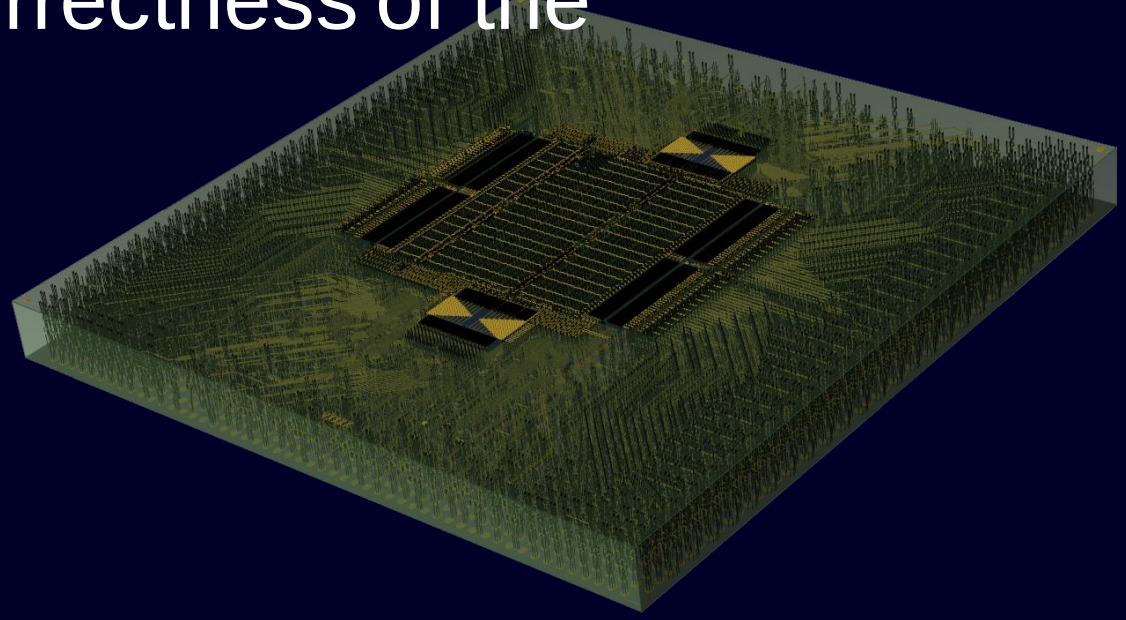
Integration of multiple ICs (chiplets) on a single substrate is critical for high performance computing. Due to the large number of connections involved connecting the various ICs, it is hard to verify the correctness of the connections.



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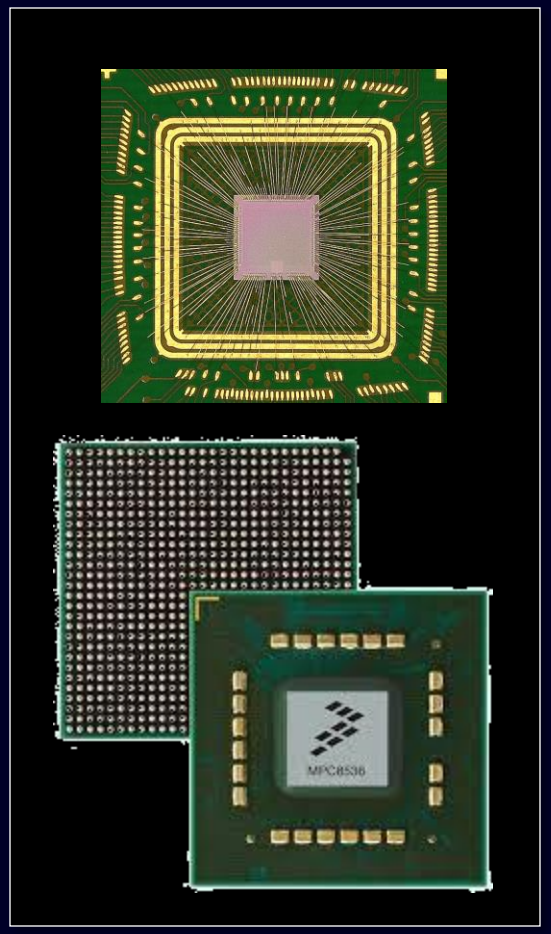
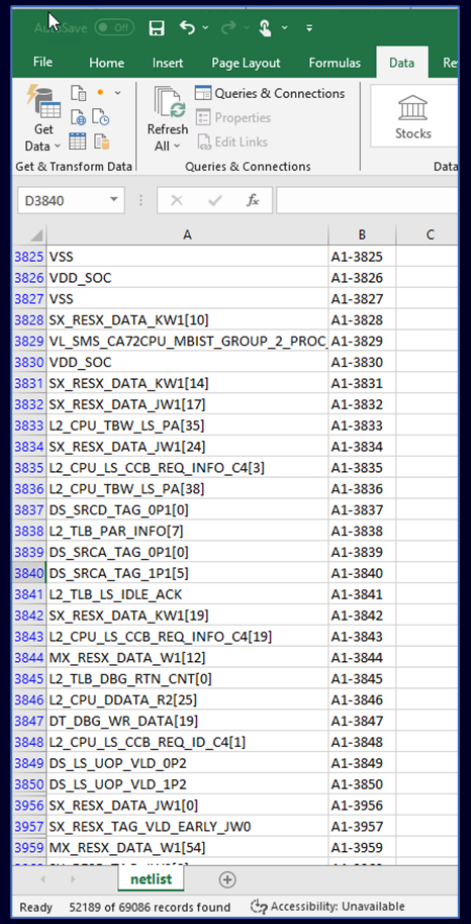
Historical vs Modern Package Design





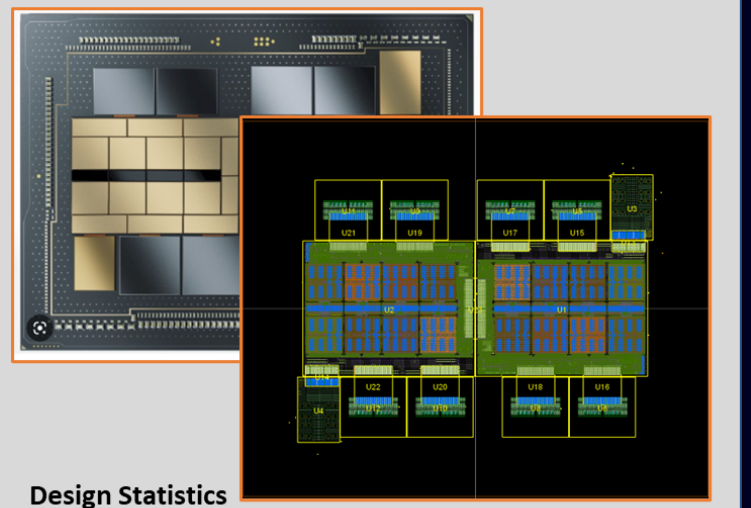
	A	B
3825	VSS	A1-3825
3826	VDD_SOC	A1-3826
3827	VSS	A1-3827
3828	SX_RESX_DATA_KW1[10]	A1-3828
3829	VL_SMS_CA72CPU_MBIST_GROUP_2_PROC	A1-3829
3830	VDD_SOC	A1-3830
3831	SX_RESX_DATA_KW1[14]	A1-3831
3832	SX_RESX_DATA_JW1[17]	A1-3832
3833	L2_CPU_TBW_LS_PA[35]	A1-3833
3834	SX_RESX_DATA_JW1[24]	A1-3834
3835	L2_CPU_LS_CCB_REQ_INFO_C4[3]	A1-3835
3836	L2_CPU_TBW_LS_PA[38]	A1-3836
3837	DS_SRCD_TAG_0P1[0]	A1-3837
3838	L2_TLB_PAR_INFO[7]	A1-3838
3839	DS_SRCA_TAG_0P1[0]	A1-3839
3840	DS_SRCA_TAG_1P1[5]	A1-3840
3841	L2_TLB_LS_IDLE_ACK	A1-3841
3842	SX_RESX_DATA_KW1[19]	A1-3842
3843	L2_CPU_LS_CCB_REQ_INFO_C4[19]	A1-3843
3844	MX_RESX_DATA_W1[12]	A1-3844
3845	L2_TLB_DBG_RTN_CNT[0]	A1-3845
3846	L2_CPU_DDATA_R2[25]	A1-3846
3847	DT_DBG_WR_DATA[19]	A1-3847
3848	L2_CPU_LS_CCB_REQ_ID_C4[1]	A1-3848
3849	DS_LS_UOP_VLD_0P2	A1-3849
3850	DS_LS_UOP_VLD_1P2	A1-3850
3956	SX_RESX_DATA_JW1[0]	A1-3956
3957	SX_RESX_TAG_VLD_EARLY_JW0	A1-3957
3959	MX_RESX_DATA_W1[54]	A1-3959

Traditional Package Netlist

- Captured in Excel
- Simple table of net names and pin assignments
- Created by package designer using input from silicon team
- Low risk for single die and low pin count package designs
- Netlist verification performed manually or through simple text compare scripts

Package Complexity has exploded

- Multi-die designs are common
- Device pin counts approaching 1m and trending higher
- 200k+ net connections
- Created from disparate data sources (GDS, LEF/DEF, CSV)
- Netlist verification is a challenge – does netlist match intent?



Design Statistics

- 47 die, 5 process nodes
- >100B transistors
- 77.5mm x 62.5mm
- 51,708 nets
- 214,657 connections
- 25 layers
- 250K device pins
- 606K vias

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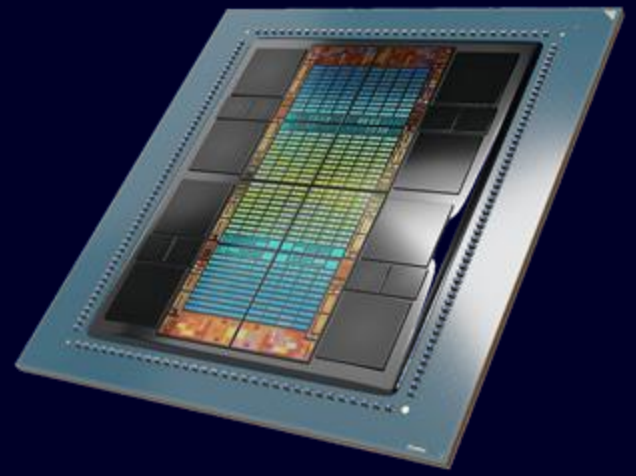
Modern substrate design has become a system integration task:

- Heterogeneous integration introduces new challenges for the substrate design engineer
- Source data is being aggregated from a myriad of data formats:
  - Ball map CSV files
  - OASIS, GDS, and LEF/DEF from P&R tools
  - Verilog RTL
  - Spreadsheet Data
  - Plain text files
  - 3Dblox™



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Legacy connectivity methods no longer viable

- HBM‡ is driving explosion of connectivity for AI and HPC applications
- Using Excel for netlist management is no longer practical
- Verilog RTL is becoming more prevalent due to chiplet designs
  - Far more efficient to connect die to die interfaces
  - Use of bus notation greatly decreases chance of error (d[63:0] vs d63, d62, …., d1, d0)
  - Ability to re-use RTL work done by ASIC design and verification teams
- Specialized tools such as Siemens Xpedition Substrate Integrator (XSI) address the challenges of managing large scale connectivity problems

‡HBM: https://en.wikipedia.org/wiki/High_Bandwidth_Memory

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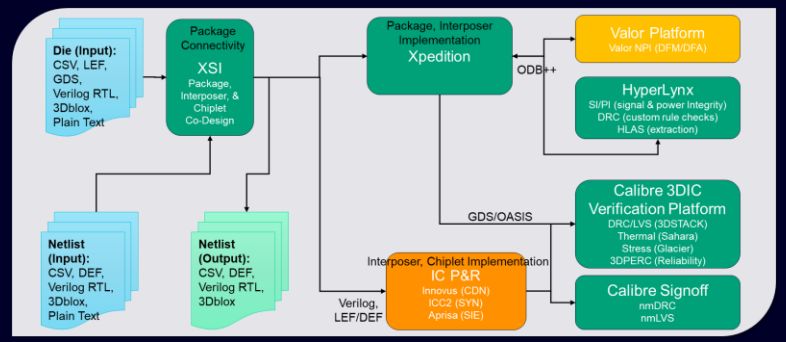
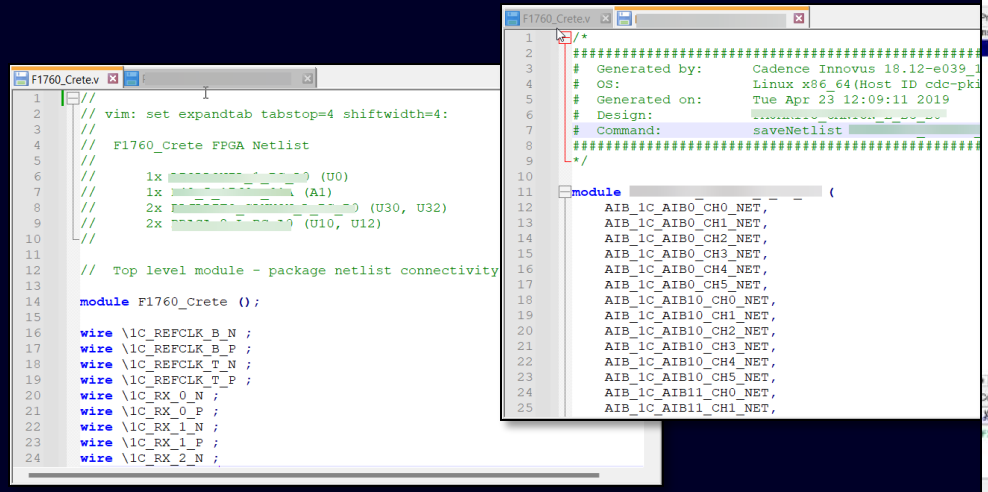
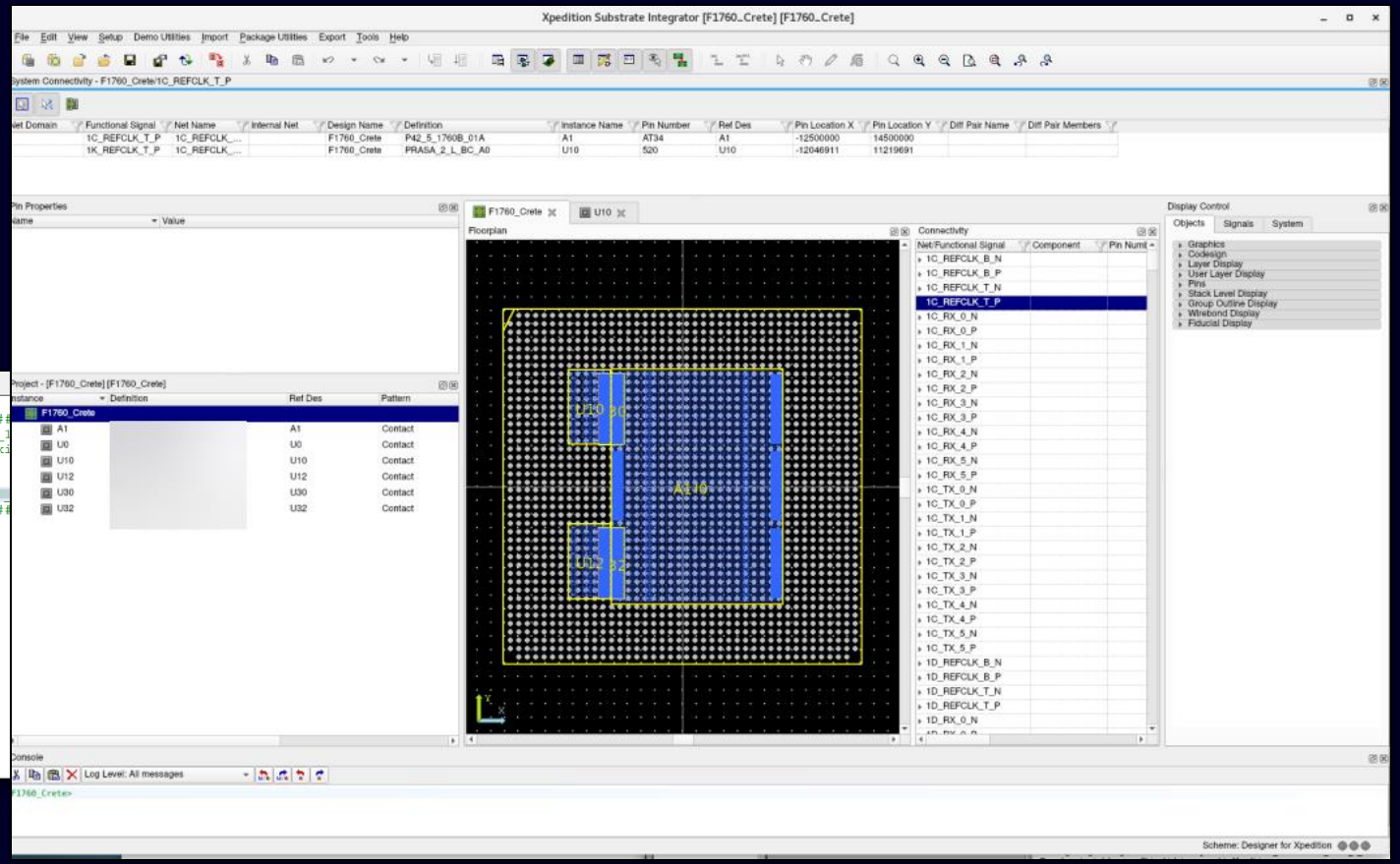
Import Verilog Connectivity into XSI







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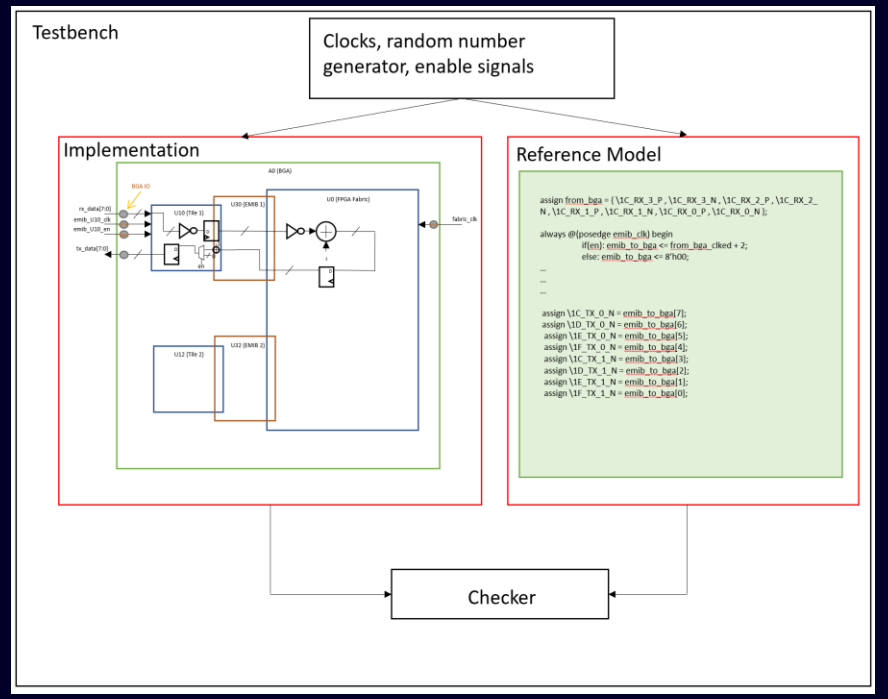
Challenges of Functional Verification

- Functional models for each die
- Models or provisions for discrete components
- Testbench to exercise the functionality and verify correctness
- Expertise to develop and run simulation(s)
- While it is technically possible to perform functional verification of a complex substate assembly, it is often impractical to do so for a number of reasons.



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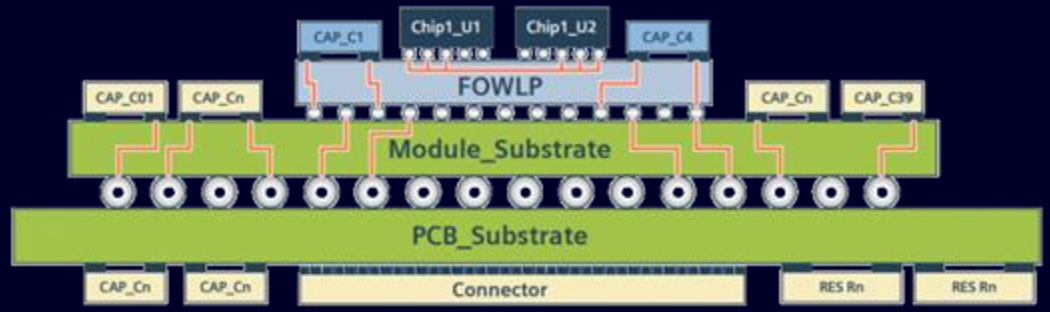
Layout vs Schematic



- What about LVS? Can't LVS verify our system? Yes and No
- LVS at the system assembly level is gaining popularity thanks to tools such as Siemens Calibre 3DSTACK
- LVS can only tell us if the physical implementation of the design matches the source netlist
- LVS can identify shorts and opens and other similar physical issues but it cannot tell us if the design is actually "correct"

Automatic Formal-based Approach

- Benefits of formal connectivity solution for package designs:
  - Easy setup
    - No lengthy simulation testbenches
  - Detect connection errors
    - Specified connections don’t exist.
    - Unintended connections, e.g. short circuits.
  - Ensure correctness of connections
    - Exhaustive analysis and proof capability
  - Complex systems with millions of connections
  - Early detection
  - Compliance
    - Siemens Check Connect is ISO 26262 certified

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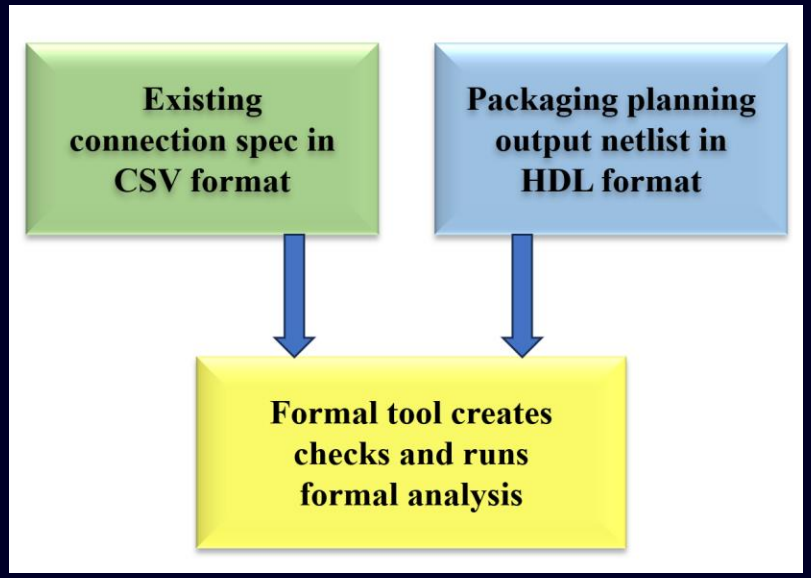
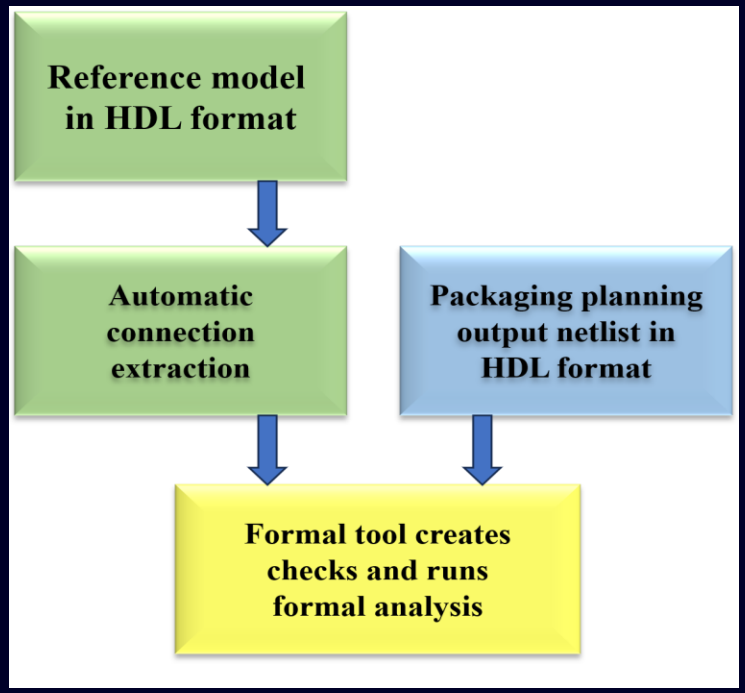
Two Flows of Verifying Package Connectivity

Using existing connection spec in CSV

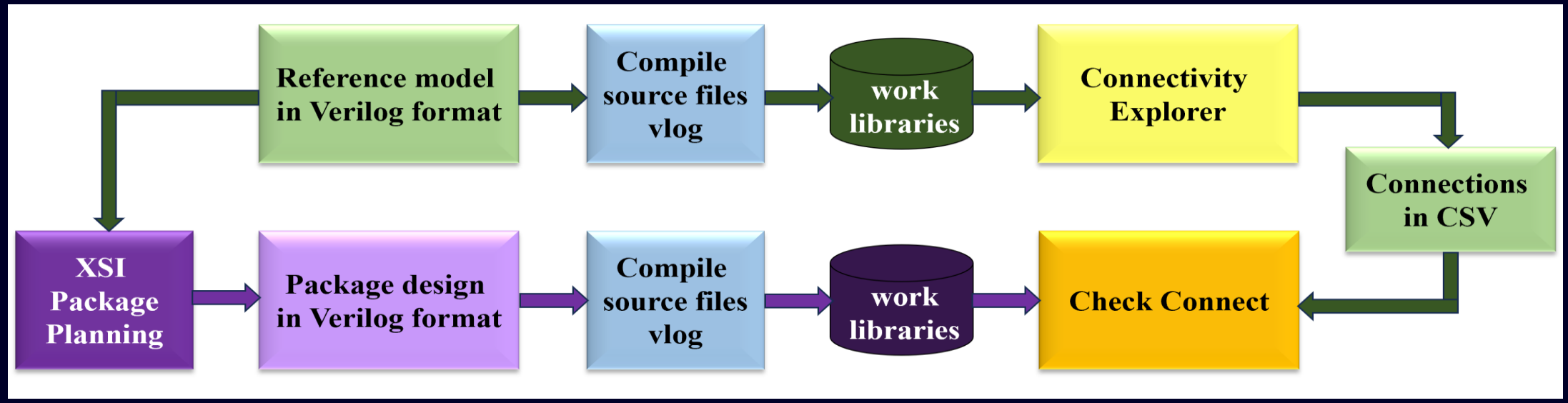


Using reference model to extract spec



The Detail Flow of the Examples

- Package design used tool XSI, and XSI generated Verilog netlist.
- Connectivity Explorer generated connection spec in CSV file.
- Check Connect verified the connections of XSI output against the spec.



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The Script to Verify Package Connectivity

Makefile:

```
#### Compile designs
 Compile_vl:
        vlog -sv -f flist_golden.txt -work lib_golden
        vlog -sv -f flist_package.txt -work lib_package
#### Generate Connectivity Spec
 Generate_conn_csv:
        qconnect_check -explore -od log_csv \
        -infile config.txt \
        -dut F1760_Crete -work ./lib_golden
#### Run Formal Analysis
 Check_connect:
        qverify -od log_cc -do "\
        connectcheck compile -d F1760_Crete -work lib_package;\
        connectcheck load csv log_csv/qconnect_explore_F1760_Crete.csv;\
        connectcheck verify "
```

Understand Formal Verification

- Black box function logic of blocks help formal performance
- If formal finds a violation, it provides waveforms to show the violation
- If formal proves a connection, no stimulus can violate it.
- When all spec items are proven, the package design has all expected connections.
- What if the connectivity specification misses some connections?
  - Check Connect can detect them.

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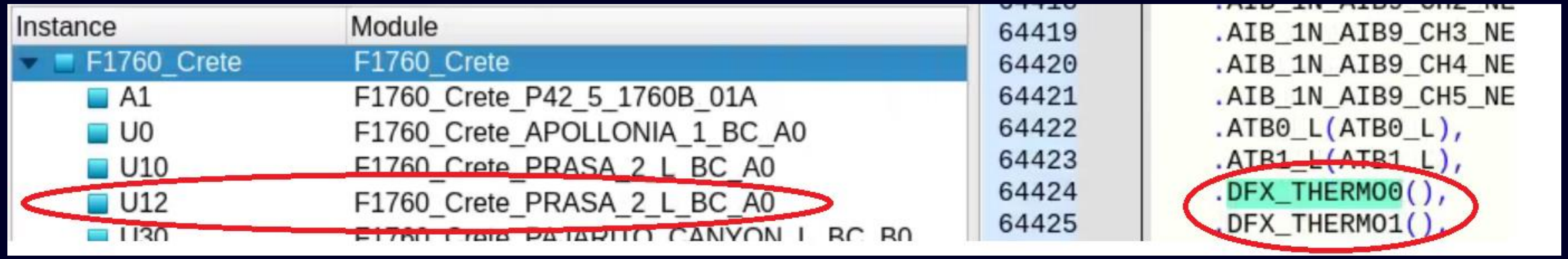
The Results of Two Testcases

	Time for extracting connection spec	The number of connections	Verification results	Time for verifying the package design
Design 1	15 seconds	21367	All proven	30 seconds
Design 2	35 seconds	43440	All proven	56 seconds

Missing Connections Found

- The tool found two missing connections.
  - The designer has purposely left two thermal sensor pins unconnected
  - The designer was impressed they were identified.



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Conclusion

- Verifying package connectivity is challenging.
- Automatic formal-based approach is the solution.
- The setup for running formal tool is simple and reusable.
- Formal can verify large number of connections for big package designs.
- Using formal method right after package planning can improve the quality of physical implementation dramatically and shorten the time to market.

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Questions?

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Thank You!

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