Saras Embedded STile™ IPD Technology for High Performance Power Delivery Networks

Bart DeProspo
Director of Product Management

Outline

- Company Introduction
- Power Challenges
- Proposed Solutions
- Saras STile Solution
- Summary and Conclusions

Saras Micro Devices

To be the leading supplier of advanced power delivery solutions for leading AI/ML, HPC, & network systems

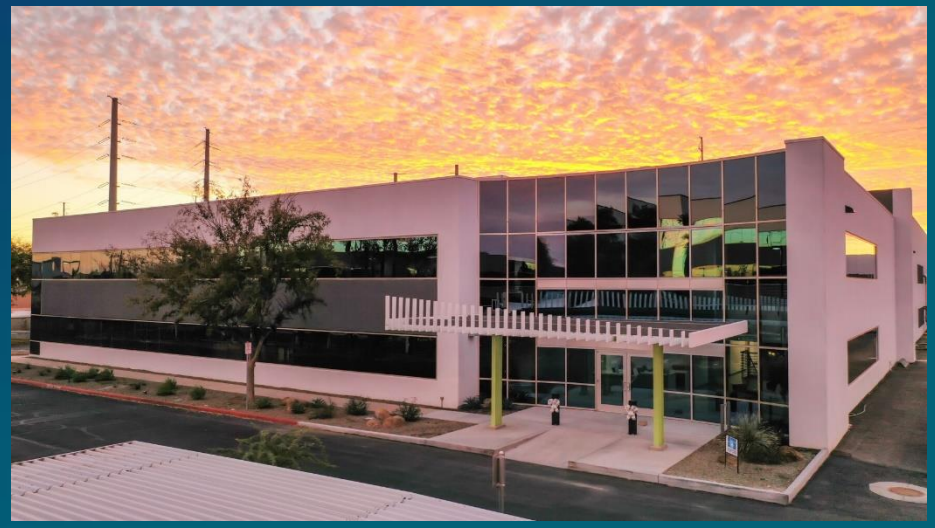
April 2021
Founded in Atlanta, GA

August 2022
Opened Cupertino, CA Sales office

March 2023
'Start-up of the Year' by 3D InCites

August 2023
Opened Atlanta Inland Tract COE

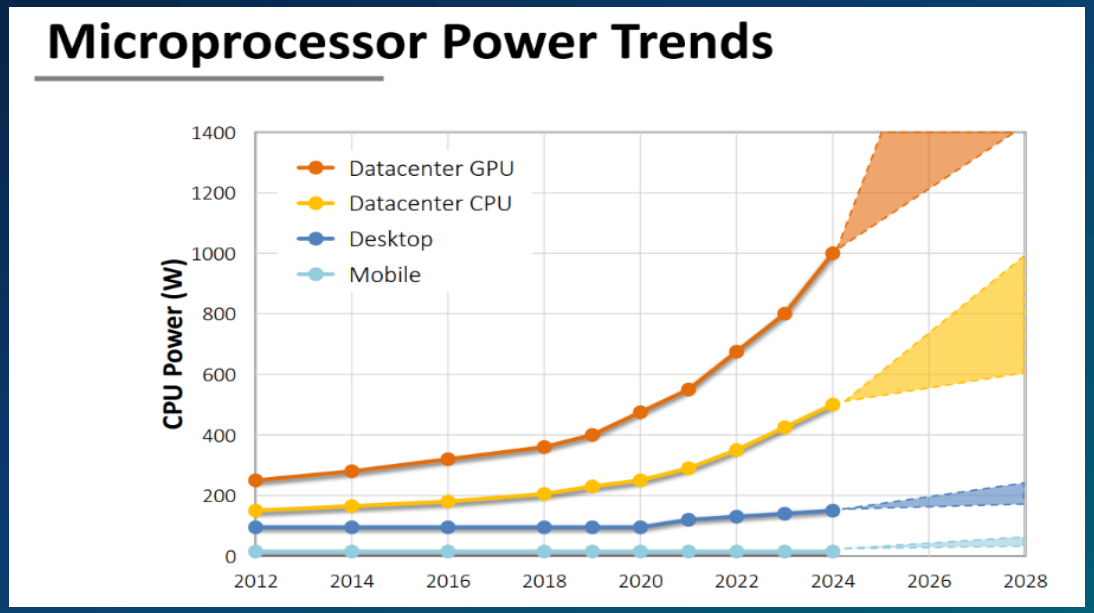
January 2024
Launched new HQ in Chandler.



Manufacturing COE and HQ (Chandler, AZ)

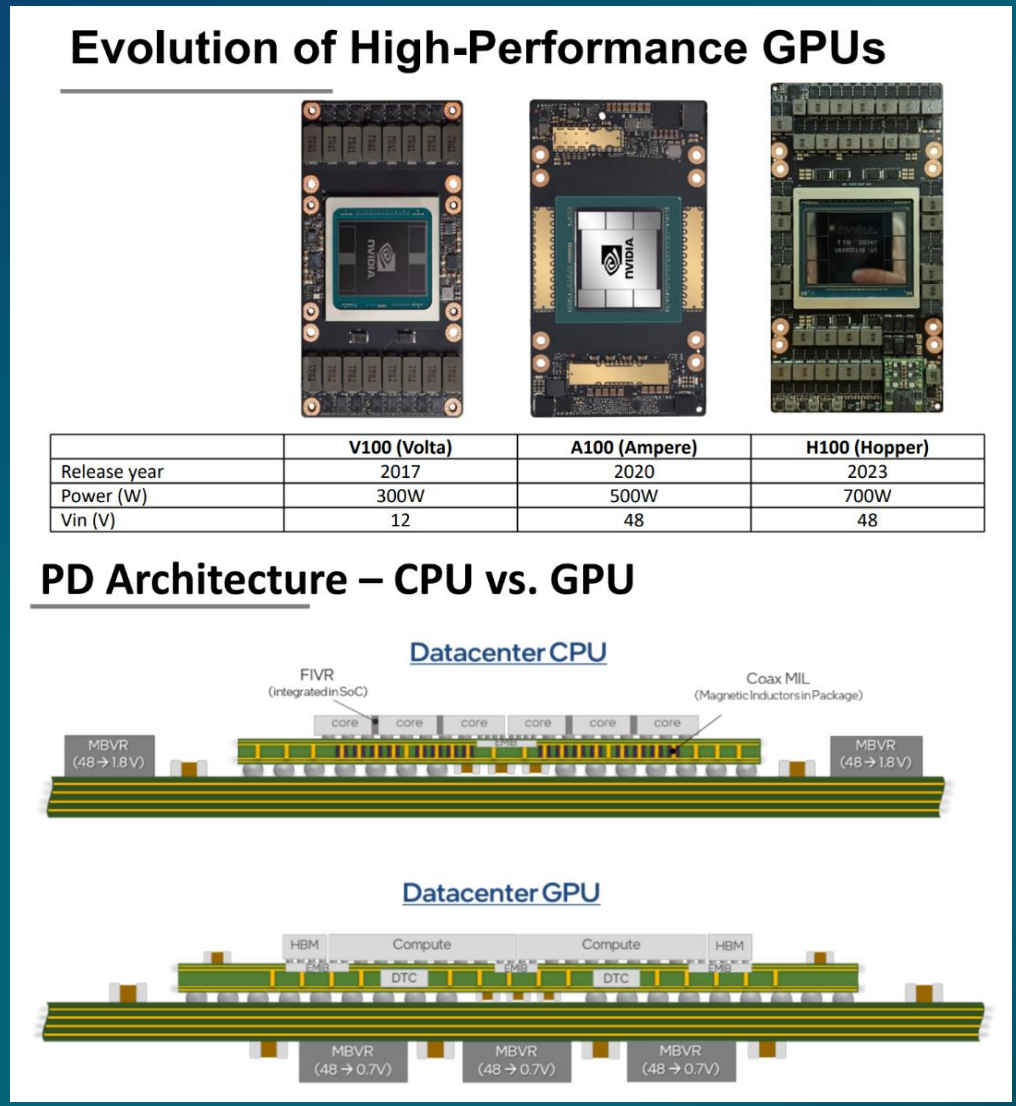
R&D COE (Atlanta, GA)

Power Problem



Source: Intel 2024[1]

- Increasing Power and Current Density
- Rising I^2R losses due to higher I and lower V
- Reduced space for package level Caps

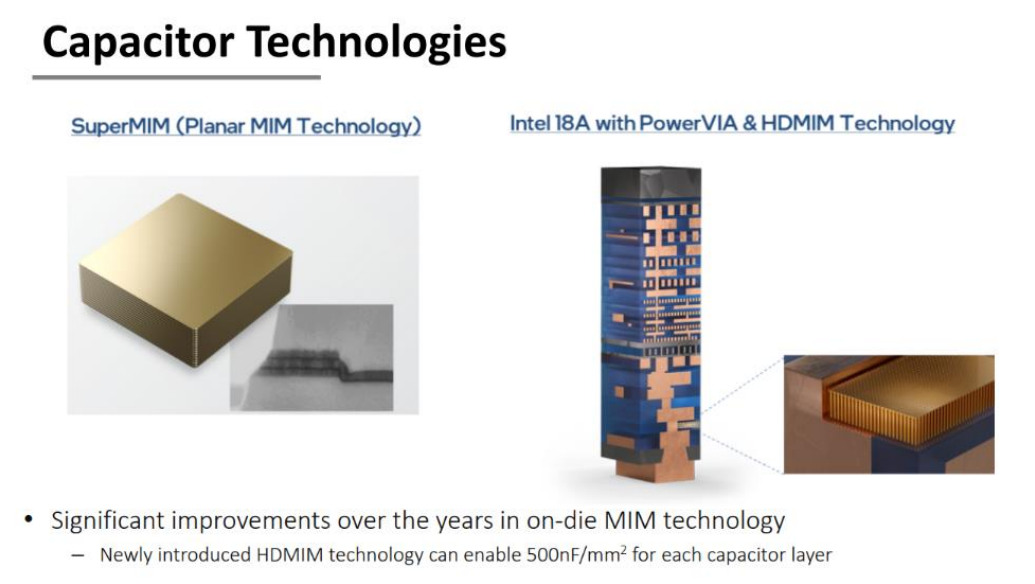


	V100 (Volta)	A100 (Ampere)	H100 (Hopper)
Release year	2017	2020	2023
Power (W)	300W	500W	700W
Vin (V)	12	48	48

Source: nVidia 2024[2]

Proposed Solutions

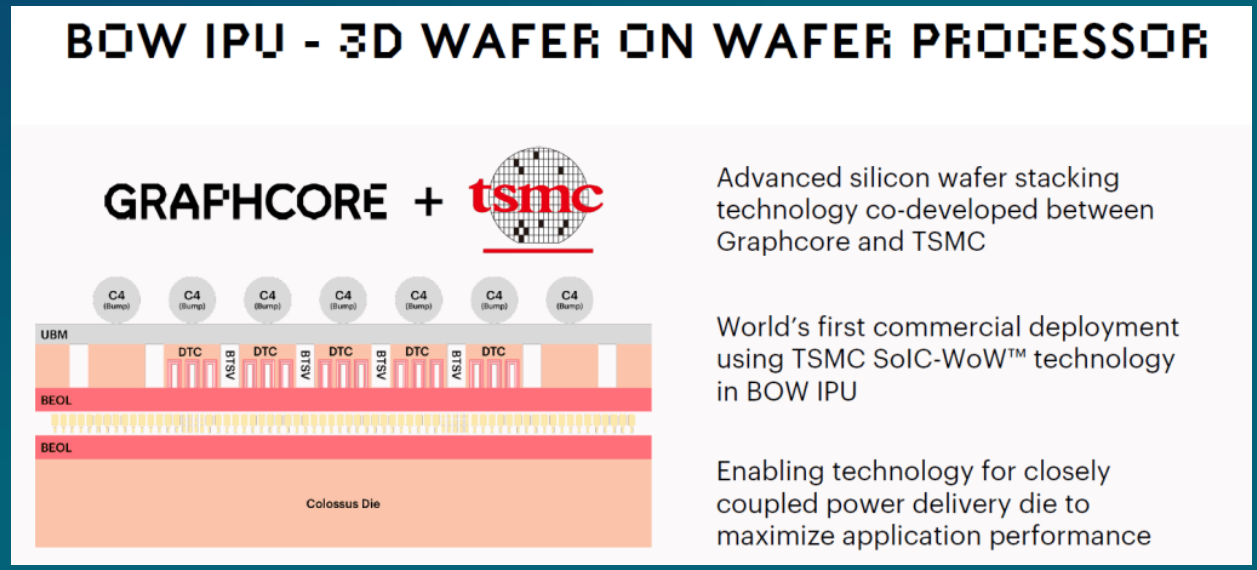
On Chip



Source: Intel[3]

- On Chip Back-Side Power Delivery
- Focus on Capacitor integration with Silicon

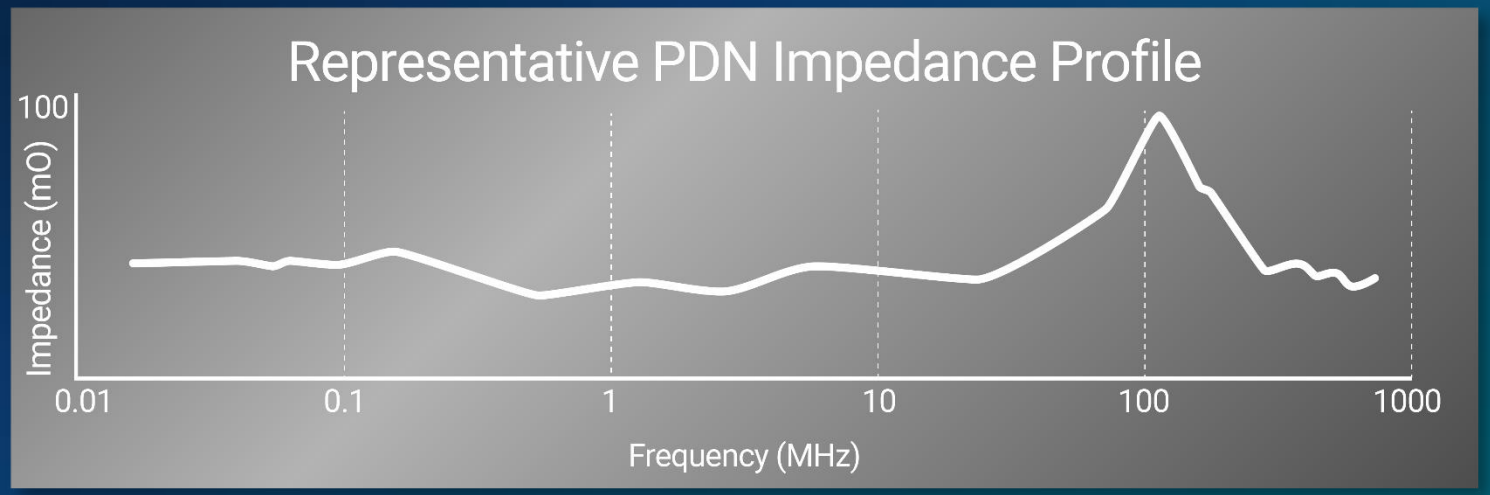
Package Level

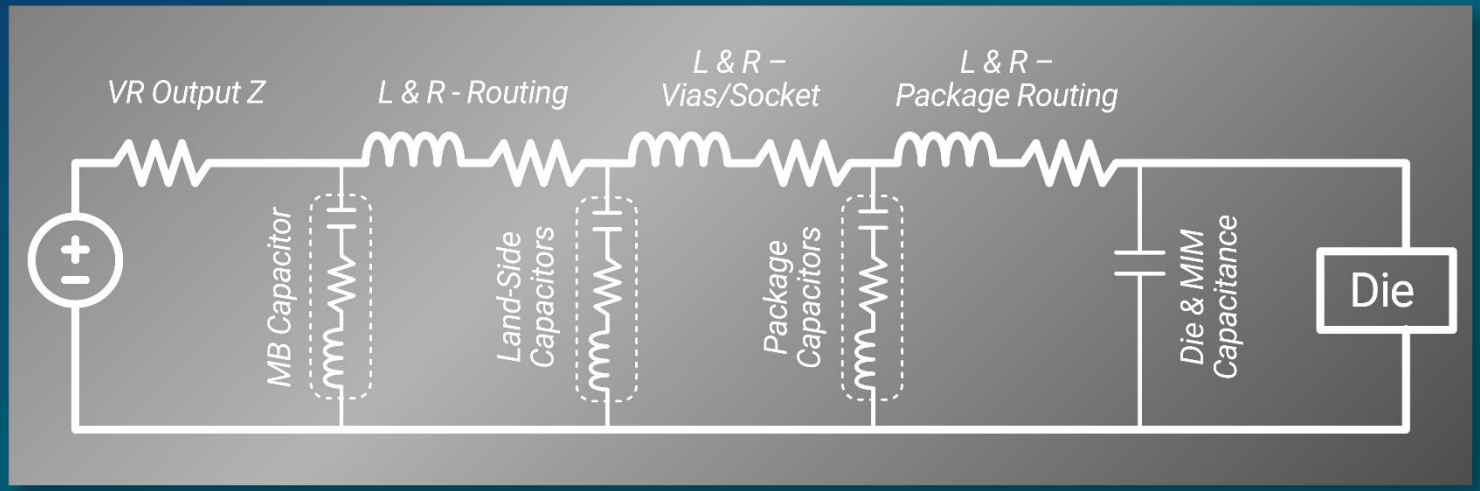


Source: TSMC[4]

- Silicon DTC Interposer
- Embedded IPD's in Silicon

Todays PDN Approach





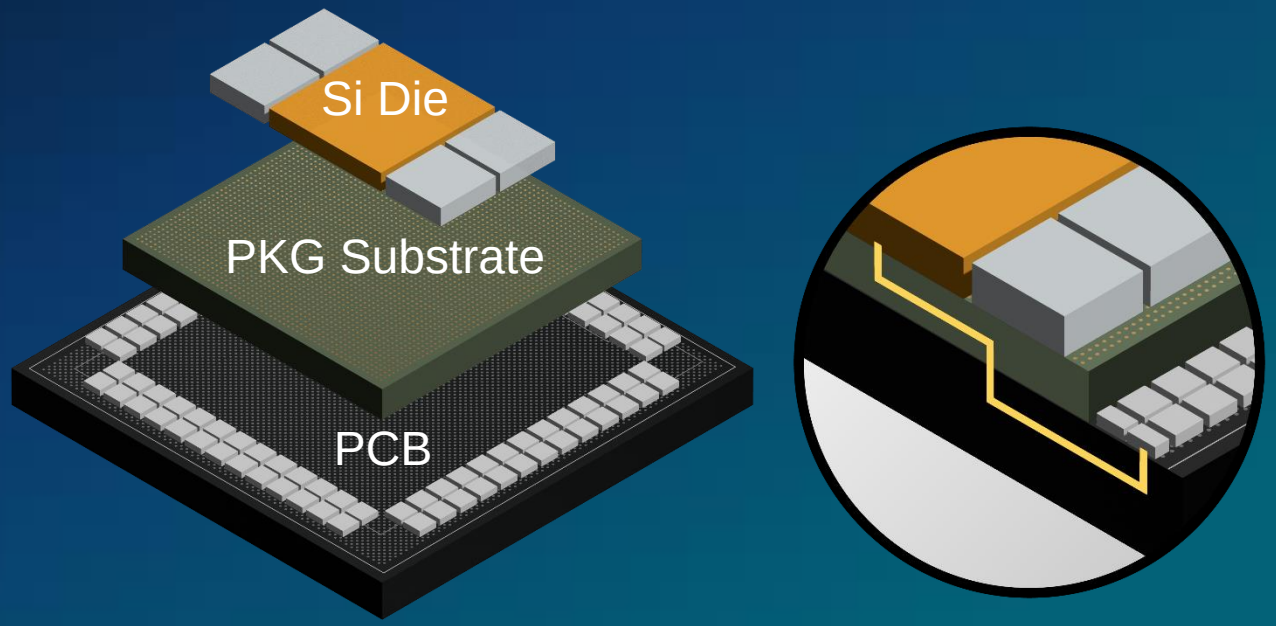
PDN Challenges:

- Design Complexity
- PDN Losses
- Increase in Total Number of Discretes

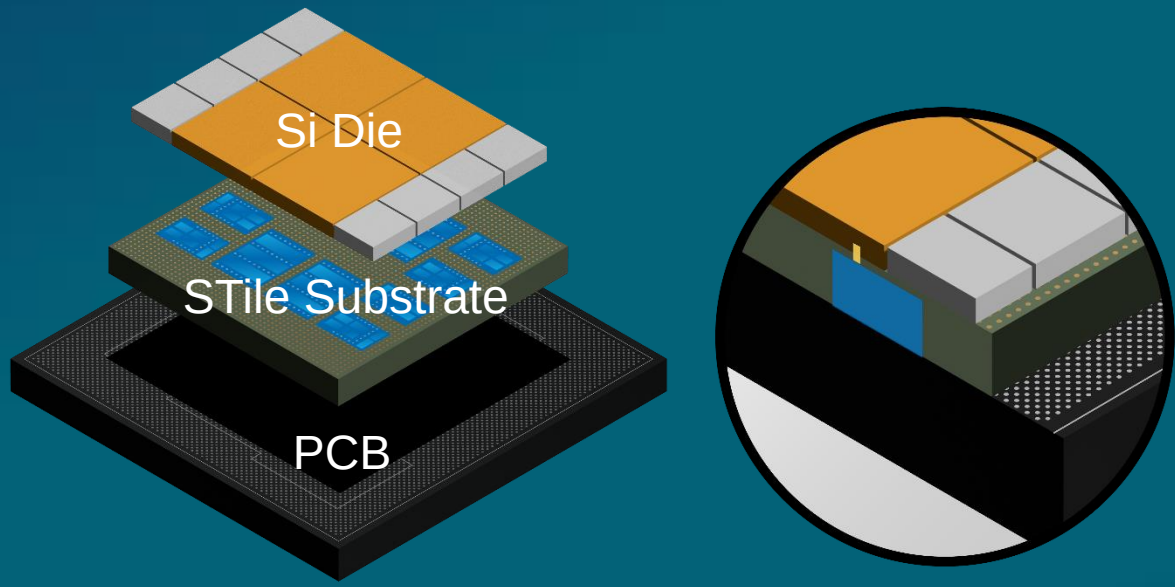
Saras STile™ Technology

CURRENT STATE

State of Art

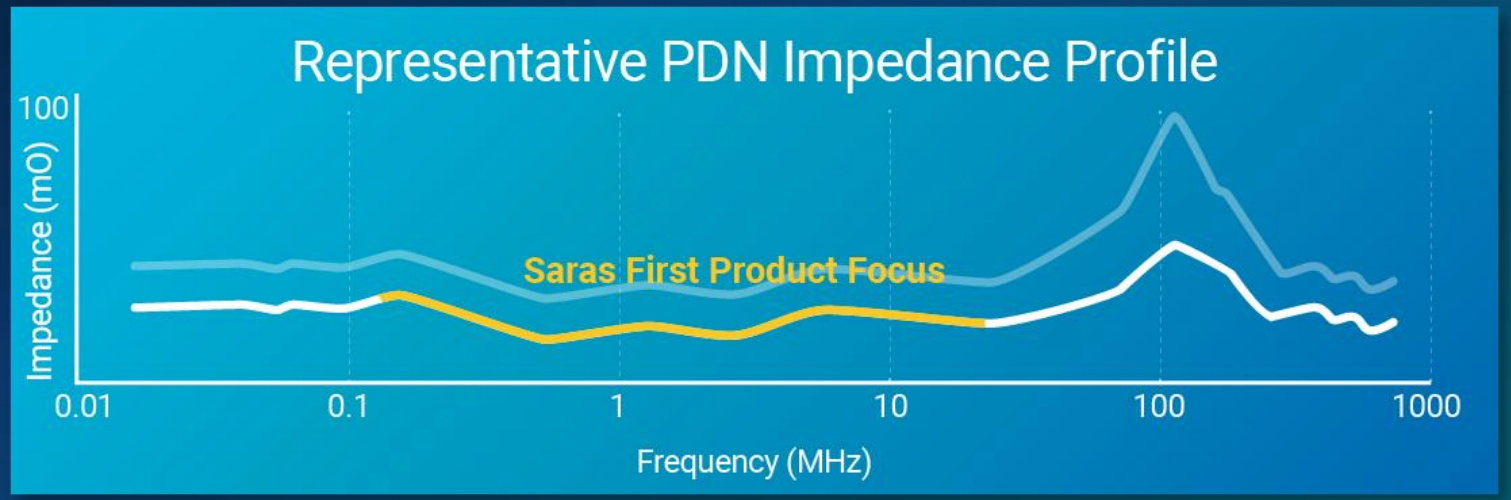


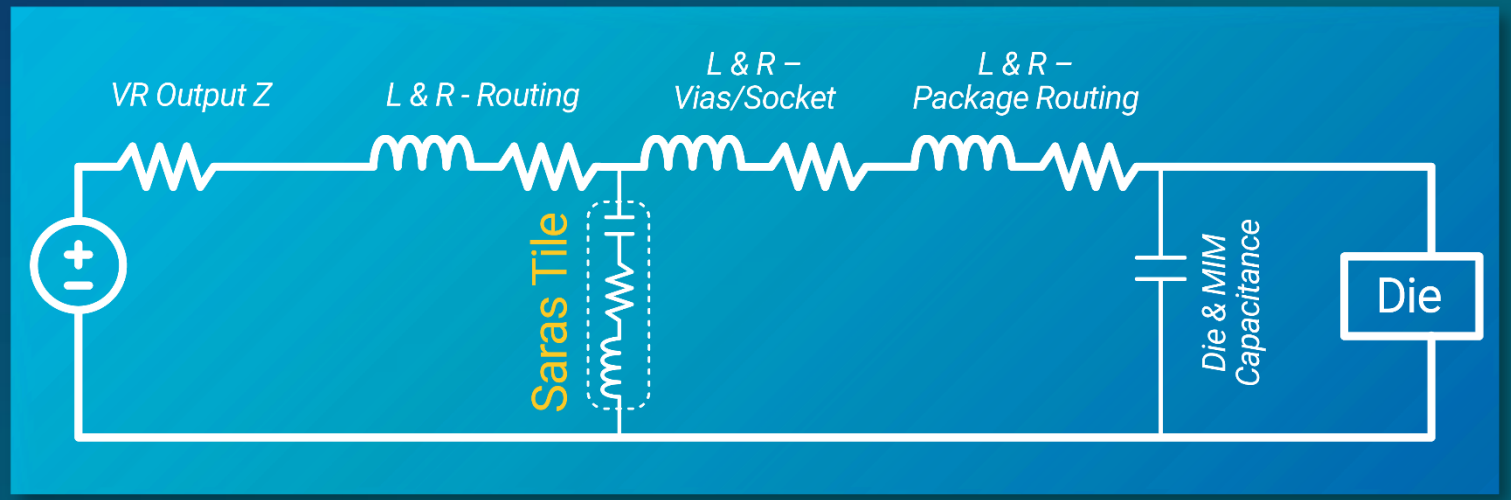
- Hundreds of Passives Required
- Long power path routing lengths
- Rising Si to Package Area Ratio



- Function Specific STiles
- Vertical Power Deliver
- No Limitation from Passive Components

Product Application Focus

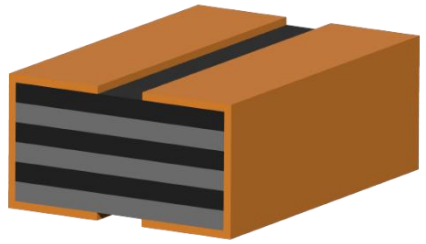




STile PDN Benefits

- Design Simplicity
- Higher Performance
- Larger Area Real Estate for Silicon

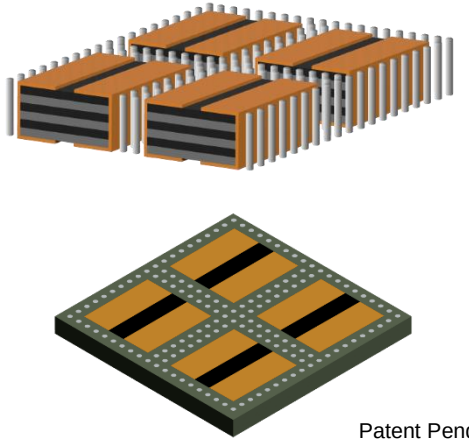
Saras Product Offerings



Capacitor Element

- ► Stacked Capacitive Element
- ► Formfactor and Performance Customizability

Development 2023

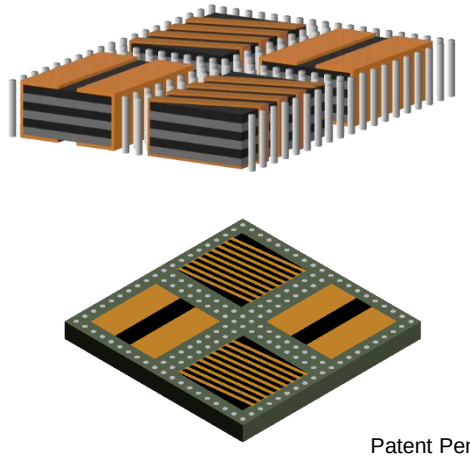


Patent Pending

STile™ Technology

- ► Multi-domain Capacitor
- ► Single Integrated Device

Product 2024



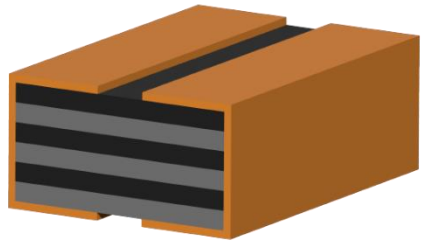
Patent Pending

Integrated Voltage Regulator

- ► Integration of L + C
- ► Enable advanced PDN Roadmap

Introduce 2025

Saras Product Offerings



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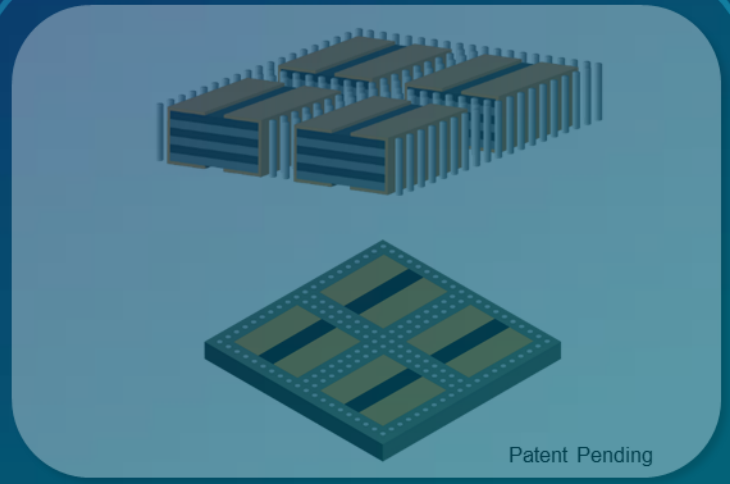
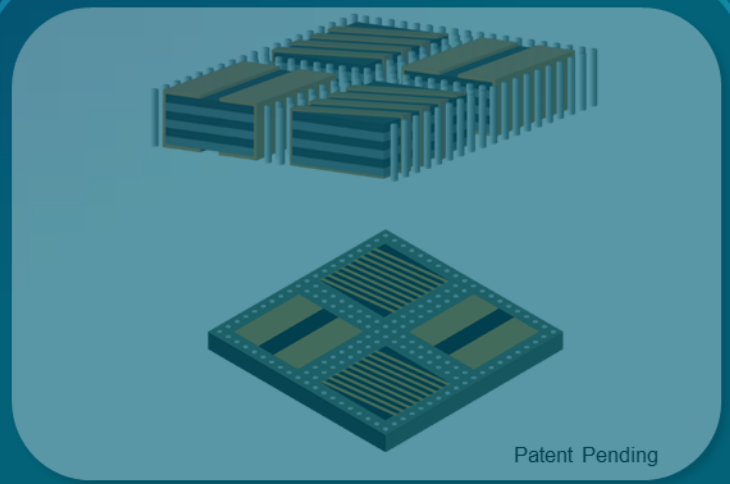


STile™ Technology

- ► Multi-domain Package Capacitor
- ► Single Integrated Device

Product 2024



Integrated Voltage Regulator

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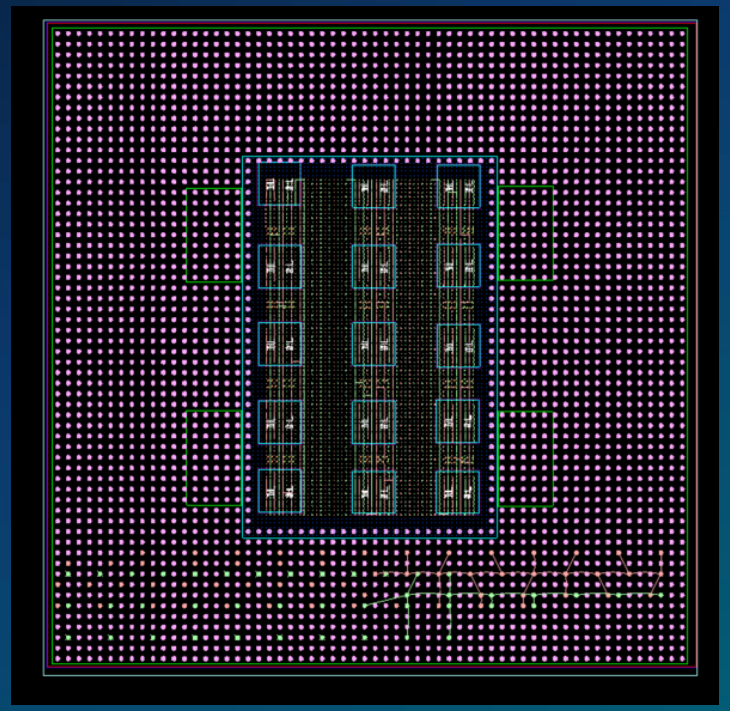
- ► Enable advanced PDN Roadmap

Introduce 2025

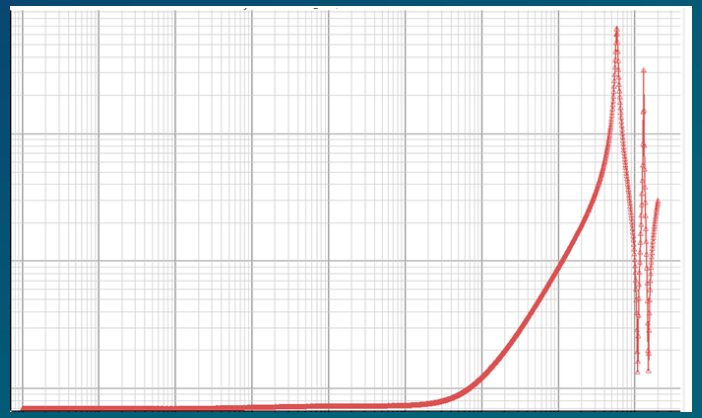
Device Performance

Capacitive Cell Size Examples		Cell A	Cell B	Comment
Dimension XY (mm)		4.0 x 4.0	4.0 x 7.0	Additional customization available upon request
Min. Capacitance (uF) @ 100kHz	800 µm high	24 - 64	42 - 112	1.5 µF/mm^2 – 4.0 µF/mm^2. Higher Density on Request
	1000 µm high	32 - 72	56 - 126	2.0 µF/mm^2 – 4.5 µF/mm^2. Higher Density on Request
	1200 µm high	40 - 80	70 - 140	2.5 µF/mm^2 – 5.0 µF/mm^2. Higher Density on Request
R_s @ 100 KHz (mΩ)		15	15	Maximum ESR
ESR @ S.R.F. (mΩ)		10	10	Maximum ESR
Frequency Range		<30 MHz		Dictated by Resonance
Operating Temperature Range		0^{o}C – 125^{o}C		
Capacitance Variation versus Temperature		<10%		Preliminary Reliability Data
Rated Voltage		4V		Higher RV possible
Capacitance Variation versus RVDC		<5%		Limited Test Data Available

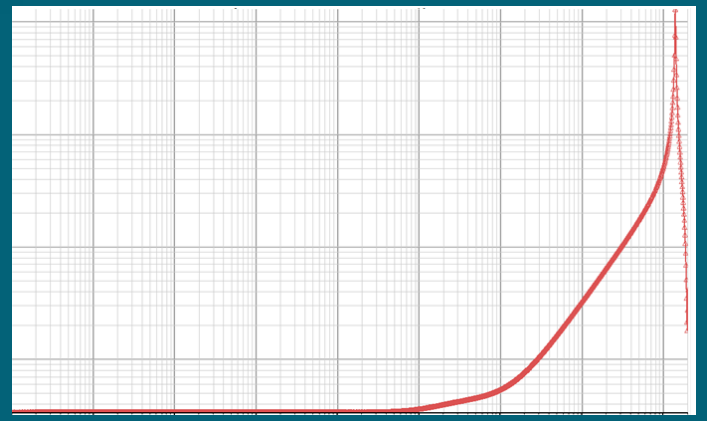
System Level Model | Preliminary



SIEMENS



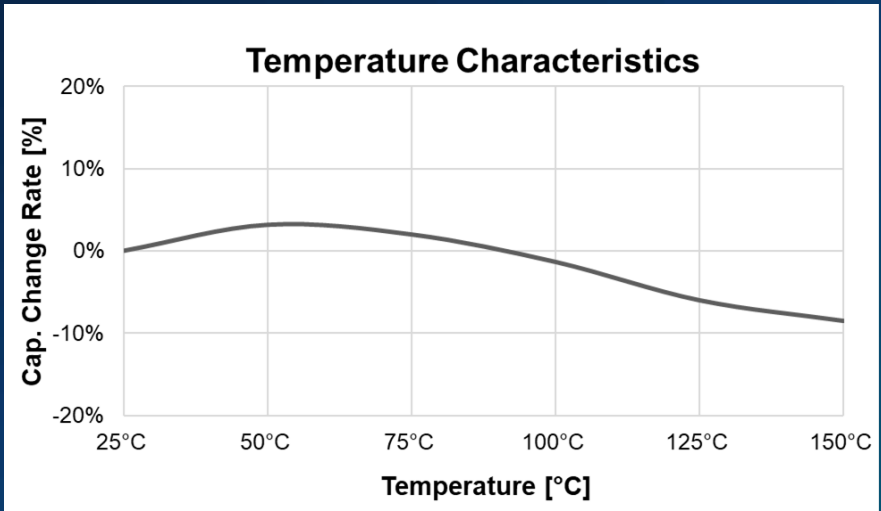
- No embedded STile™

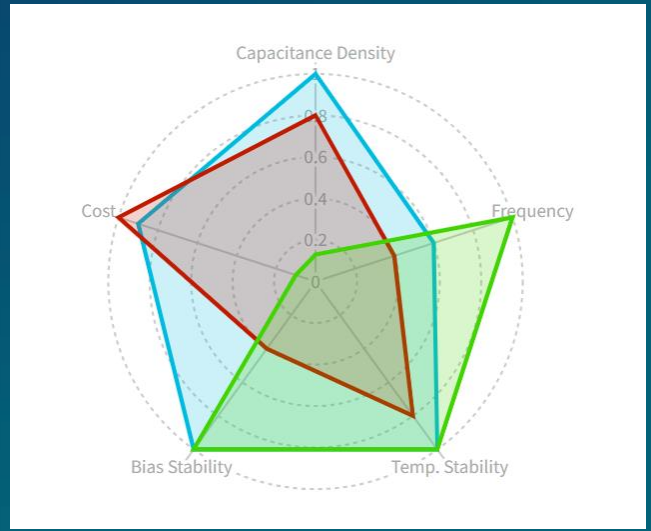


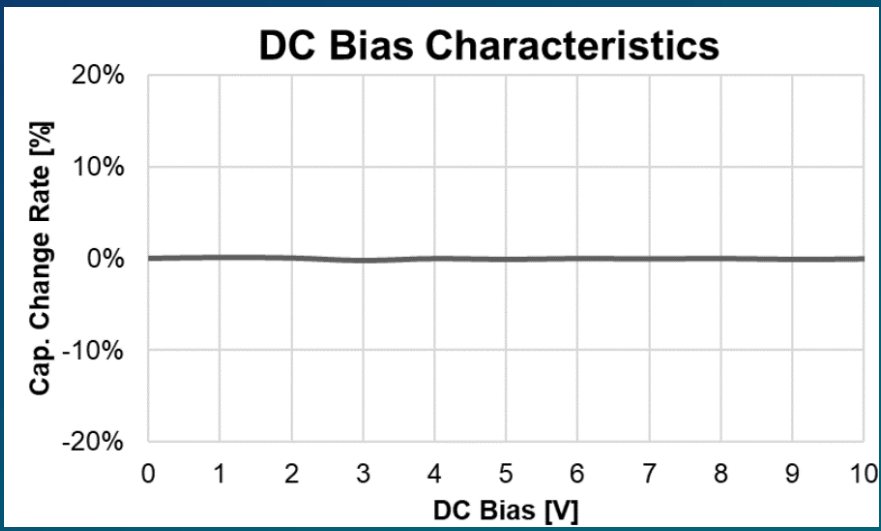
- With Embedded STile™

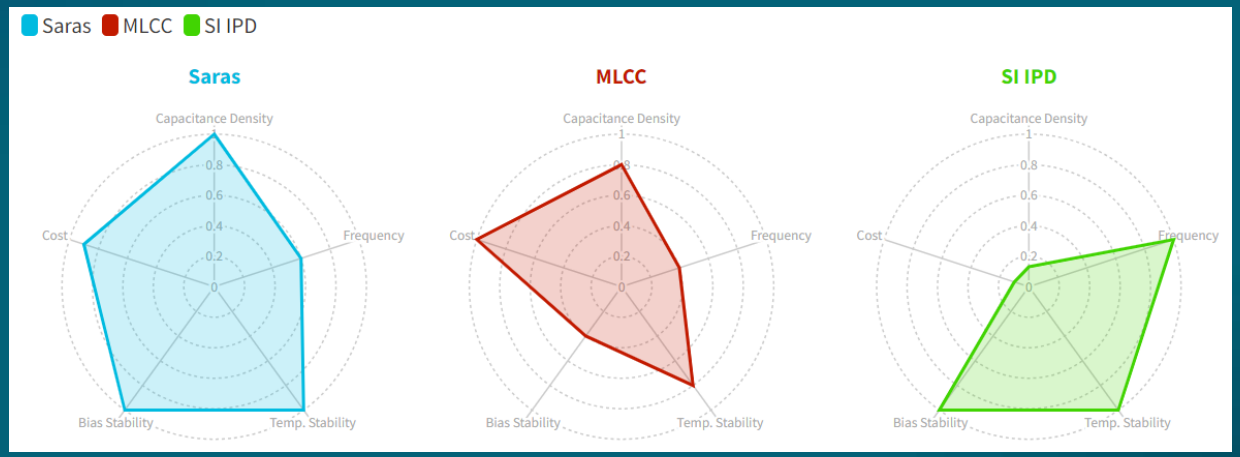
48% Reduction in System Level |Z|

STile Stability and Positioning









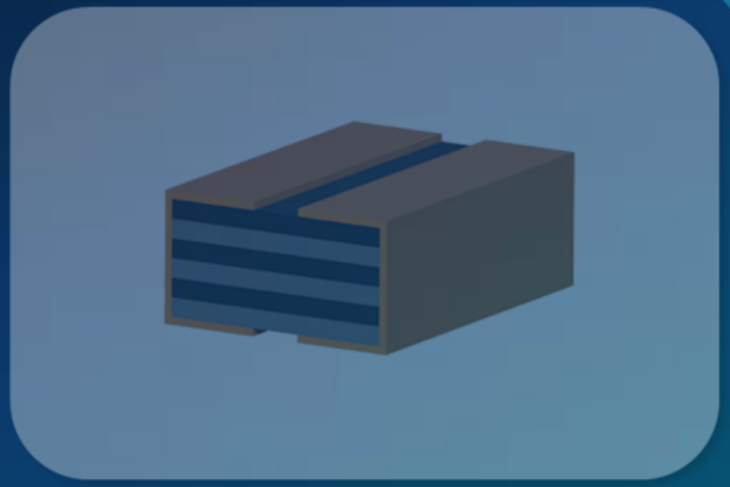
Saras Capacitor Temperature and Bias Stability superior to MLCC

Capacitor Reliability Testing

Test	Test Conditions	Test Targets	Test Duration	Results
HTS	150°C	500 Hours	500 Hours	**<10% Change in C_s/R_s**
Bias Test	4V @ 105°C	150 Hours	720 Hours	**<10% Change in C_s/R_s**
TCG	-40°C to 125°C	1000 Cycles	1200 Cycles	**<5% Change in C_s/R_s**
T/H-1	85°C / 85% RH	500 Hours	1000 Hours	**<10% Change in C_s/R_s**
T/H-2	110°C / 85% RH	100 Hours	800 Hours	**<5% Change C_s/R_s**
bHAST	4V @ 110°C / 85% RH	24 Hours	48 Hours	**<5% Change in C_s/R_s**

- Capacitor stability through extended reliability test conditions

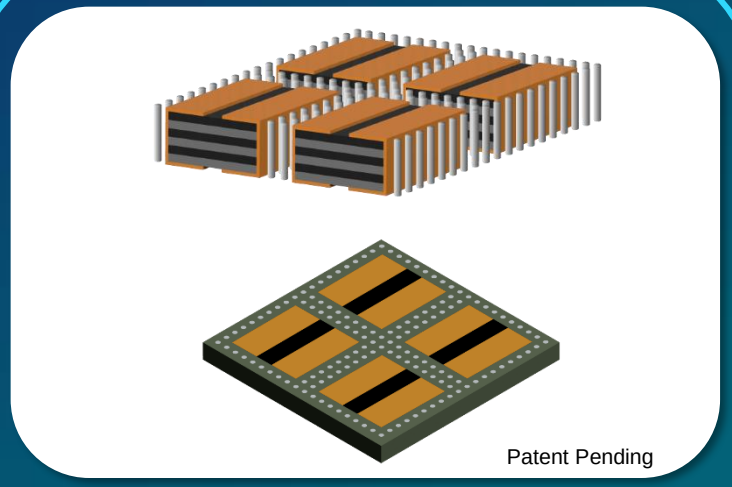
Saras Product Offerings



Capacitor Element

- Stacked Capacitive Element
- Formfactor and Performance Customizability

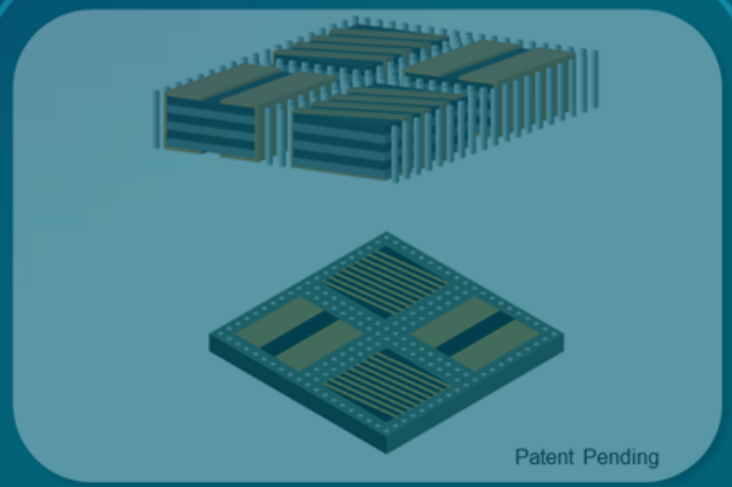
Development 2023



STile™ Technology

- Multi-domain Package Capacitor
- Single Integrated Device

Product 2024

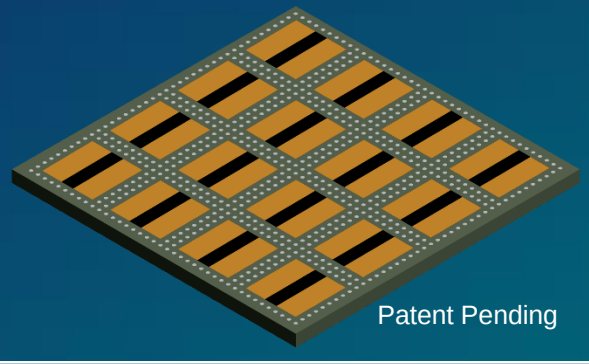
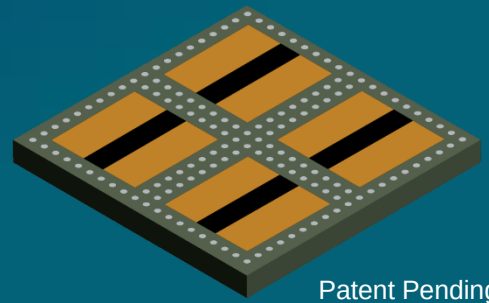


Integrated Voltage Regulator

- Integration of L + C
- Enable advanced PDN Roadmap

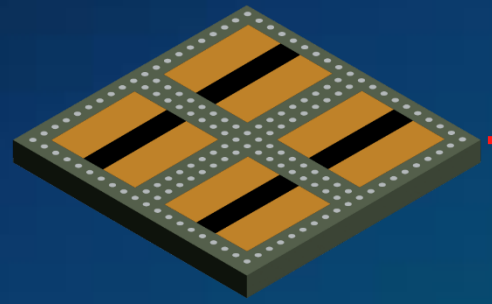
Introduce 2025

Saras Development STiles™

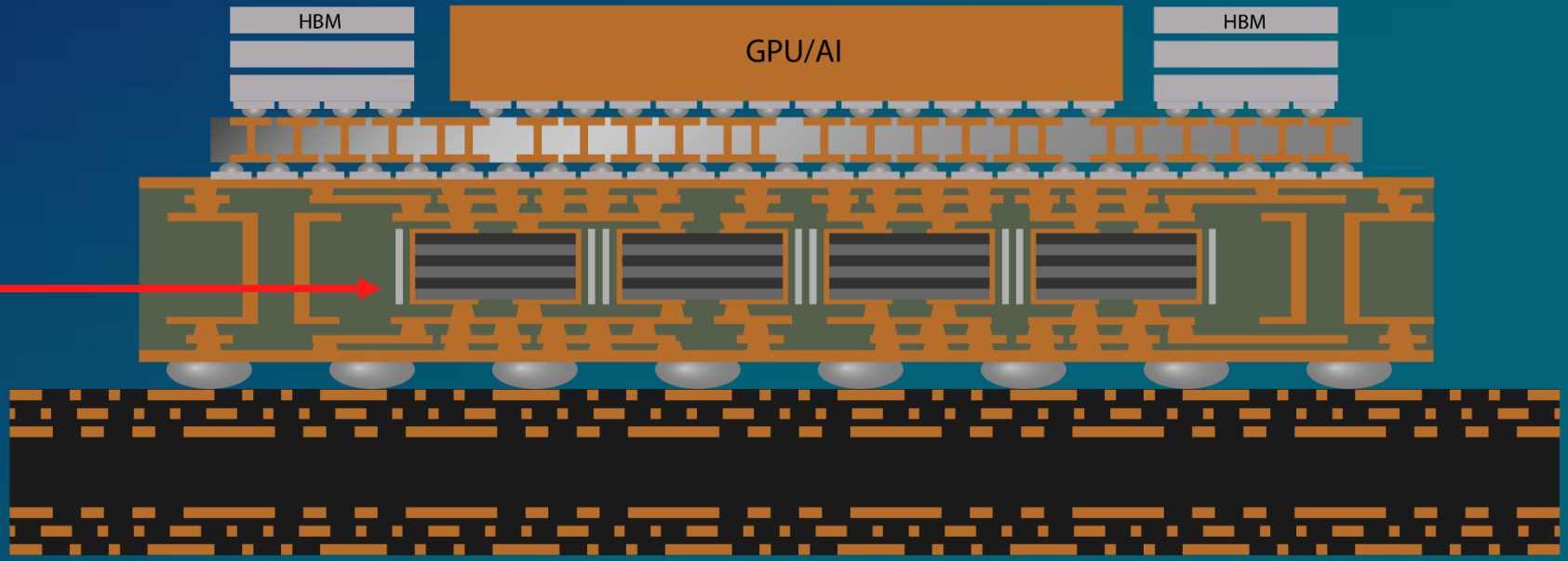
	Saras TV1.1	Saras TV1.2
	 Patent Pending	 Patent Pending
Tile Size (mm)	21 x 21 x 1.2	11 x 11 x 1.2
Total Cap Domains	16 (4x4 mm cap domains)	4 (4x4 mm cap domains)
Total Capacitance (µF)	640 - 1,280	160 - 320
Number of Thru Vias	1472	240

- Non-uniform Capacitor Sizing Possible

Package / System Integration Options

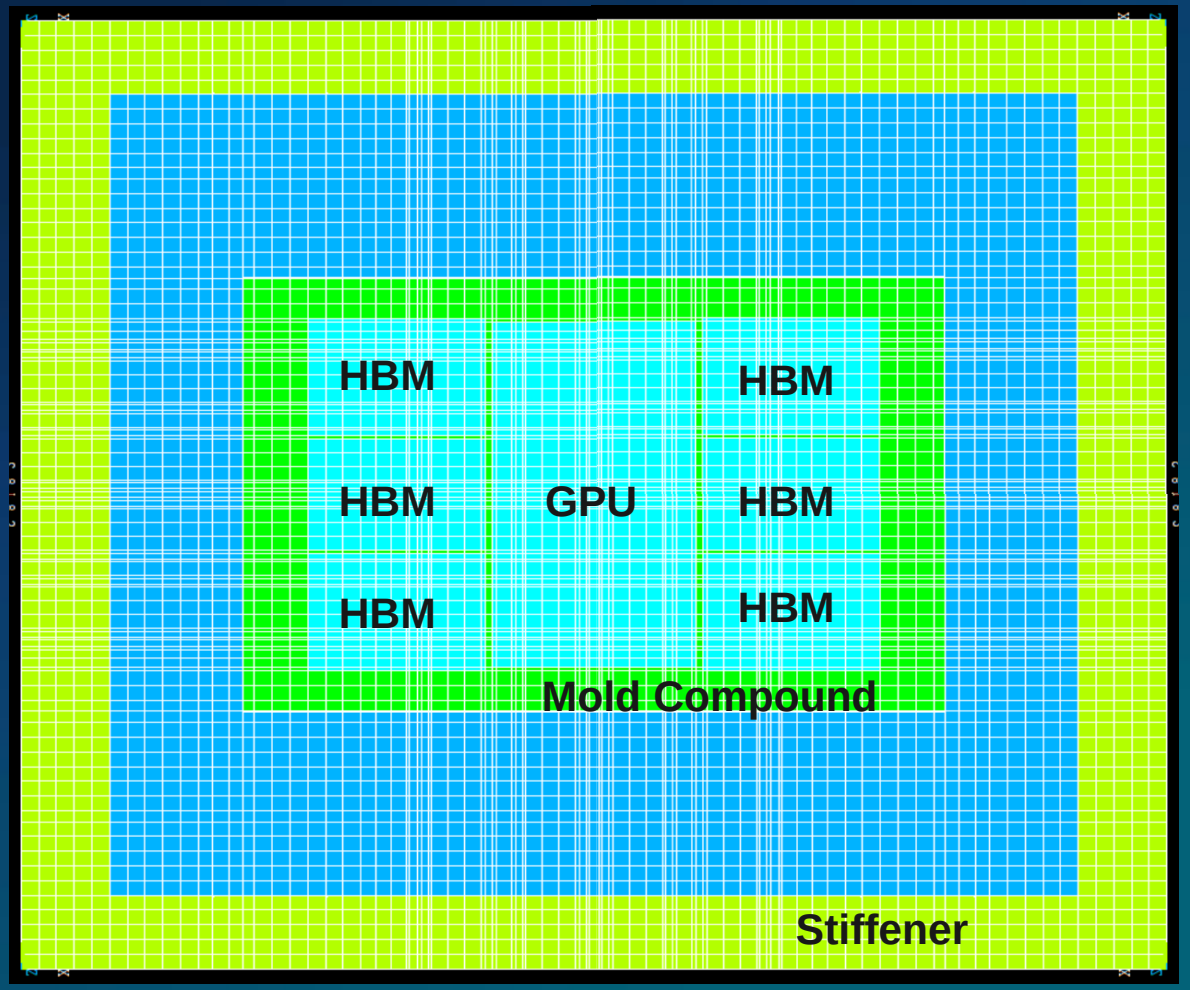


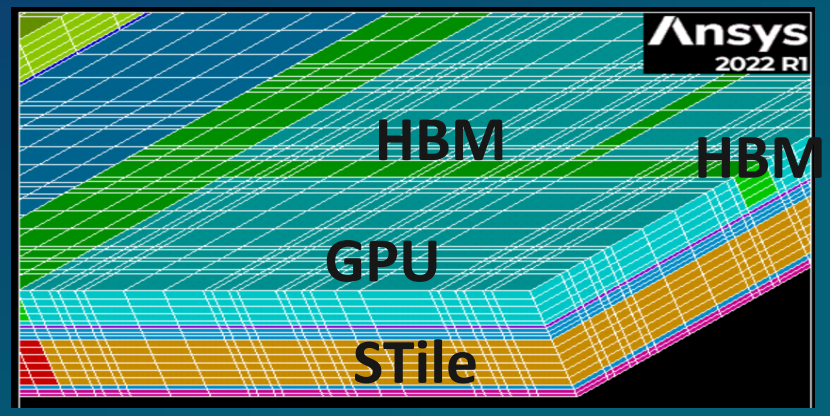
Patent Pending

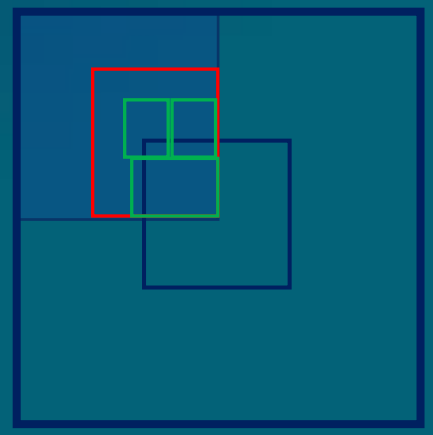


- Primary Development focus to embed STiles inside of the Organic Package Substrate
- Alternative embedding options available
- Pass through Via's ensure sufficient DC return paths

Thermomechanical Modeling Setup

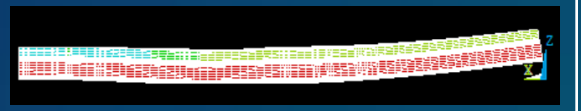
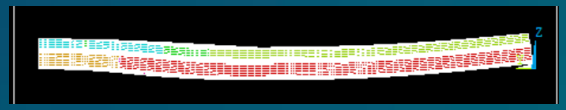
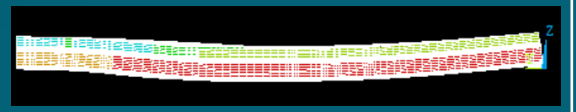
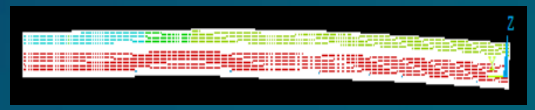
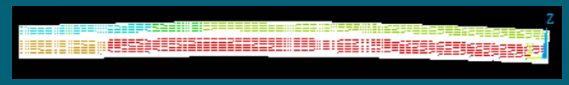
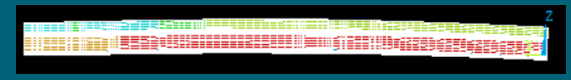






- Impact of embedded STile on Substrate
- ANSYS FEA Analysis on embedded STile Devices
- How does the Package Behave during Reflow?

Modeling Results

Conditions	No STile	21mm x 21mm STile	4 – 11mm x 11mm STiles
195°C ⟶ 20°C	 1x Warpage	 0.76x Warpage	 0.72x Warpage
195°C ⟶ 260°C	 1x Warpage	 0.85X Warpage	 0.82X Warpage

- Presence of STile shows reduction in warpage

Conclusions

- Power delivery challenges require new innovations beyond Silicon
- The Saras STile addresses these challenges by:
  - Best in class Capacitance density and stability
  - Customizable Vertical Power Delivery Solution
  - Supports increased Si functionality
- STile Production in 2H of 2024
- Introduction of Inductor and Capacitor STile by 2025

Powering the Future

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