IMAPS 20th Device Packaging Conference | March 18-21, 2024 | Fountain Hills, Arizona

ASE

Advanced Mechanical Analysis Workflow for Chiplets Integration Predictive Design

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Outline

- Introduction
  - Semiconductor Industry Trend
  - Chiplets integration motivation and design challenges
- Advanced Design Ecosystem and Mechanical Analysis for Chiplets Integration
  - Design consideration
  - Mechanical analysis and simulation flow
- ASE Integrated Design Ecosystem for Chiplets Integration
  - Cases studies
- Conclusion

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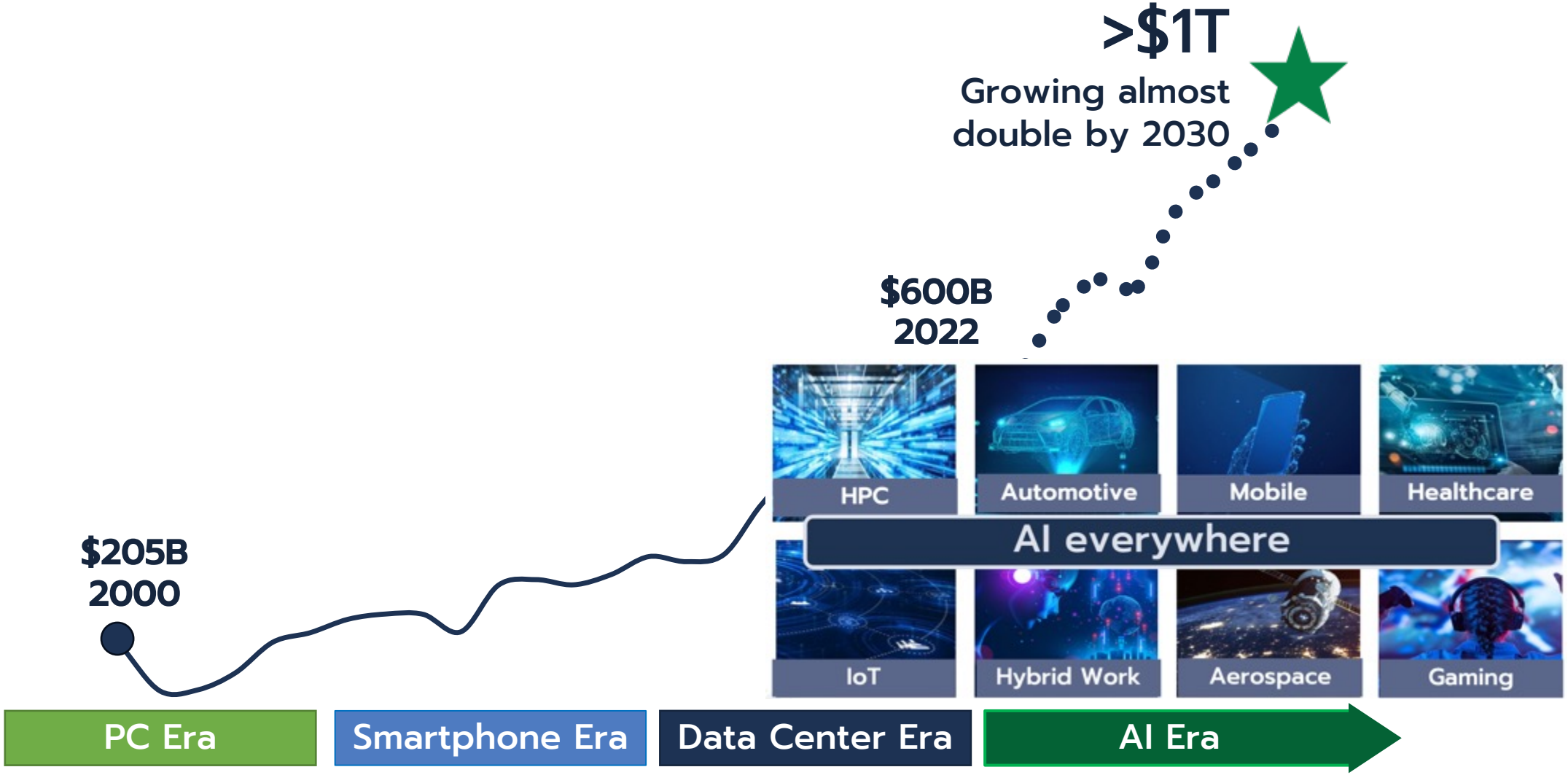
Semiconductor Industry Landscape



Source: Gartner 2023

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Scaling for AI Era

MORE THAN MOORE

Market demand for AI performance is faster than Moore's Law doubling transistors every 18 months

- AI/ML performance has increased nearly 6.8x~11x in the past two years from 2021~ 2022 that outstrips more than Moore's Law

Source: AMD 2023

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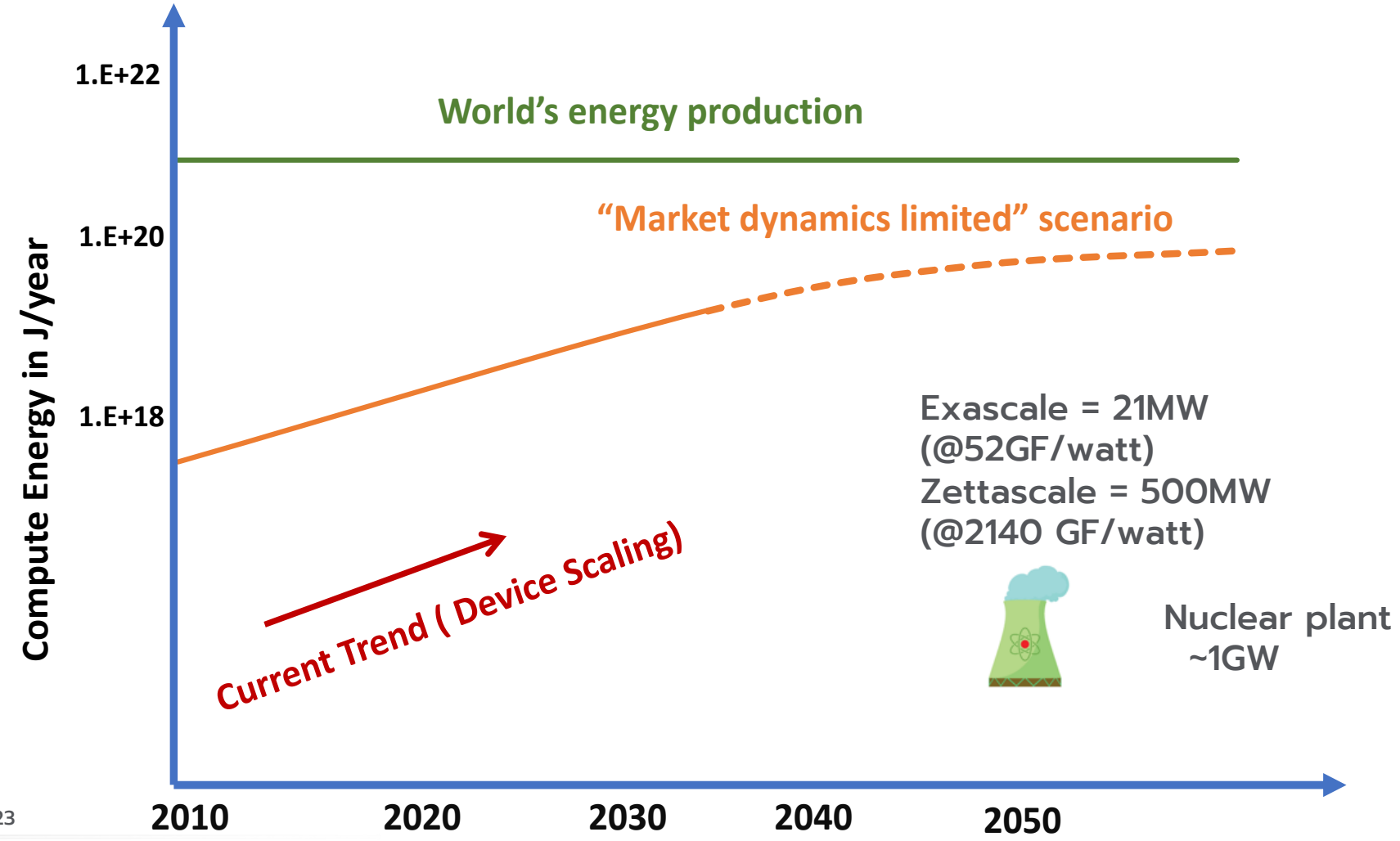
Compute Requirements Exploded in AI Era



Source: AMD 2023

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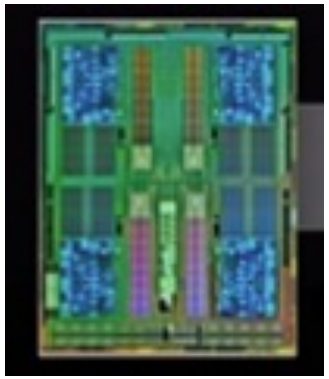
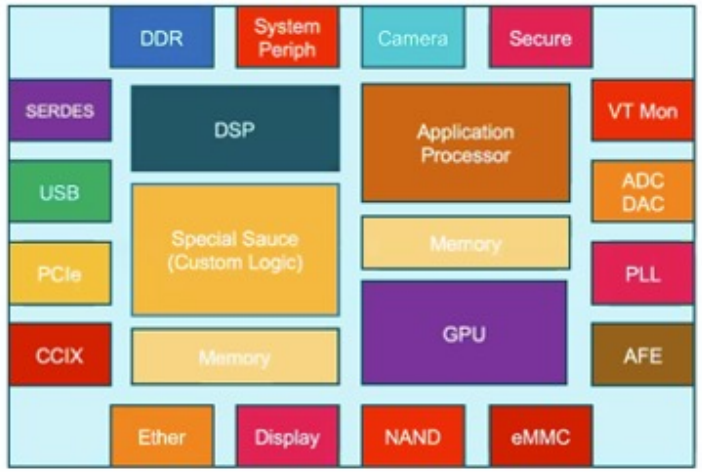
Chiplets and Heterogeneous Integration



Monolithic SoC



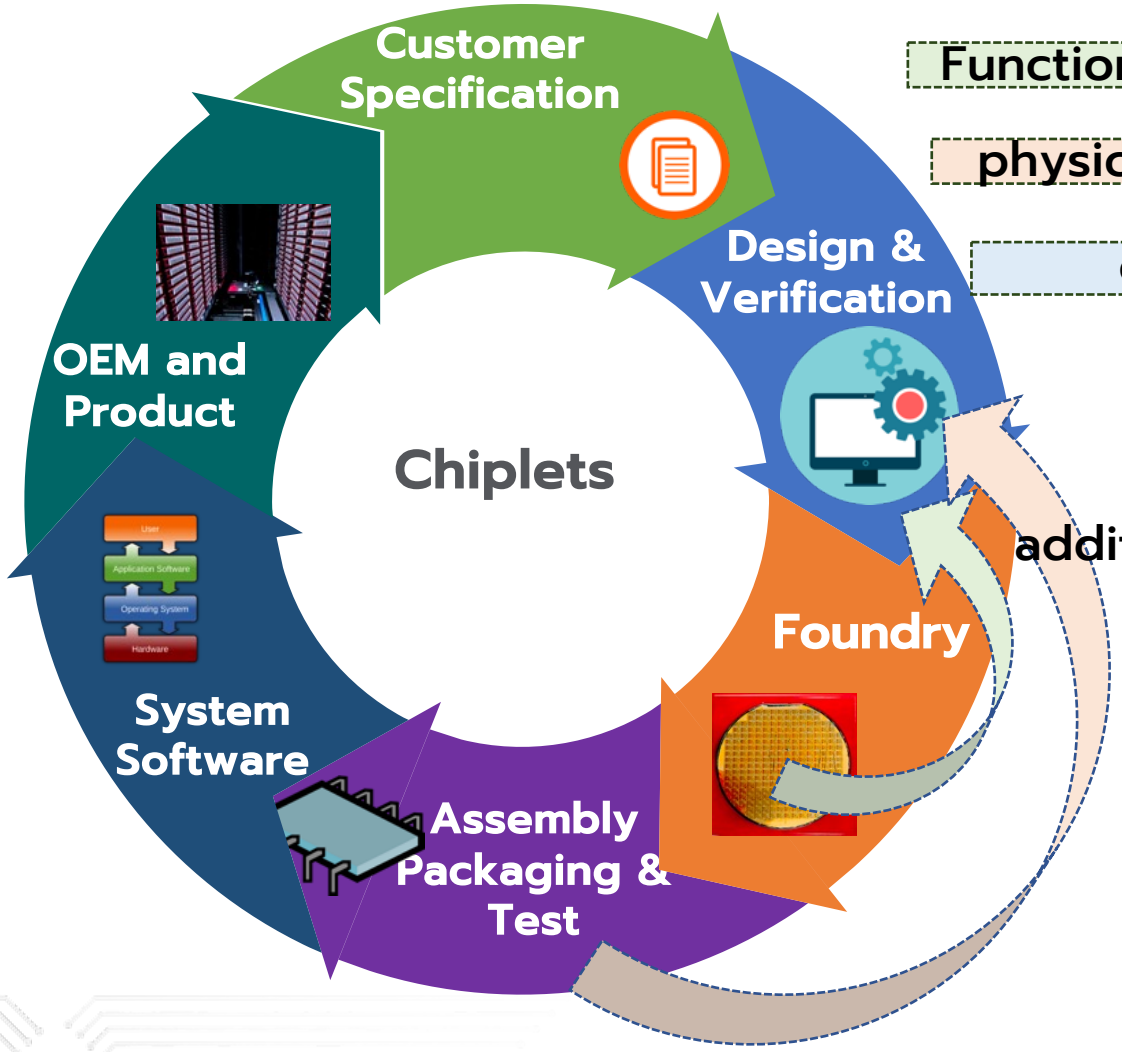
Modularized SoC (Chiplets)

Drivers for on-package Chiplets

- ❑ Mix & Match systems--*Enable construction of Different Si Nodes*
- ❑ Reuse IPs—Package becomes new System-on a Chip (SoC)
- ❑ System flexibility--*Processors, accelerator*
- ❑ Performance optimization--*Low latency & high BW*
- ❑ Time to Market
- ❑ Low Cost—Enable optimal process technology; Smaller for better yield

6

Chiplets – More Complex Workflow



Functional modularity

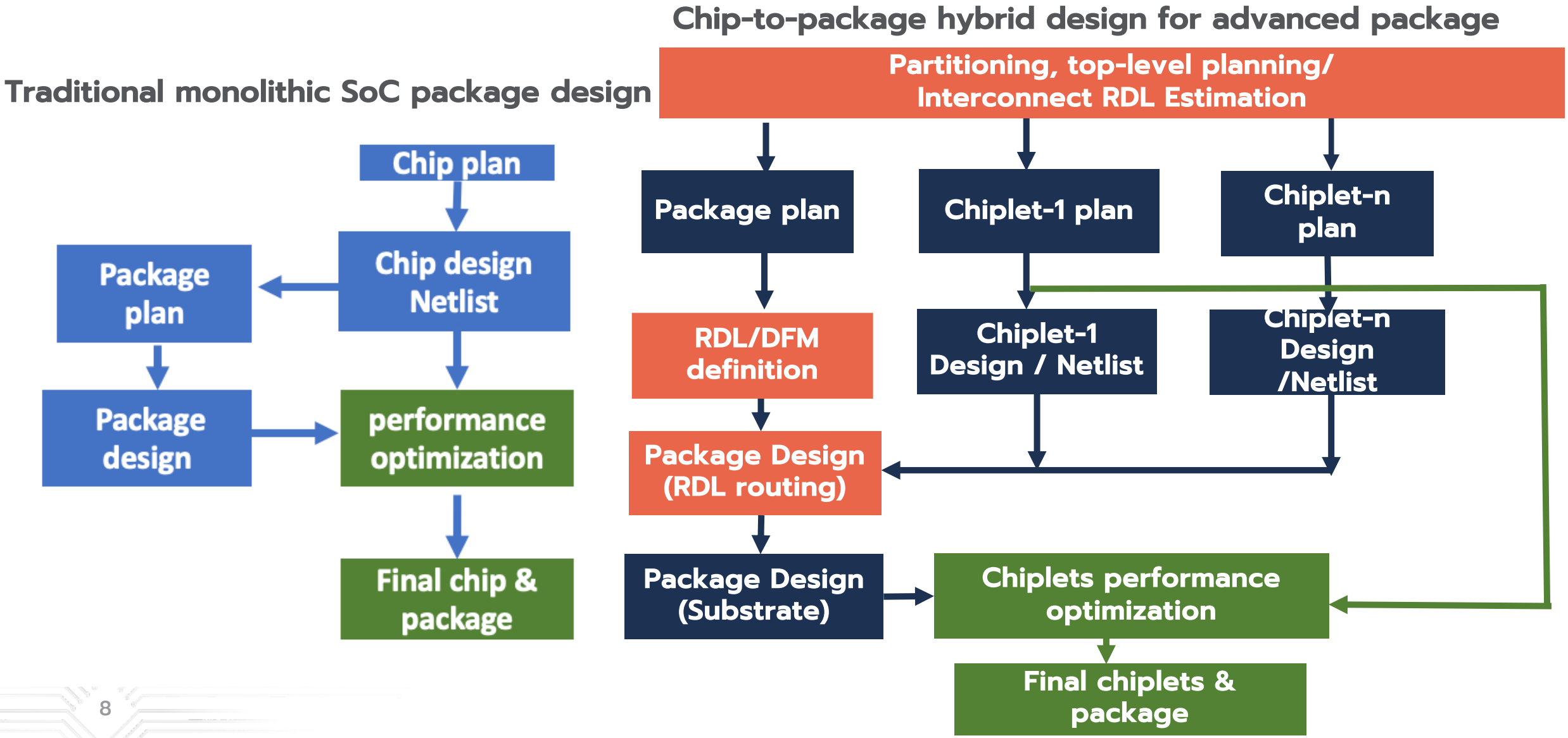
physical modularity

codesign

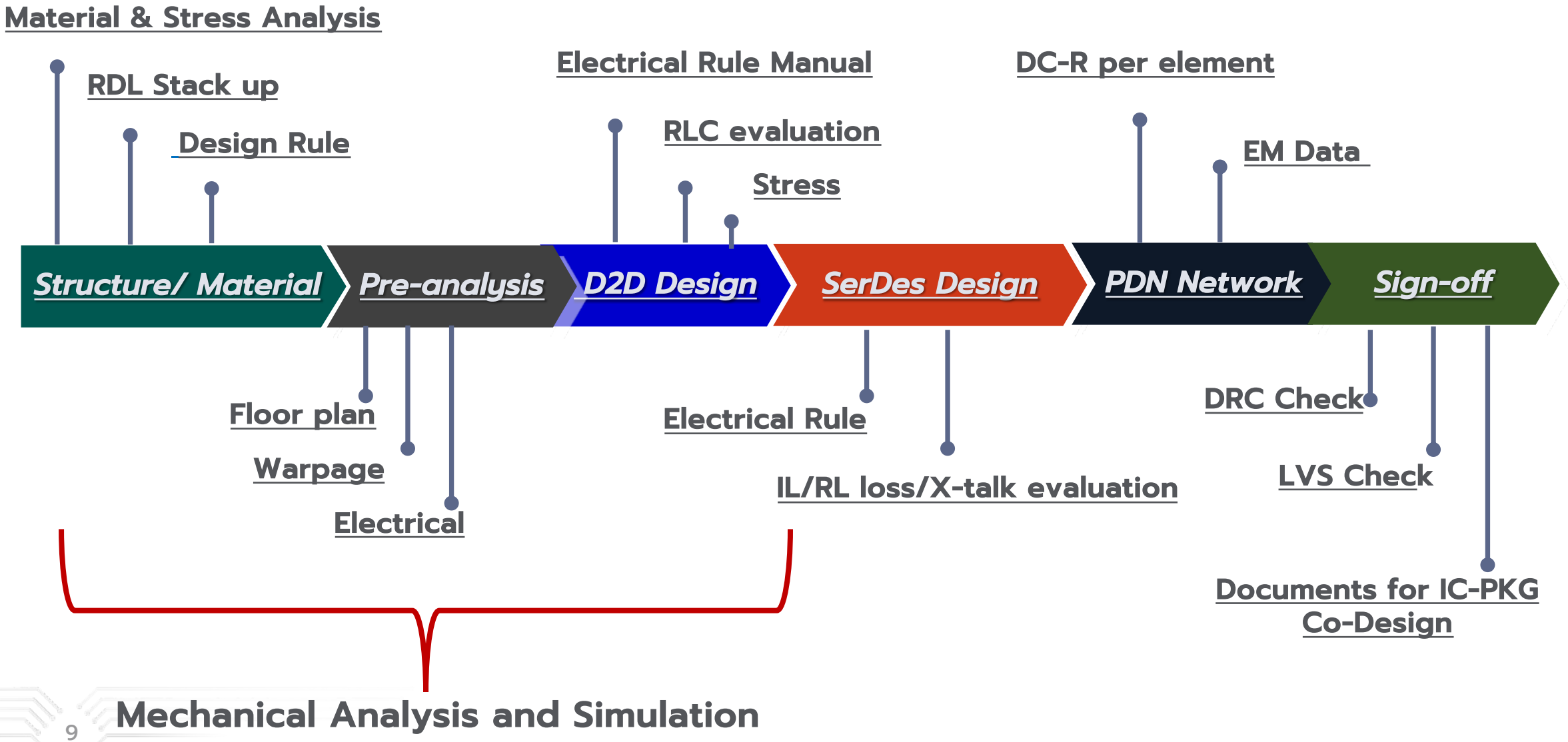
Key factors for more complex

- Functional modularity
- Physical modularity
- Interconnect
- Packaging
- Test and operations
- Supply chain

Chip-Package Co-Design Consideration

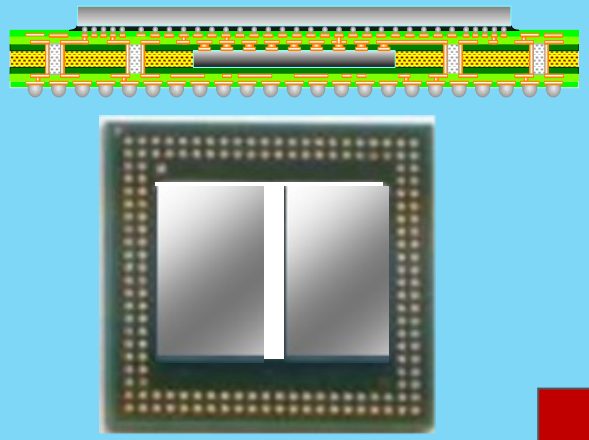


Chip-to-package hybrid design planning flow

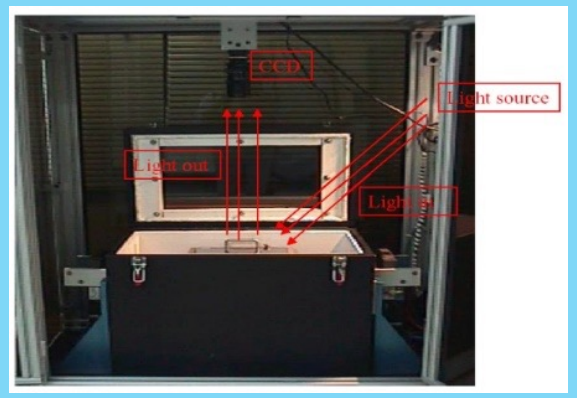


Mechanical Analysis and Simulation

Measurement Data

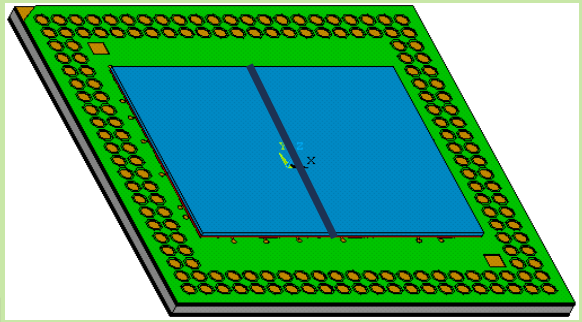


FCBGA

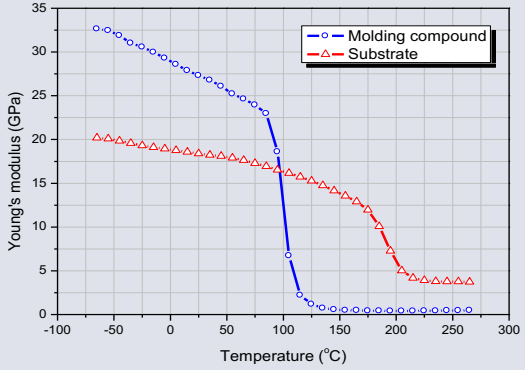


Shadow Moiré measurement

Simulation Data

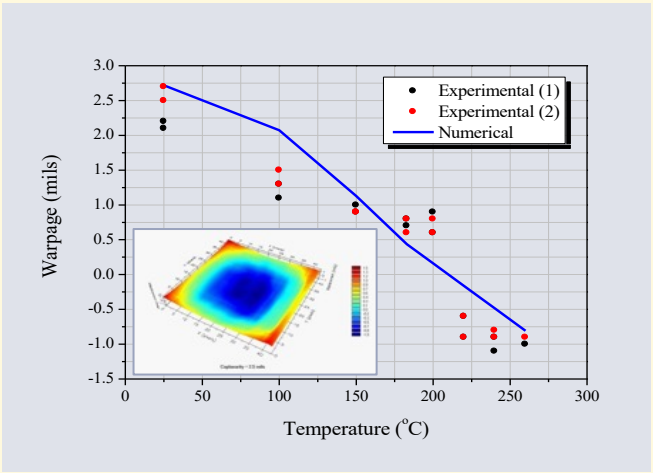


FEM modeling



Material property measurement

Validation & Optimization



Validation between experimental and numerical data

Optimize Design

Mechanical Analysis Flow for Chiplets Integration

Input Parameters (Pre-Assembly/Test):

1. No of Dies
2. Die Size
3. Die Thickness
4. Die Location
5. Stack/Non-Stack
6. Substrate
7. Any embedded die, ex: DTC
8. CTE
9. Tg
10. Poisson's ratio
11. Modulus
12. RDL - Metal Density
13. KOZ – Keep out zone
14. Mix and Max Technology
15. Micro bumps/Pillars
16. Hybrid Bonding
17. TSV

STRUCTURE

MATERIAL

Design

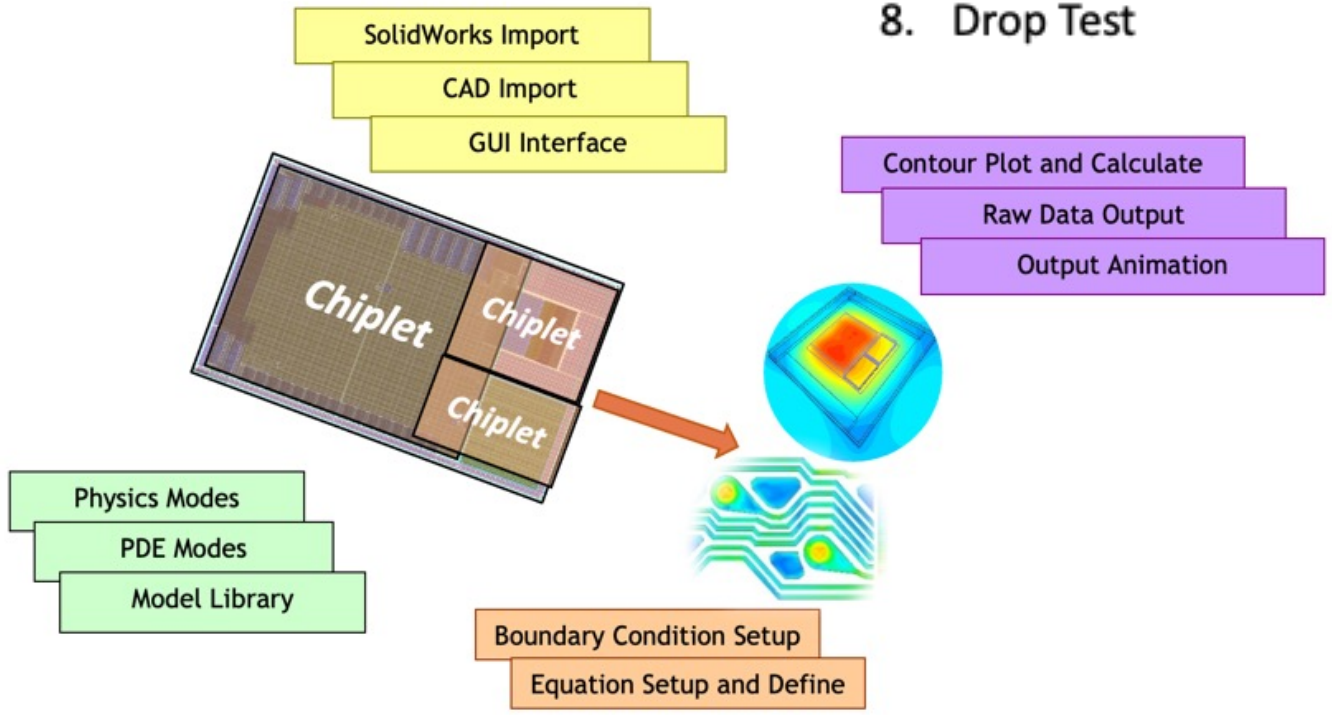
Interconnect

Input Parameters (Post - Assembly):

1. Bump pitch
2. Stiffener Ring
3. Heat Spreader
4. BSM
5. Preform TIM
6. BLT
7. Flux Boundary

Output Parameters:

1. Structure, DFM, DFT,
2. Stress Test
3. Warpage Trend
4. Temperature Cycling
5. Biased/Unbiased HAST
6. MSL
7. Vibration
8. Drop Test



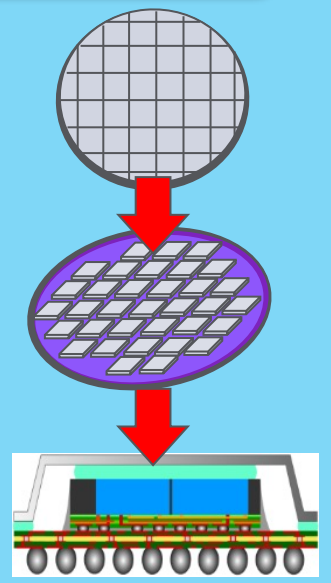
Impact of Advanced Mechanical Analysis and Simulation

Manufacturing Process

Incoming Wafer

FEOL

BEOL



Cycle Time

60 Days

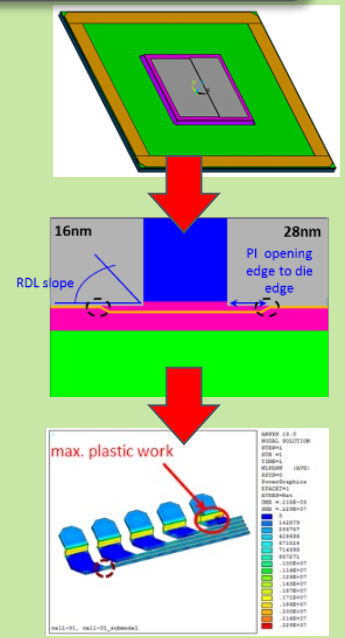
VS

Simulation Process

Input

Solution

Output



Cycle Time

1 Day

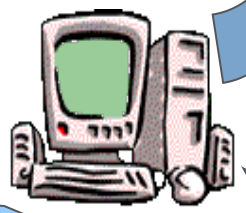
ASE Auto-Stress Simulation Platform

1

Remote Web Terminal
Design parameters key-in

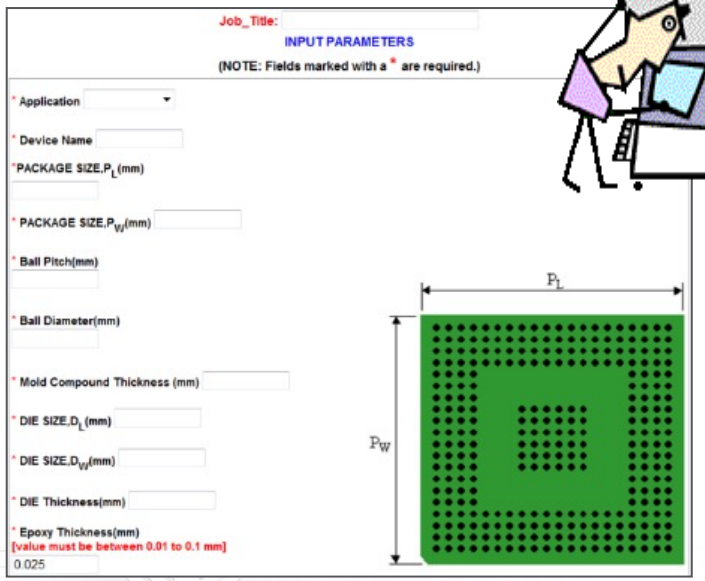
3

ASE e-Mail System
Automatically sending results from e-Stress Simulator server to customers.



e-Stress Simulator
Server Stress calculation
using ANSYS
based on finite
element methods

2



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DOFU BGA STRESS SIMULATION REPORT FOR ASE KH

Simulation Models

1.General description :

The geometrical parameters of components of the DOFU BGA are listed in Table1.

Package conditions	
Package type	DOFU BGA
Package size (mm x mm)	10.00x10.00
Epoxy thickness (mm)	0.025
Mold thickness (mm)	0.70
Substrate thickness (mm)	0.21
Compound type	CEL-9200HF10
Epoxy type	QMI-529
Simulation conditions	
Stress-free temperature	175 degree C (Curing temperature of compound)
Temperature loading	175 degree C to 25, 260 degree C

2.Finite Element Modeling :

We perform 3-D finite element analysis on the DOFU BGA package. A quarter symmetry model is built up due to symmetry. The package is properly constrained to maintain numerical stability. The analysis is carried out using ANSYS v.10.0. The meshing region and the detailed structural outline is shown in Figure 1, where

Figure 1 : Layout of modeling region of the DOFU BGA.

2.Potential of Die Crack

Since silicon is a brittle material having low resistance to the tensile stress, the 1st principal stress is a proper index in examining the potential of possible die crack. Cracking may occur on the die if the tensile stress is large enough to propagate microcrack preexisted in the die. However, if the principal stress is negative, i.e., compressive, the die is immune to cracking. Figure 3 shows the 1st principal stresses on the die at 25 and 260 degree C, it is 15.21 and 1.59 MPa,respectively. It is notice that the 1st principal stress at 25 degree C is greater than that at 260 degree C.

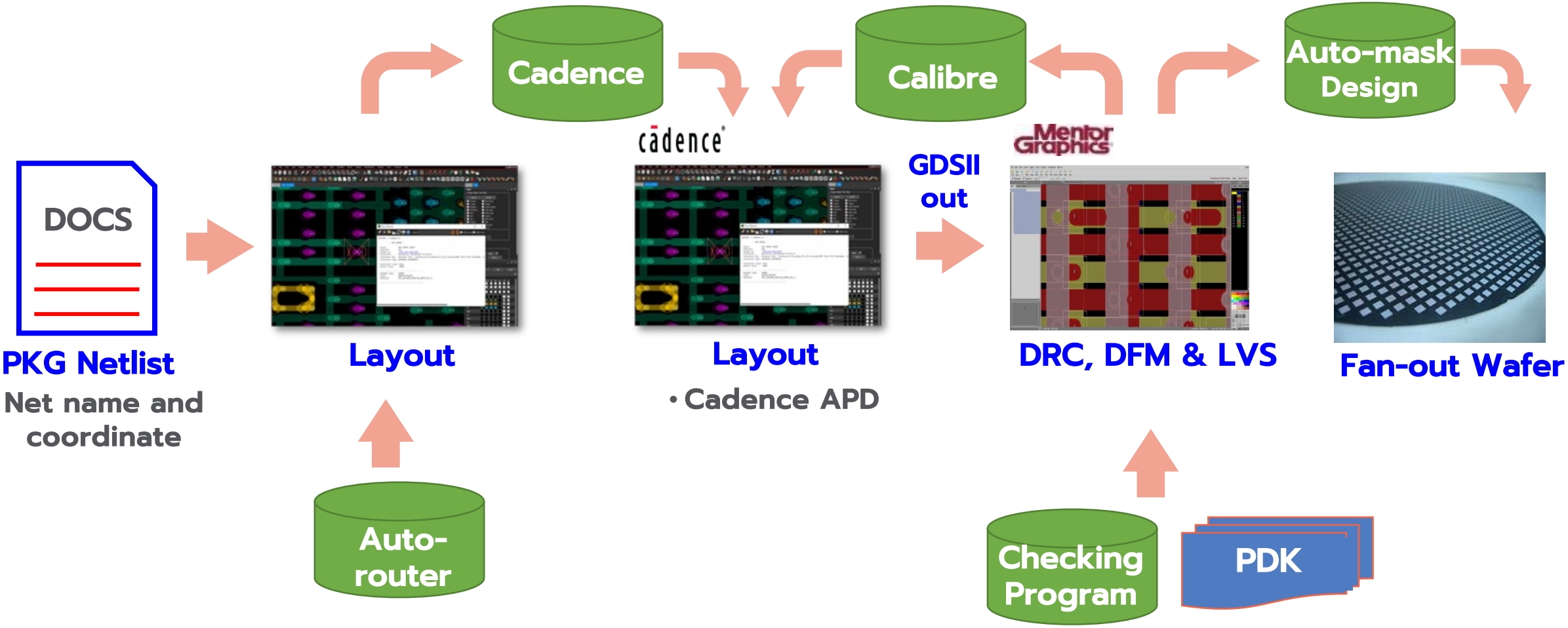
(a) (b)

Figure 3: 1st Principal stresses on the die at (a) 25 and (b) 260 degree C. (Unit : Pa)

Table 3: Maximum 1st principal stresses of die for different temperatures.

Temperature(degree C)	Max. Principal stress(MPa)
25	15.21
260	1.59

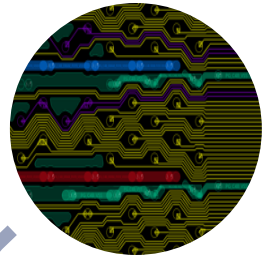
Integrated Design Ecosystem (IDE)



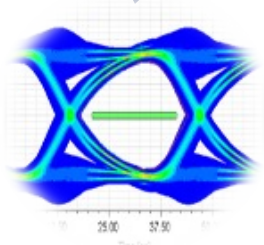
ASE Design Turnkey Solution

Toolbox Integration For FOCoS CZ

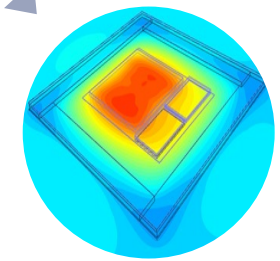
FORDL Layout

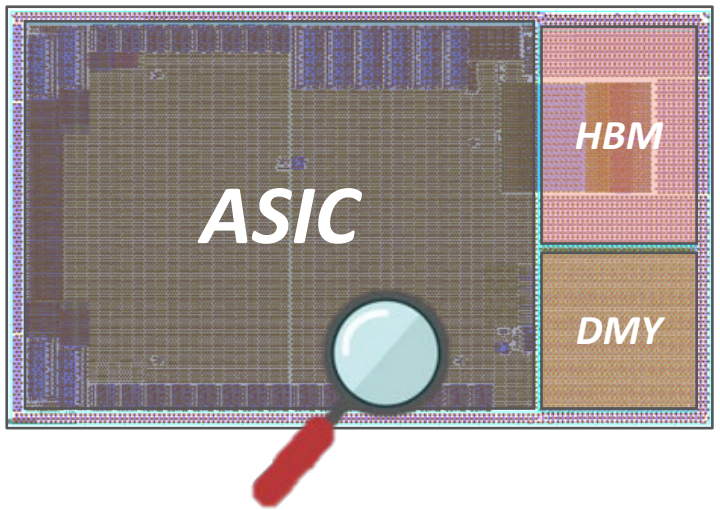


Electrical

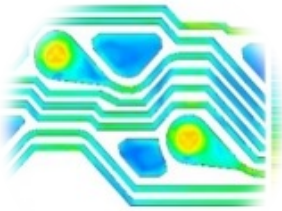


Thermal

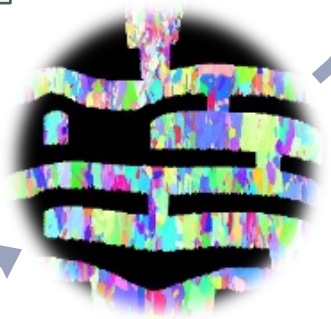




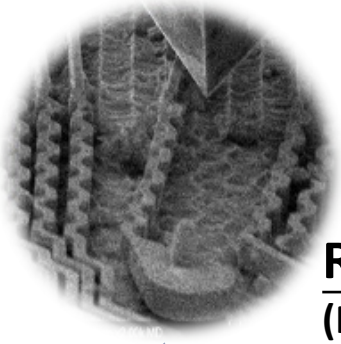
Thermomechanical Stress



Material
(FORDL EBSD)



Robustness Testing
(FORDL Picoindenter)



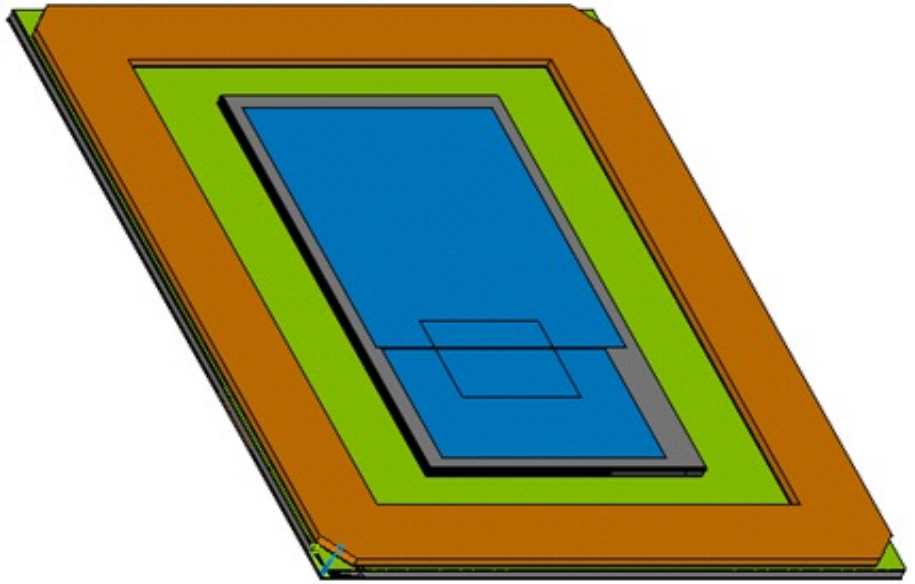
Assembly Process
(Corner Study + JMP)

Mechanical Modeling and Analysis Case Study

➢ FOCoS-B

Package Structure

- 1ASIC + HBM + 1 Si Bridge
- FO module size: 27mm x 15mm
- Si-bridge die size: 6mm x 6.3mm
- Package size: 43mm x 31mm
- Substrate 3/2/3

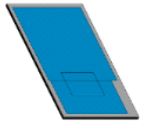
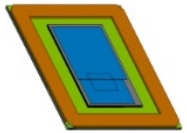


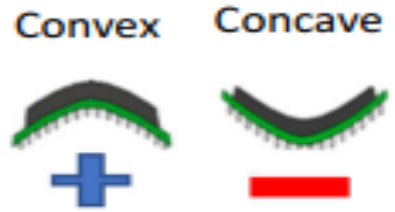
3D FEM solid model of full package

Mechanical Modeling and Analysis Case Study

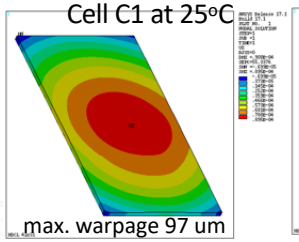
➢ FOCoS-B Warpage and Stress simulation study

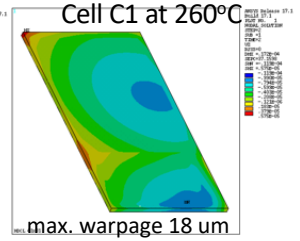
- Embedded-Si Bridge has higher stress than combo die at high temperature
- No significant different for two different molding compounds

Cell	Structure	CPD Type	Underfill Type	Underfill Type	Warpage behavior (um)		Bridge die principal stress (MPa)	
					at 25°C	at 260°C	at 25°C	at 260°C
C1 at 25°C	Combo die 	AAA	CCC	DDD	97	18	11	67
C2 at 260°C		BBB			123	17	20	69
P1 at 25°C	Package 	AAA			~155	~-115	13	~176
P2 at 260°C		BBB			~150	~-113	24	~170

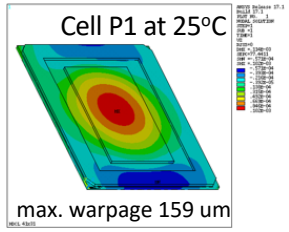


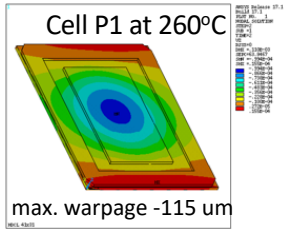
Combo Die Warpage



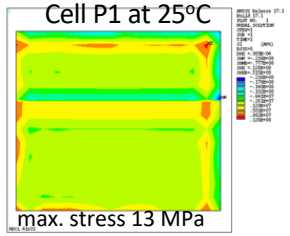


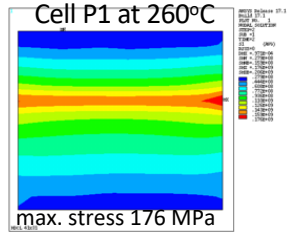
Package Warpage





Si Bridge Die Stress

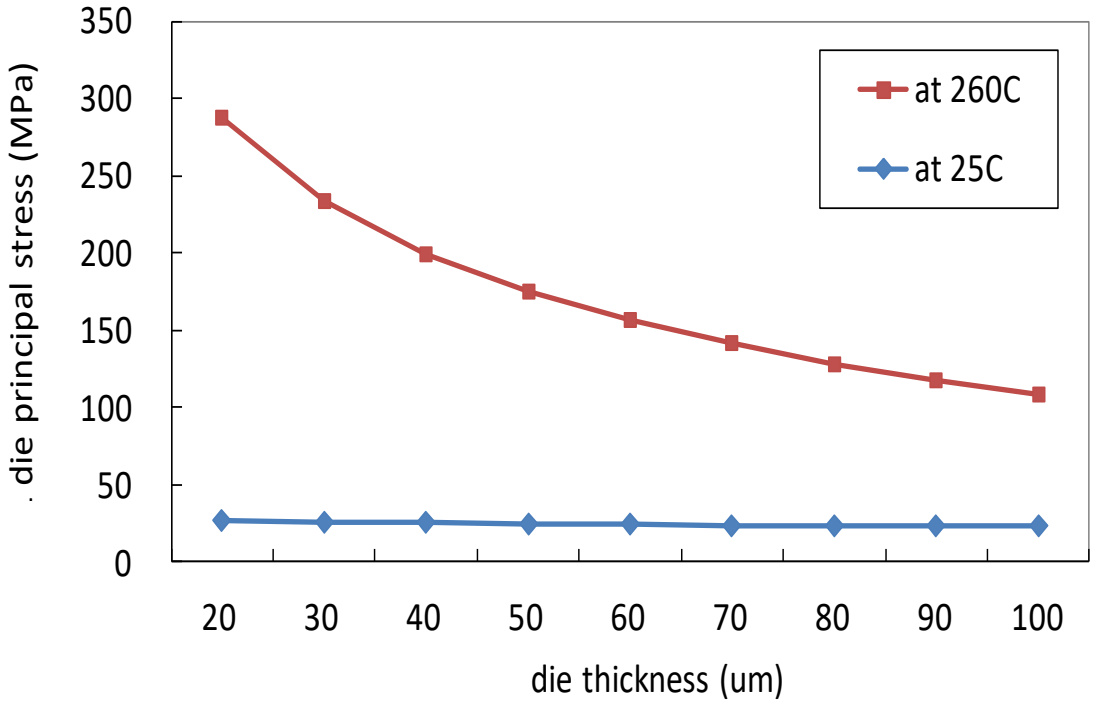




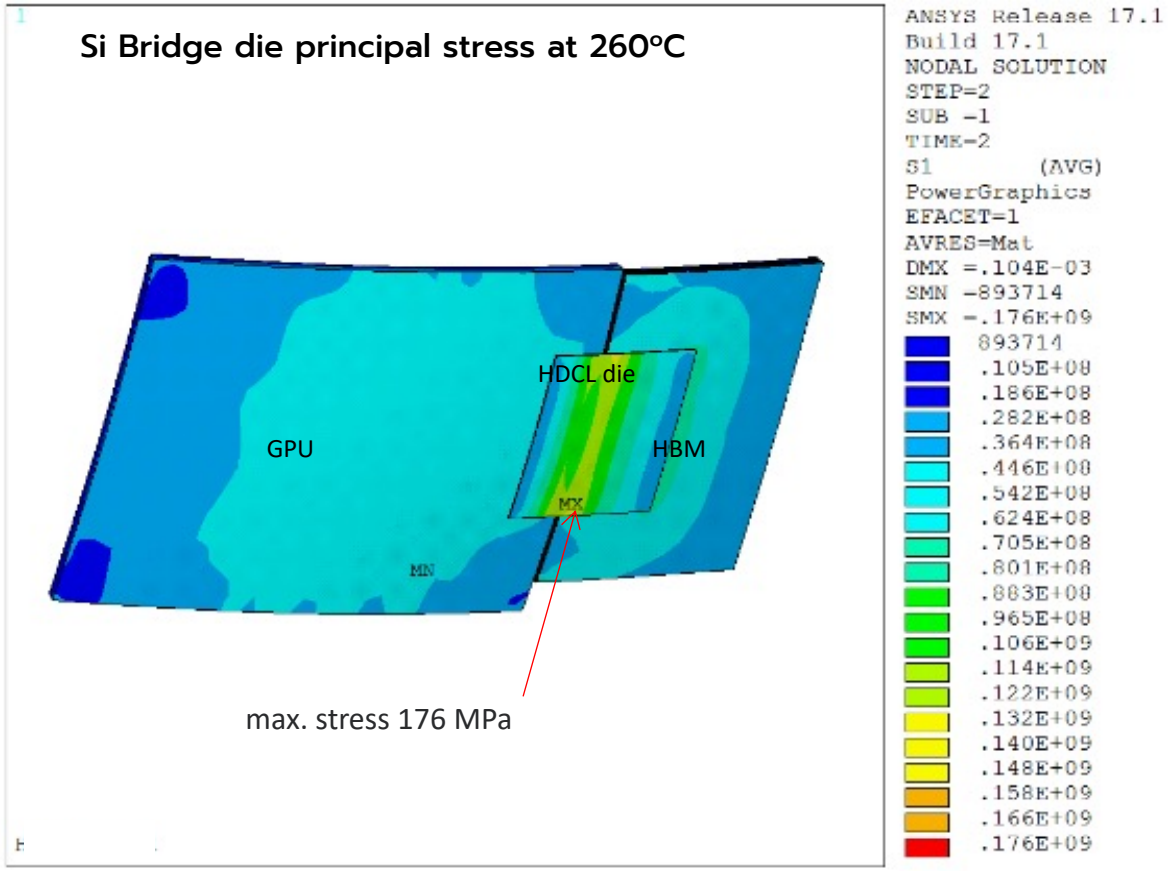
Mechanical Modeling and Analysis Case Study

➢ FOCoS-B Warpage and Stress simulation study

- Impact of embedded Si-Bridge die thickness on principle stress at package-level
  - Thinner Si-bridge die, higher stress



Si-Bridge die stress vs die thickness



Key Takeaways

- Chiplets heterogeneous integration optimizes system performance to continue scaling Moore's law with cost advantage
- Chip-package co-design and integrated design ecosystem are very crucial for chiplets integration. Mechanical stress analysis and simulation can provide predictive solutions effectively for chiplets integration design and manufacturing
- The advanced mechanical analysis workflow can:
  - Reduce the development cycle-time and save cost
  - Handle stress analysis, thermal analysis, failure analysis, and chiplet-based design optimization
  - Apply in turnkey solution design
  - Offer Auto-Stress simulation platform
- ASE can provide design turnkey solution from interposer design, stress simulation, material and structure selections to manufacturing feasibility validation for chiplets integration

Thank you