MOSAIC microsystems

Thin Glass Interposers with High-Density Interconnects

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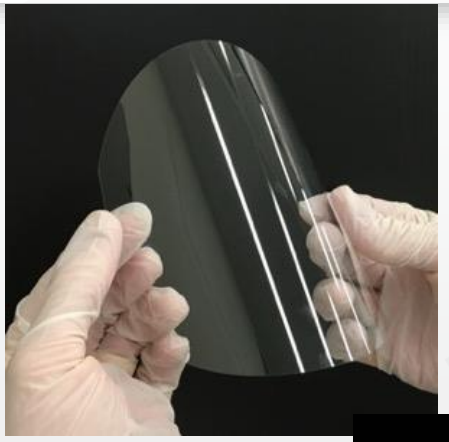
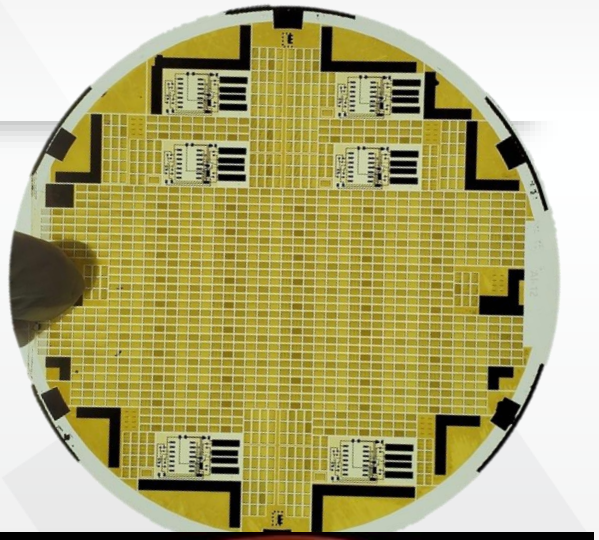
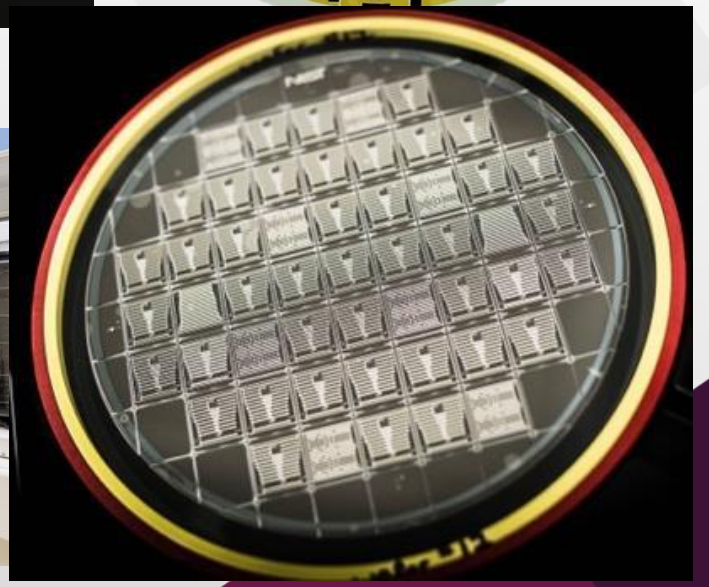
Introduction to Mosaic Microsystems

- **Glass Foundry** for advanced packaging
- Focus on **thin glass**
- Patented solution for high yield thin glass handling
- Expertise in cleaning, etching, via formation
- Based in Rochester, NY
  - 3,000 sq. ft class 1000/100/10 cleanroom







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Agenda

- Advanced packaging with glass
  - World-wide interest in Glass Substrates
- Mosaic focus
  - Viaffirm® temporary bond
  - Through-glass vias: fabrication, copper fill
  - Development of RDLs towards high density interconnects

Glass for Advanced Packaging is expanding

intel newsroom

Intel Unveils Industry-Leading Glass Substrates to Meet Demand for More Powerful Compute
Glass substrates help overcome limitations of organic materials by enabling an order of magnitude improvement in design rules needed for future data centers and AI products.

absolics

Absolics Inc., a subsidiary of South Korean conglomerate SK Group, has broken ground on a planned $400-$600 million investment in Covington, Georgia, where it will build glass-based semiconductor packaging for the U.S. chip industry.

DNP

DNP develops TGV Glass Core Substrate for Semiconductor Packages

CHIPS Act NAPMP NOFO#1
Includes call for glass substrates

SAMSUNG

Samsung Electro-Mechanics (Semco) has announced plans to develop semiconductor packaging glass substrates.

Glass has excellent properties

Physical / Mechanical

Smooth (<1 nm RMS)
High Young's modulus

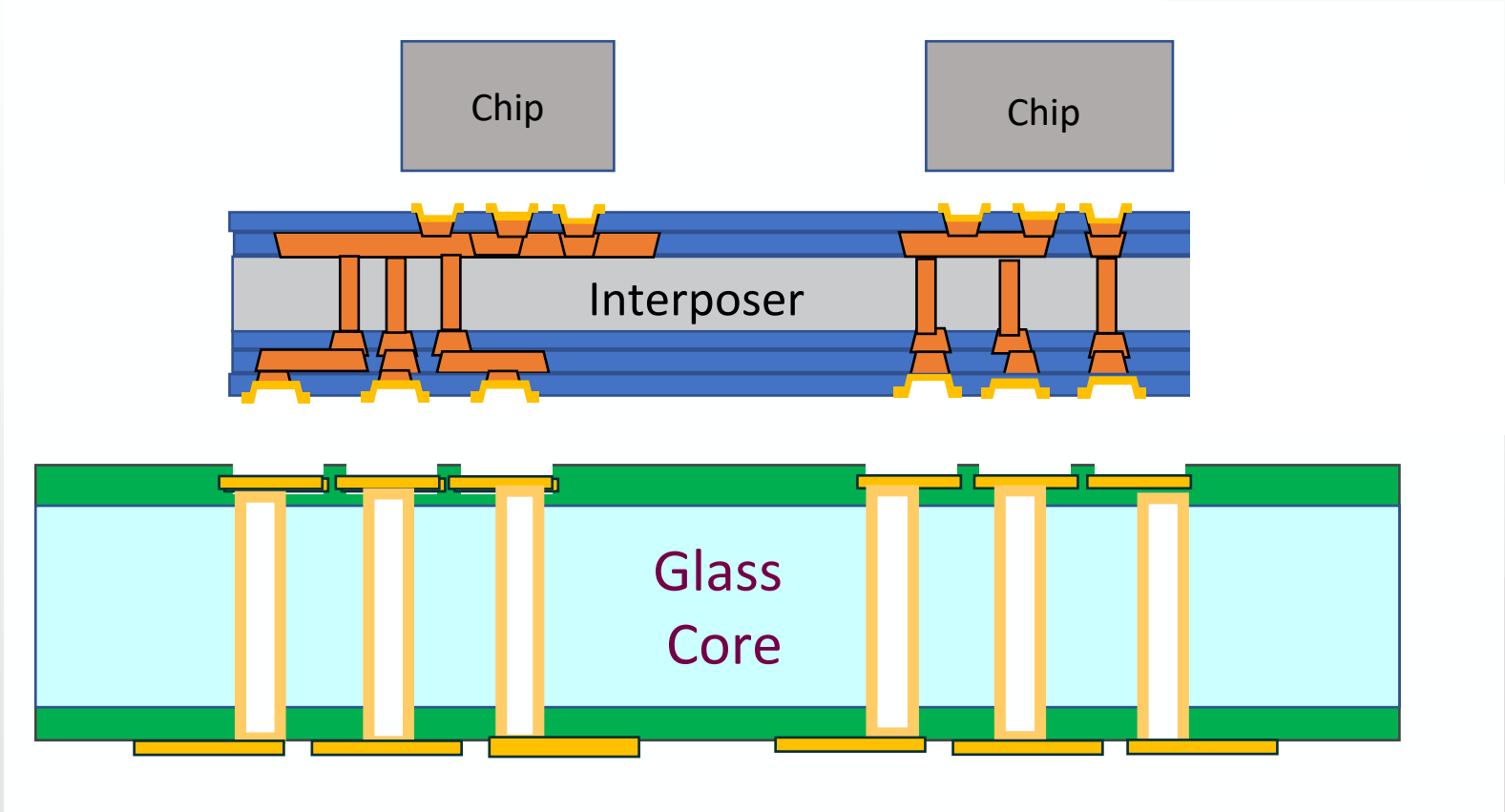
Environmental

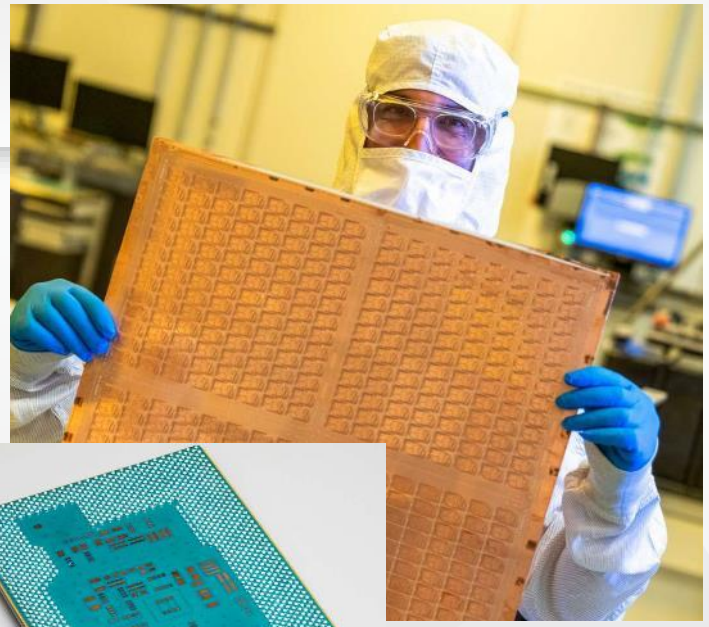
Chemically robust
Impermeable to moisture
High temperature compatible

Electrical

High resistance
Low loss (GHz)

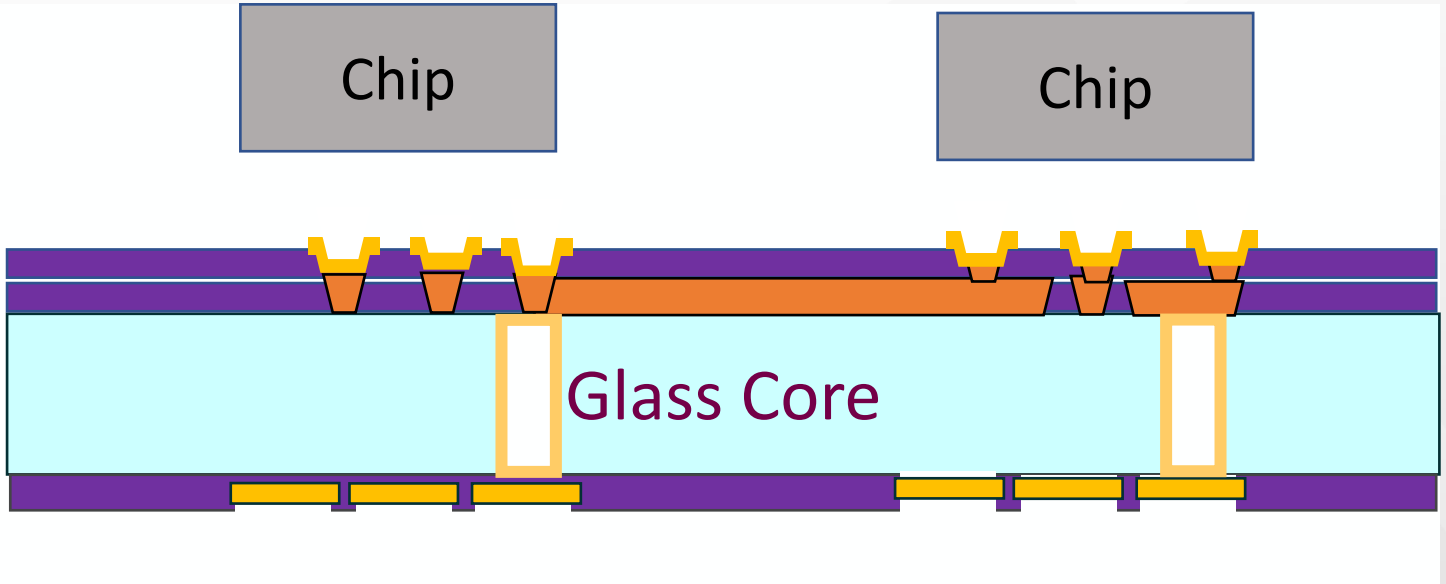
News stories: industry efforts are focused on "Substrates"





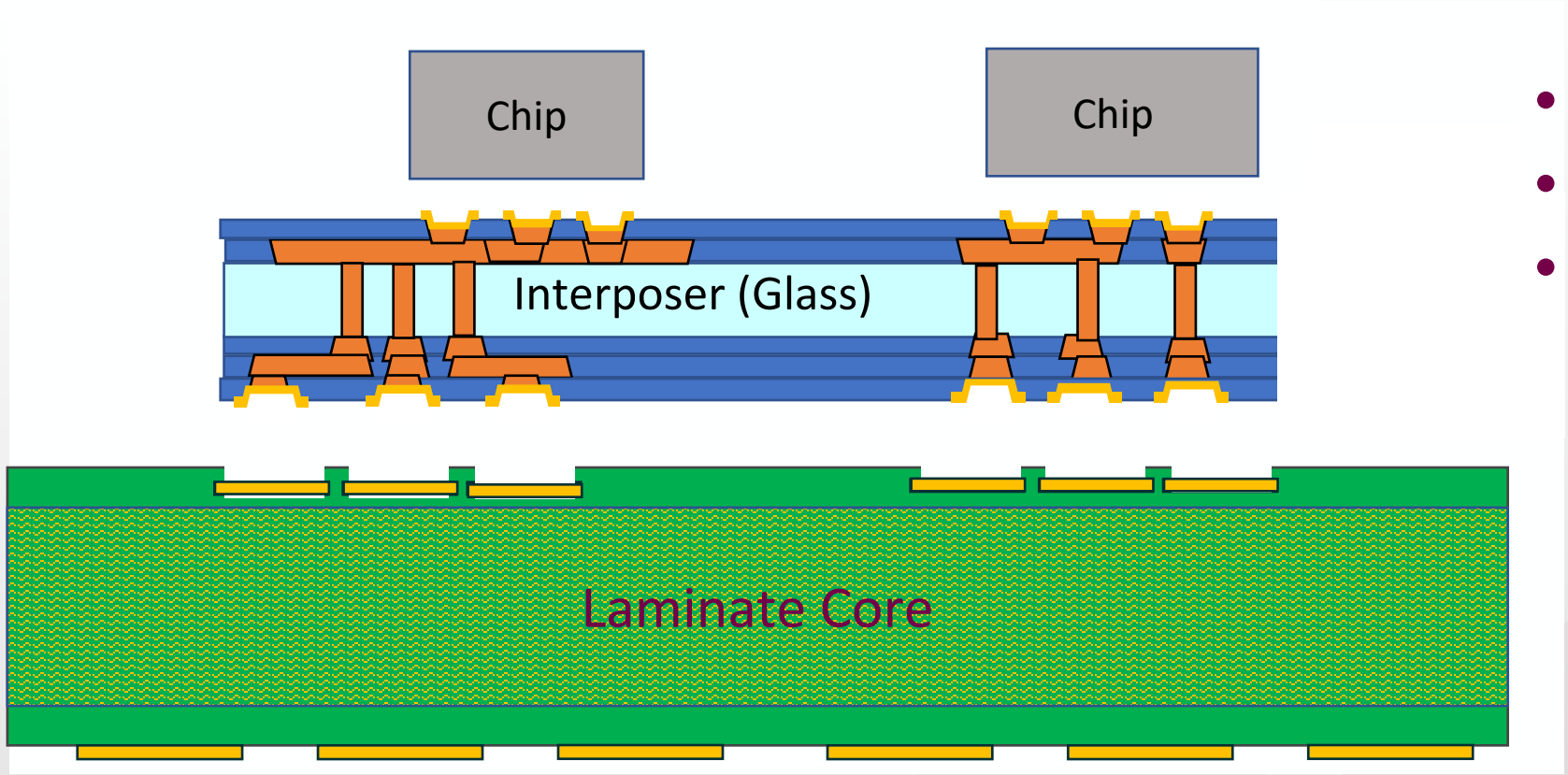
https://www.intel.com/content/www/us/en/newsroom/news/intel-unveils-industry-leading-glass-substrates.html#gs.6427gl

Emerging focus: NAPMP (NOFO for Materials and Substrates, TA2)



- Skip the interposer
- 10 + 10 RDLs
- Very tight pitch on RDLs
- Very large vias in core (loose pitch)

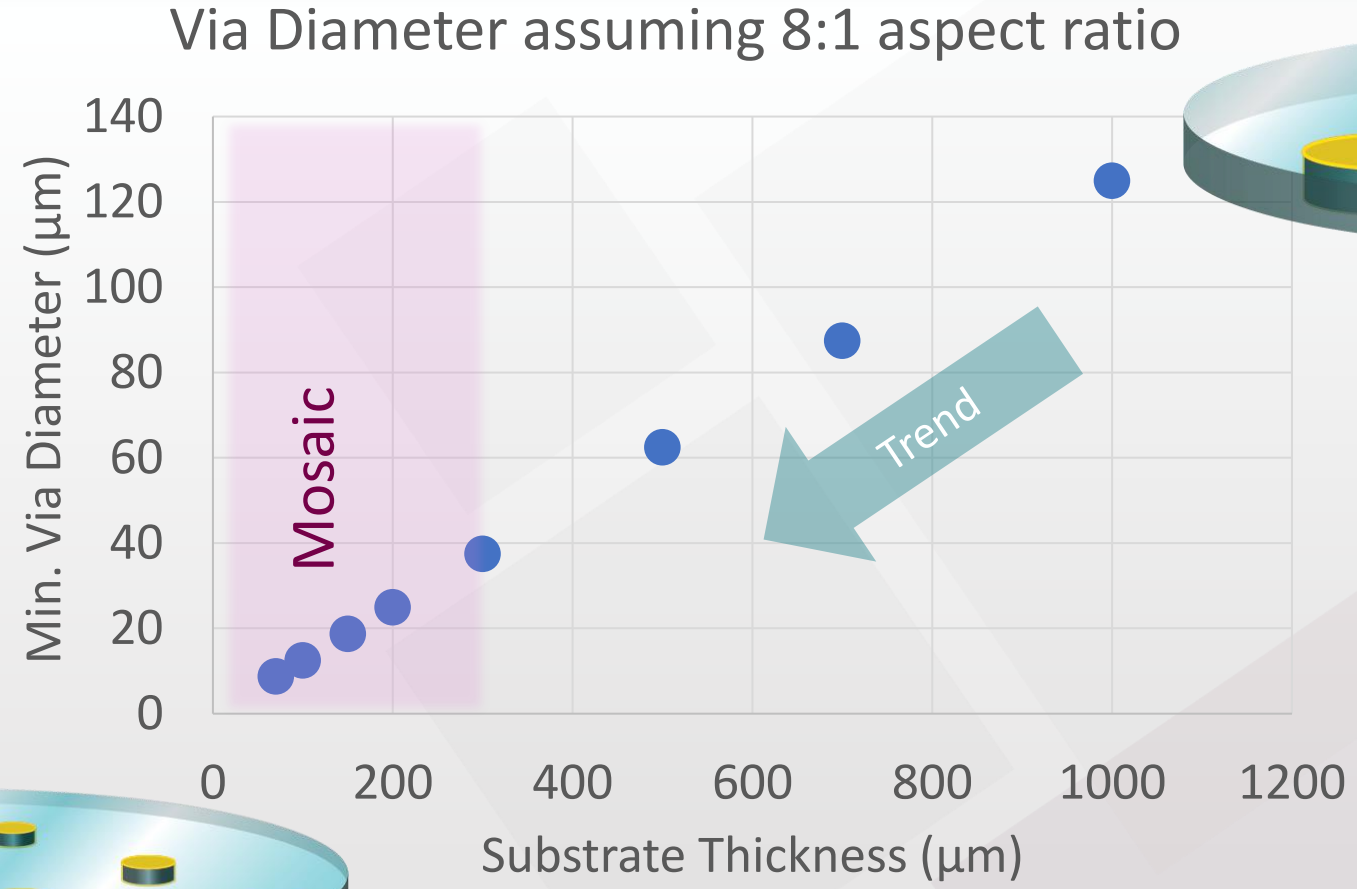
Mosaic's current focus is thin glass interposers

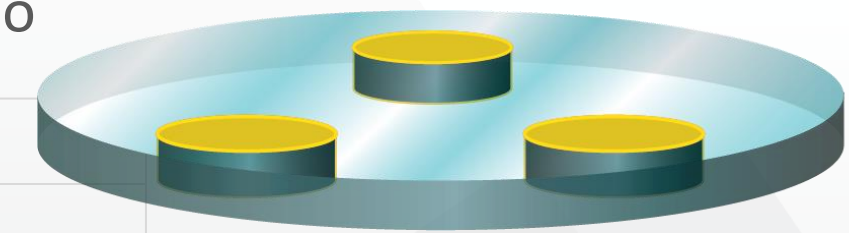


- Thin glass→ small vias
- Solid Cu via-fill
- Developing RDLs for high-density circuitry

We didn't "miss the memo" about substrates!

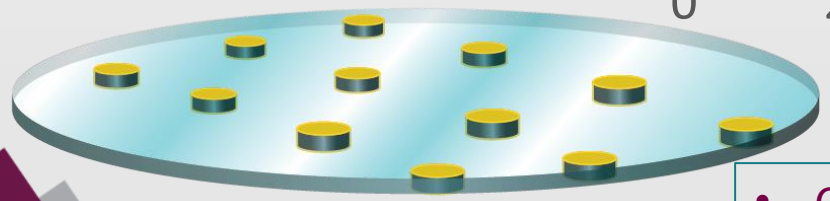
Circuit line pitch scales ~ via diameter





Mechanical Stability

Circuit Density



- Current products need thin glass (mm-W)
- Also (perhaps) ahead on the glass roadmap

The Future is Clear™

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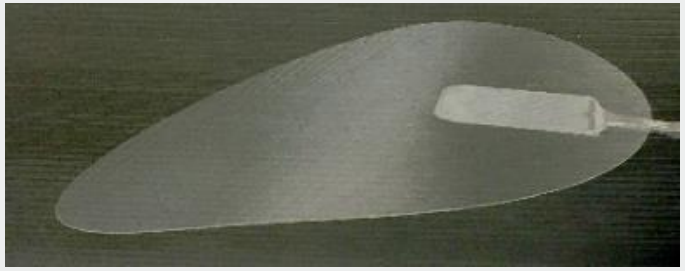
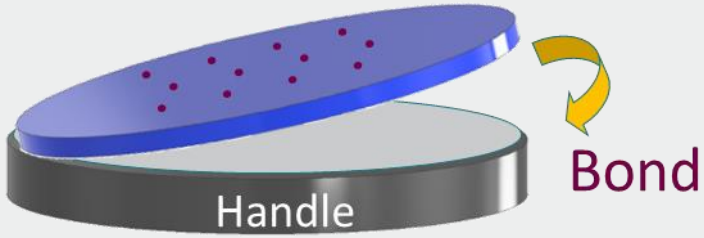
Mosaic has solved the challenges of thin glass processing

Thin glass



Temporary bond



Glass or Si handler

- **Mosaic has solved the handling problem:**

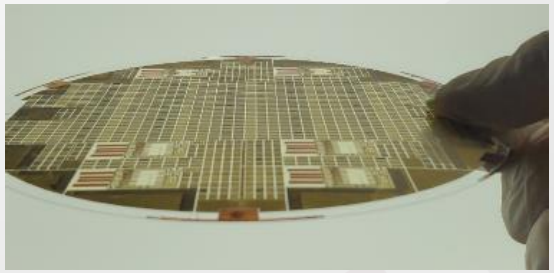
✓ Viaffirm® temporary bond technology

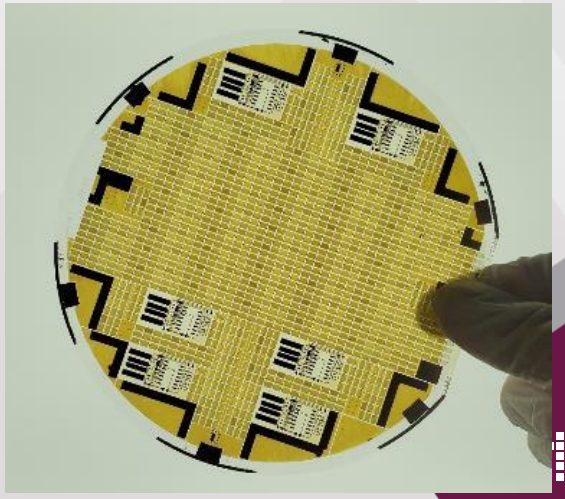
✓ High yield processing

The thin inorganic temporary bond provides a broad processing window

- Thin adhesion layer → Excellent flatness
- Extreme resistance to processing
- Chemically robust
  - *OK with Acids, Bases, Solvents*
- Thermally robust
  - *OK to 450°C*
- Vacuum-robust
  - *OK with plasma*

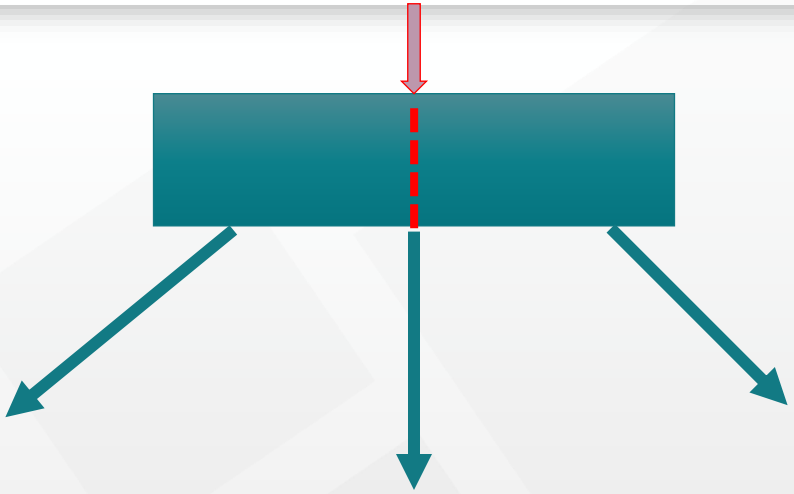
100um-thick





2 + 2 RDLs

TGV fabrication is by laser plus wet etch: allows a range of through glass via (TGV) shapes

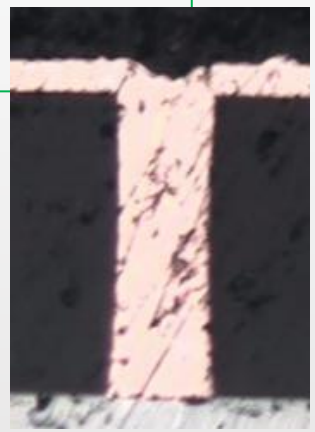


Hourglass via

Example

35um in 100um glass

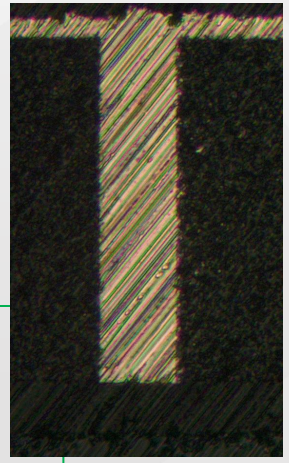
~30um waist



Columnar via

Example

33um in 150um glass



Tapered via

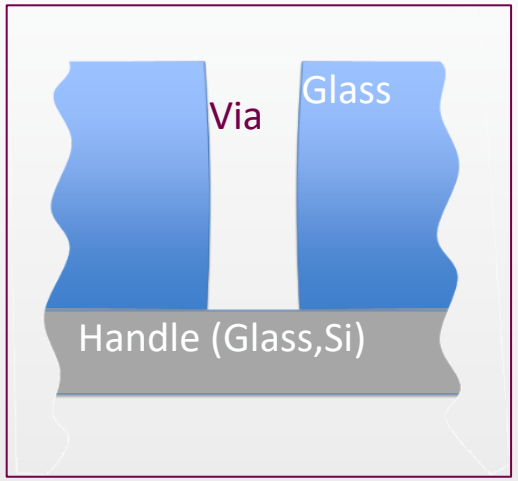
Example

30um top, 20um bottom

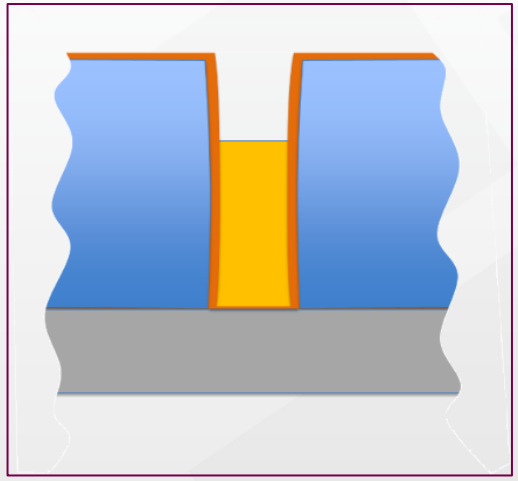
175um glass

Thin glass + bond creates a “Blind” via for copper fill

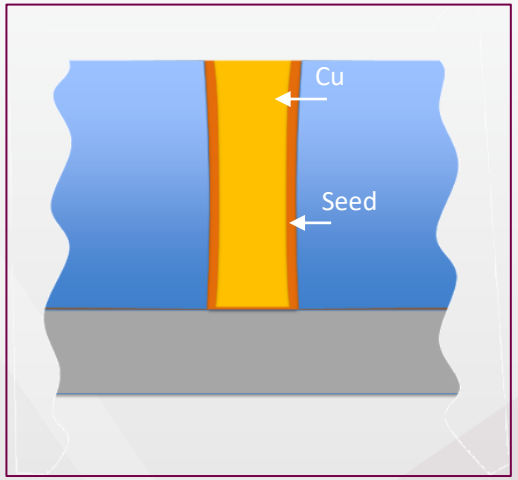
- Compatibility with industry TSV electroplating process



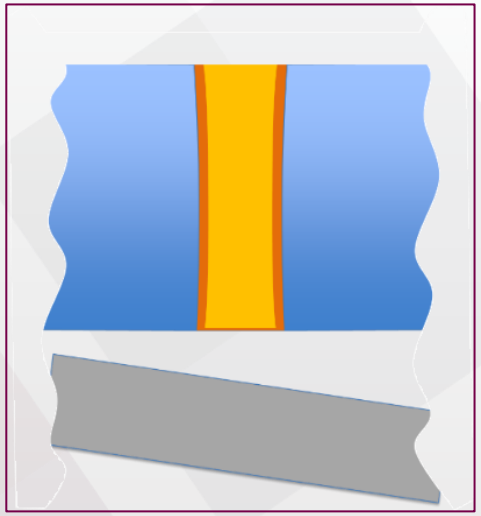
Blind via at bond to handle



Seed and bottom-up fill



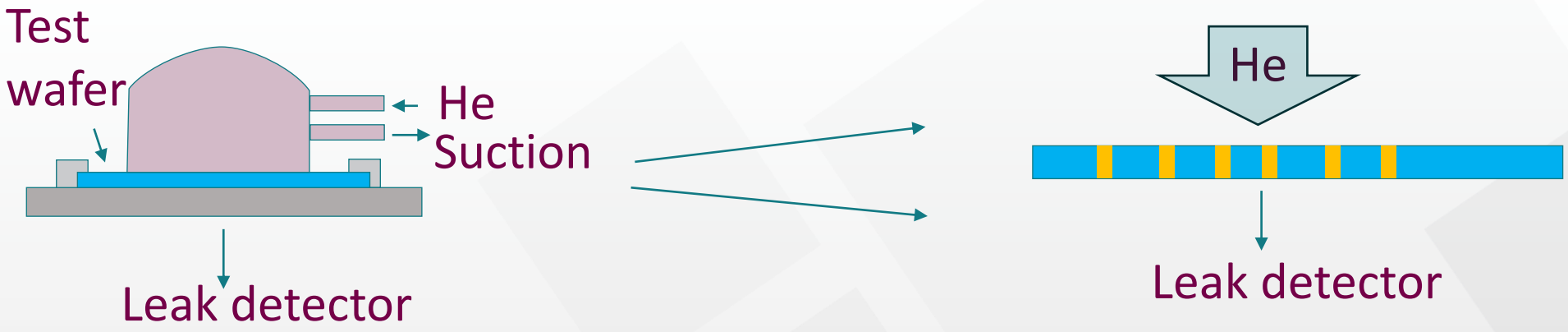
CMP



Debond reveal

Fully-filled vias are hermetic

- Helium leak test with detection limit ~$1x10^{-9}$ atm-cc/s



Alumino-borosilicate glass with 25um vias

- Wafer tested after 450C / 1.5 hrs
- Hermeticity at detection limit
  - ~3,000 vias

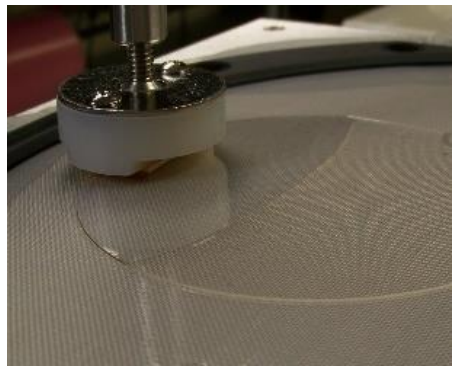
High Purity Fused Silica with 35um vias

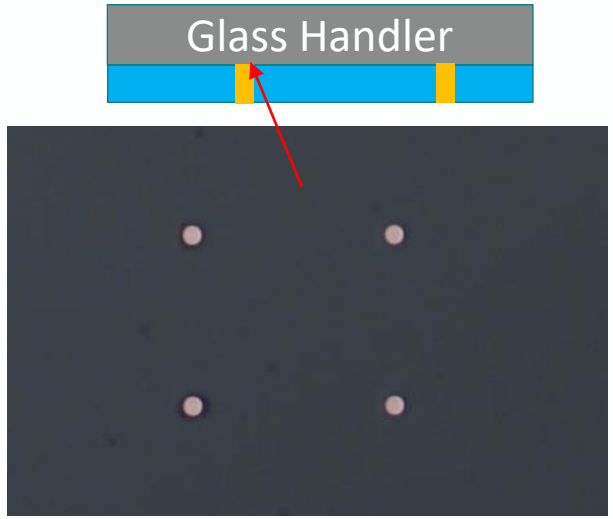
- Wafer tested before and after 260C / 1 hr anneal
- Hermeticity at detection limit
  - ~ 26,000 vias

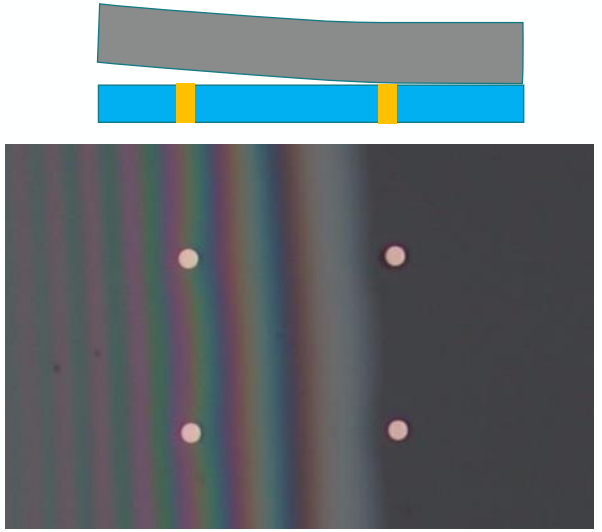
After processing, mechanical debond process

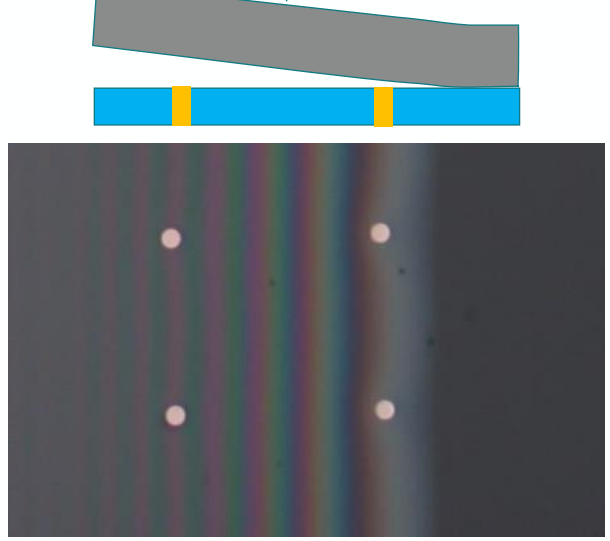
- Mechanical debond: Handle pulled away from device
- Seed layer engineering:
  - Control of adhesion at via base
  - Debond proceeds smoothly through via areas
- Filled vias peel off handle →**simplified backside reveal!**

Viewed through glass handle

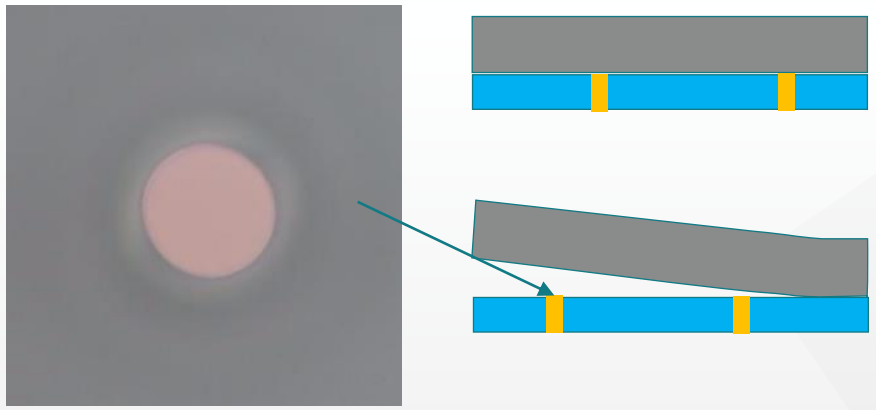




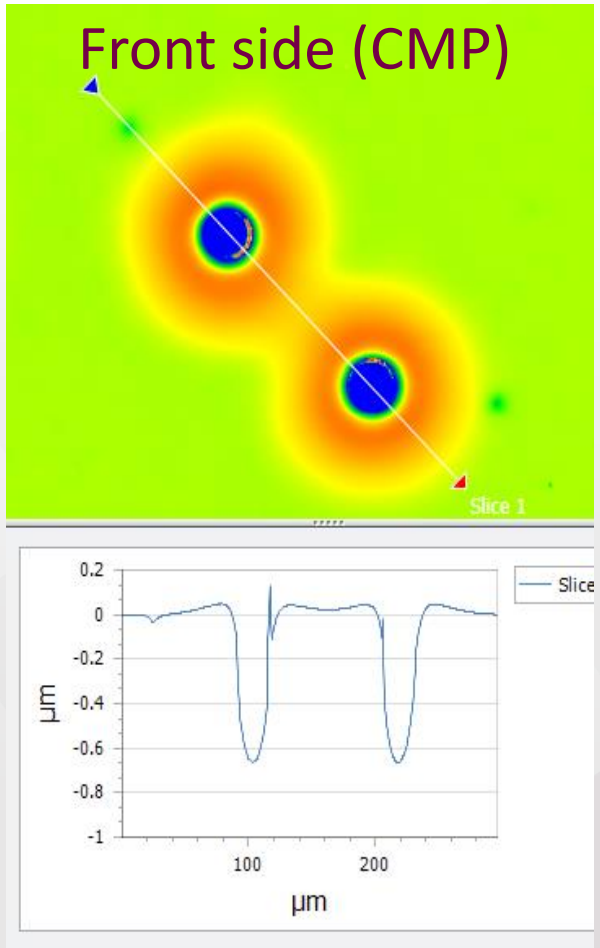


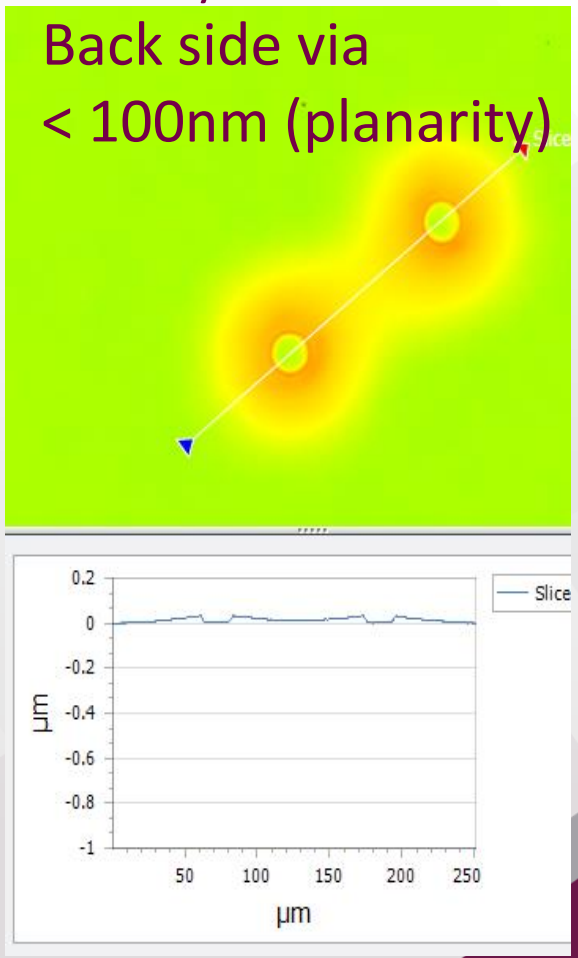


Mechanical debond yields a smooth via surface



Optical Profilometry

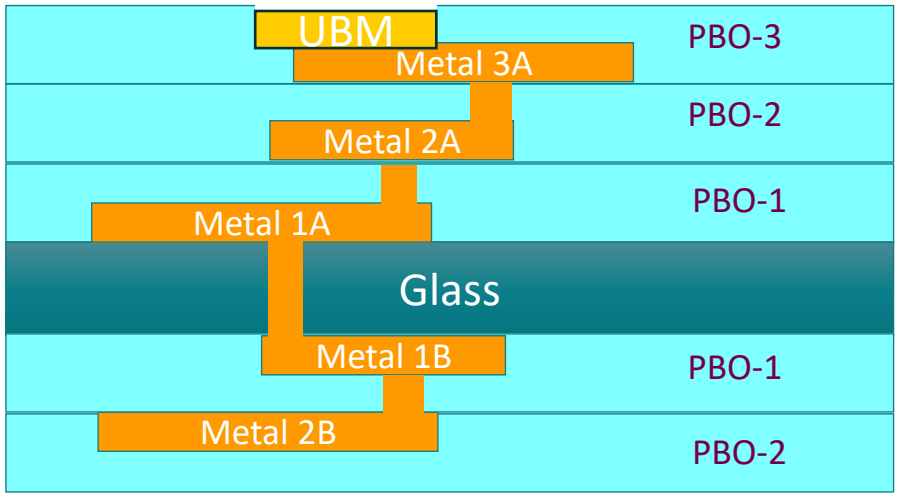




- Smooth surface is obtained with no additional processing
- No residue (by XPS)

Interposer Fabrication Process: RDLs

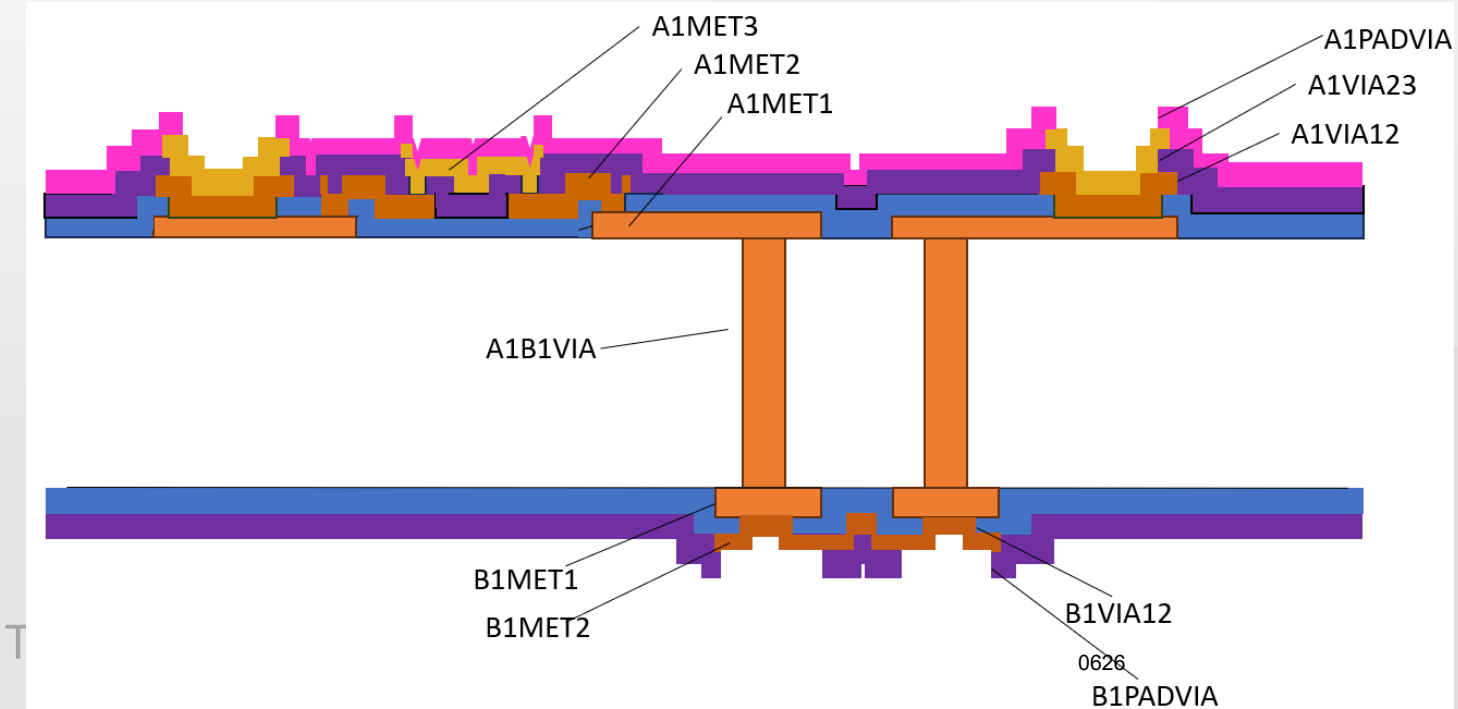
- Redistribution Layers (RDL) by the semi-additive process
- Electroplated Cu lines and PBO interlayer dielectric
  - Cu lines are 3 um thick
  - PBO interlayer dielectric is 3um thick
- Current Process at 15µm line and space
  - Demonstrated 5µm L/S
    - Current Equipment limiting factor <5µm

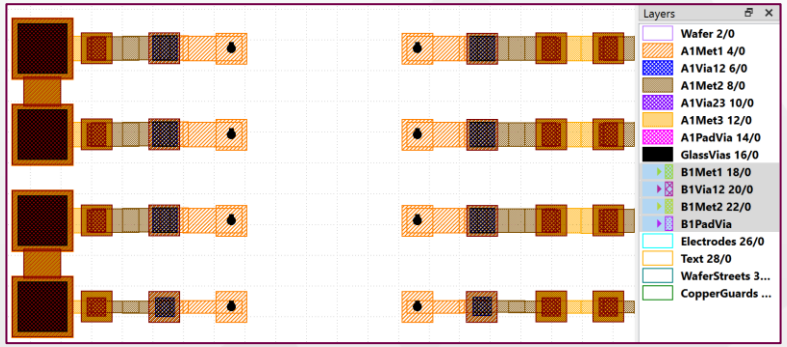


Sketch of example
3 RDL with UBM on top
2 RLD on bottom

RDL Processes on thin glass: example

- Planarization characterized: spin-on dielectric optimized
- Stress characterized
- Electrically tested daisy chains vs line-width





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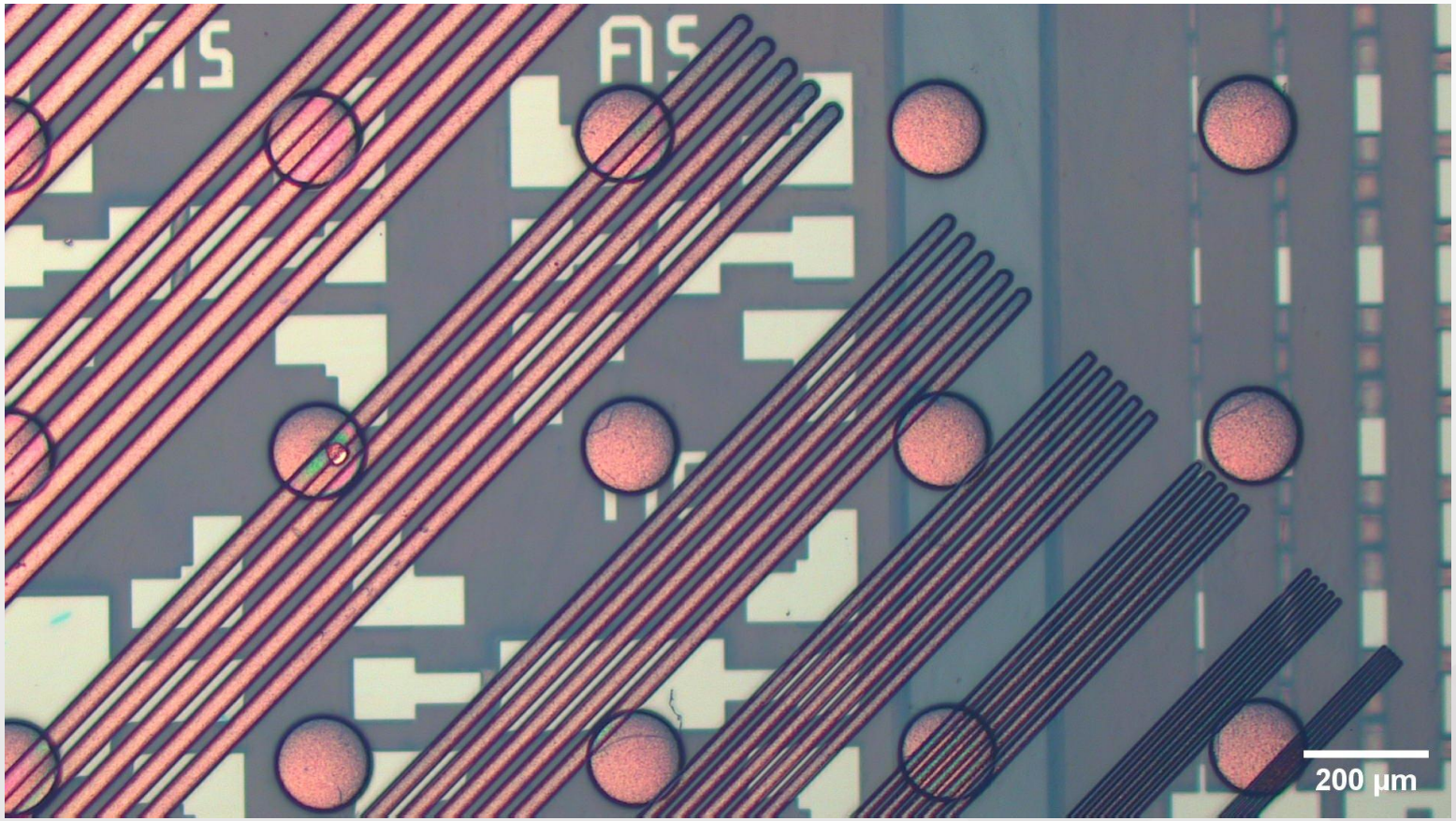
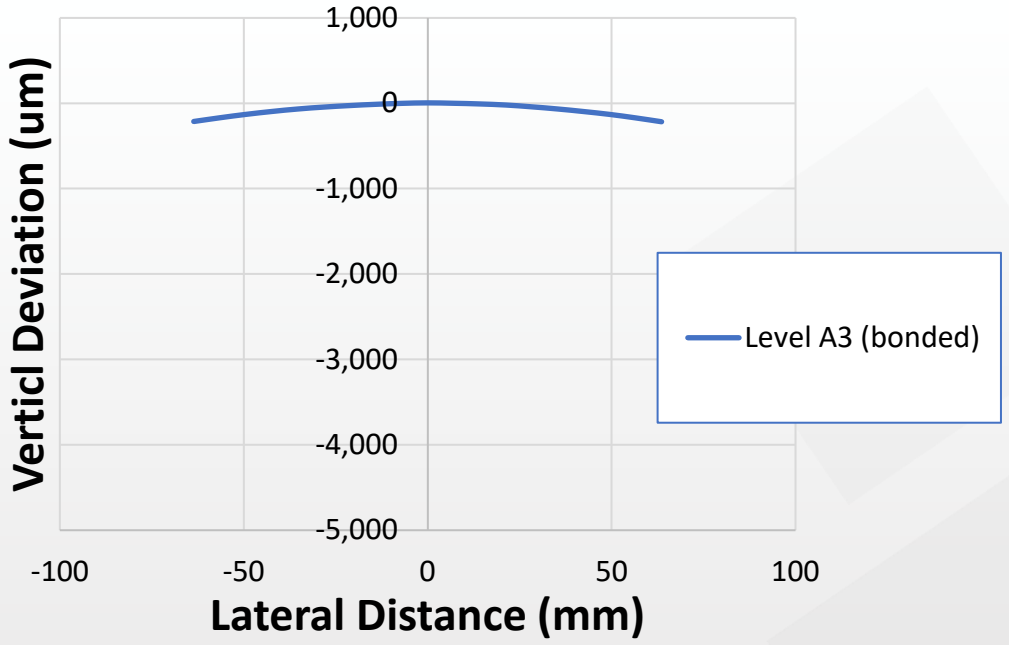
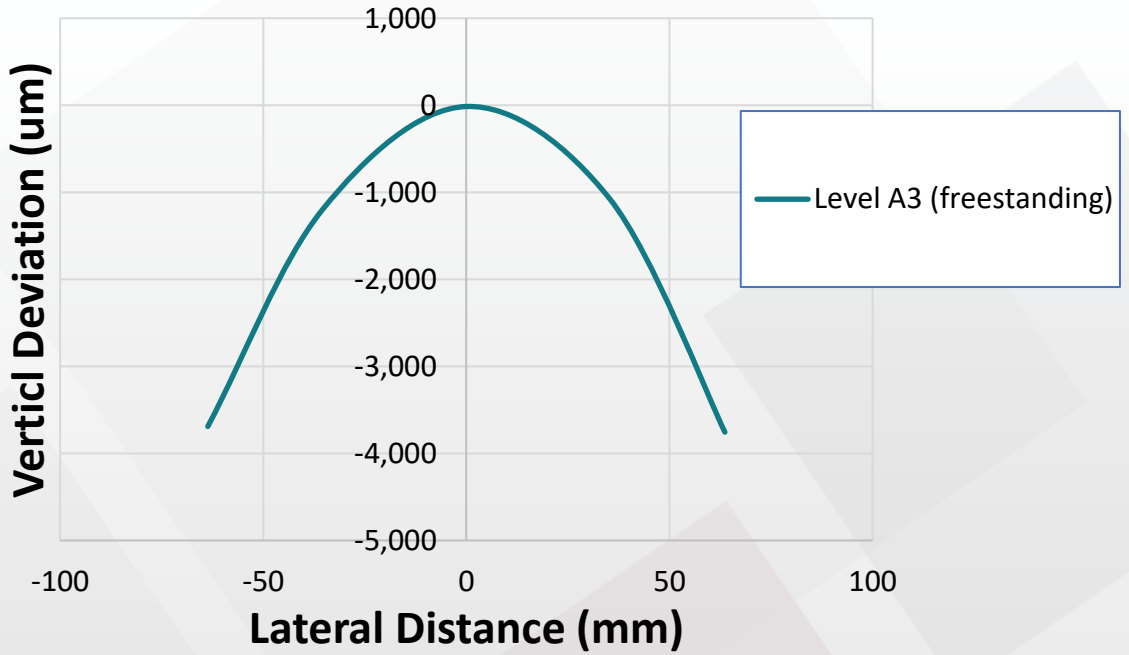
B-side RDL structures to assess metal overlayer integrity

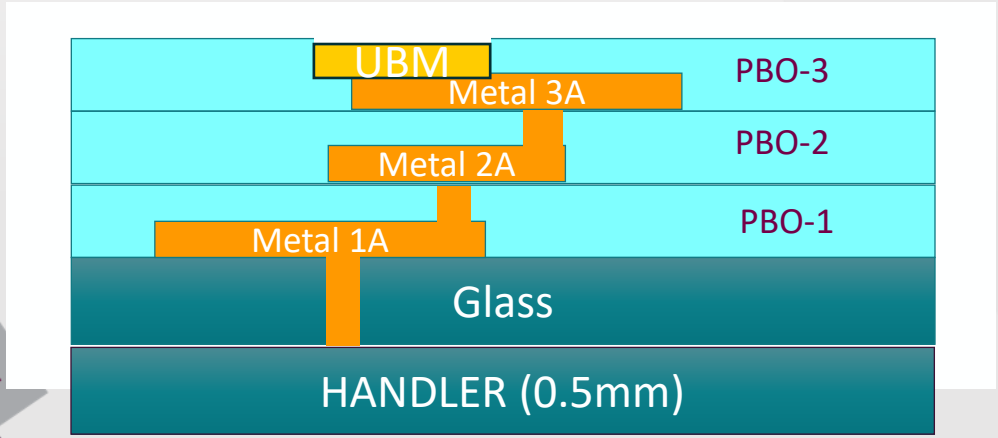


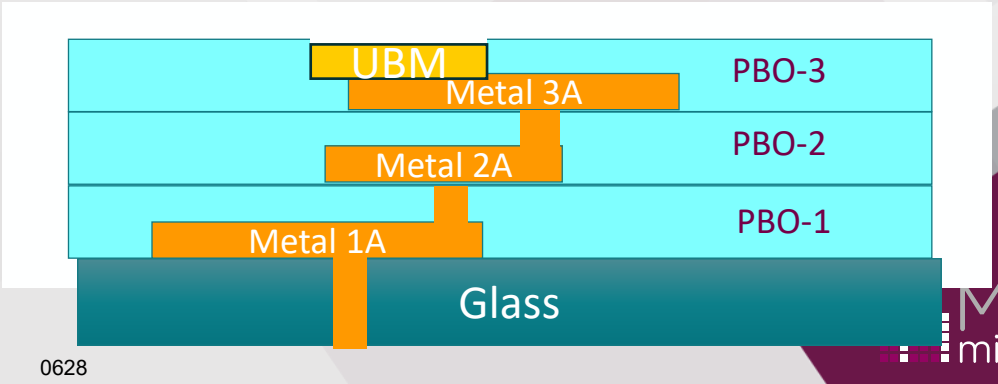
- Backside RDL example
- B1 Metal: Dots / B2 Metal: lines
- Background: A-side metal (grey = Ta adhesion layer)

One-sided 3-level RDL on handler, and off









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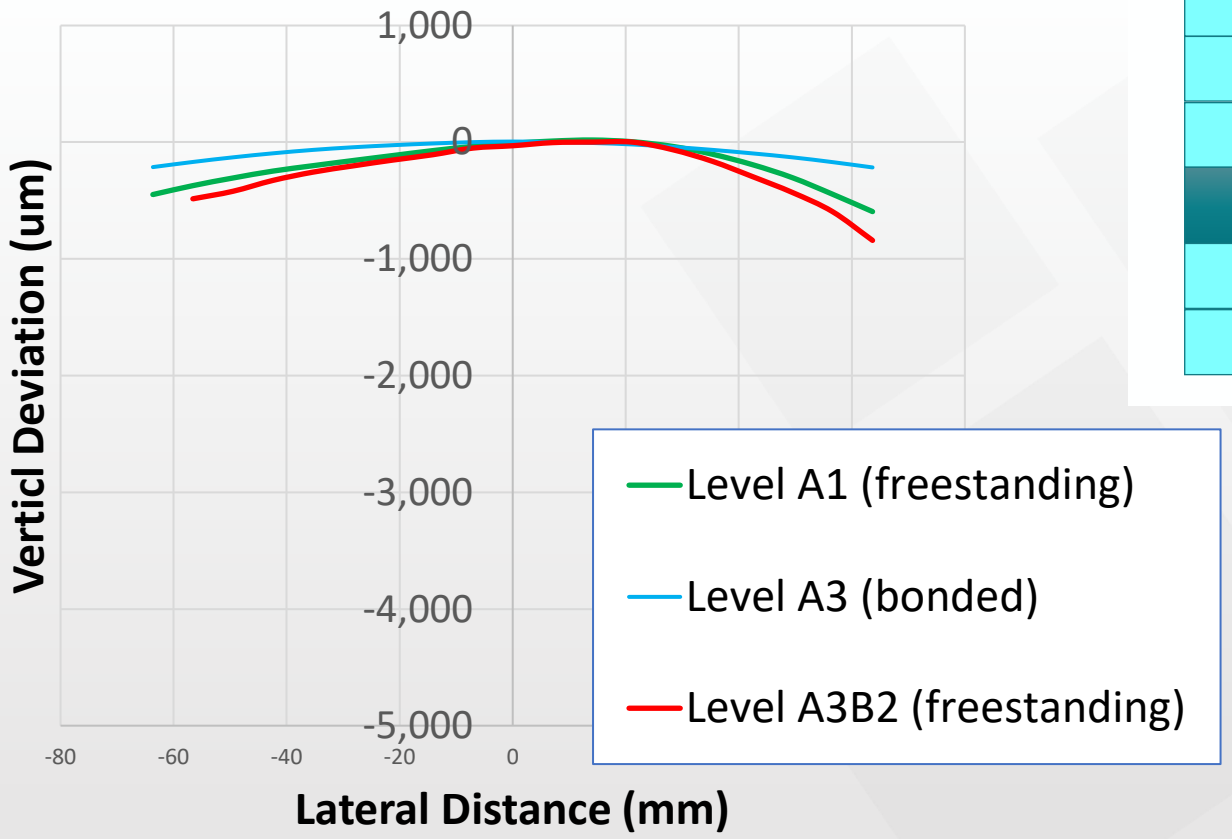
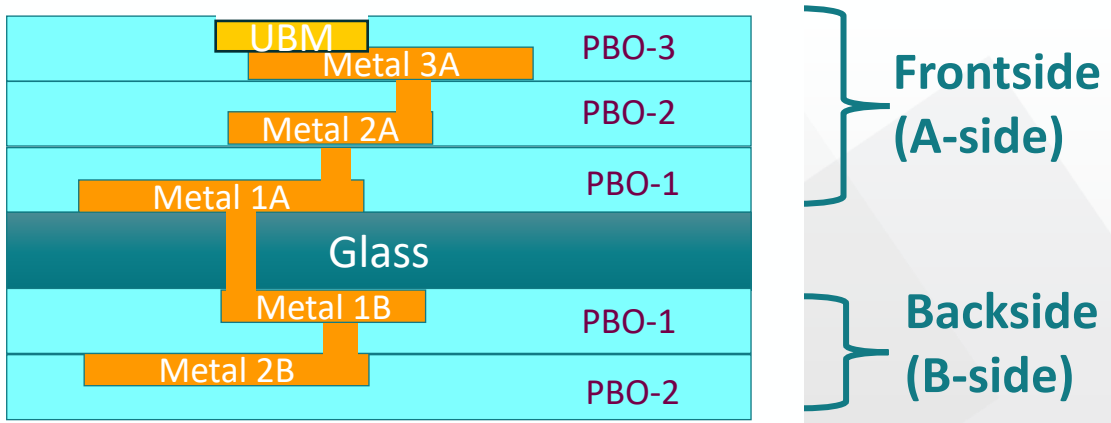
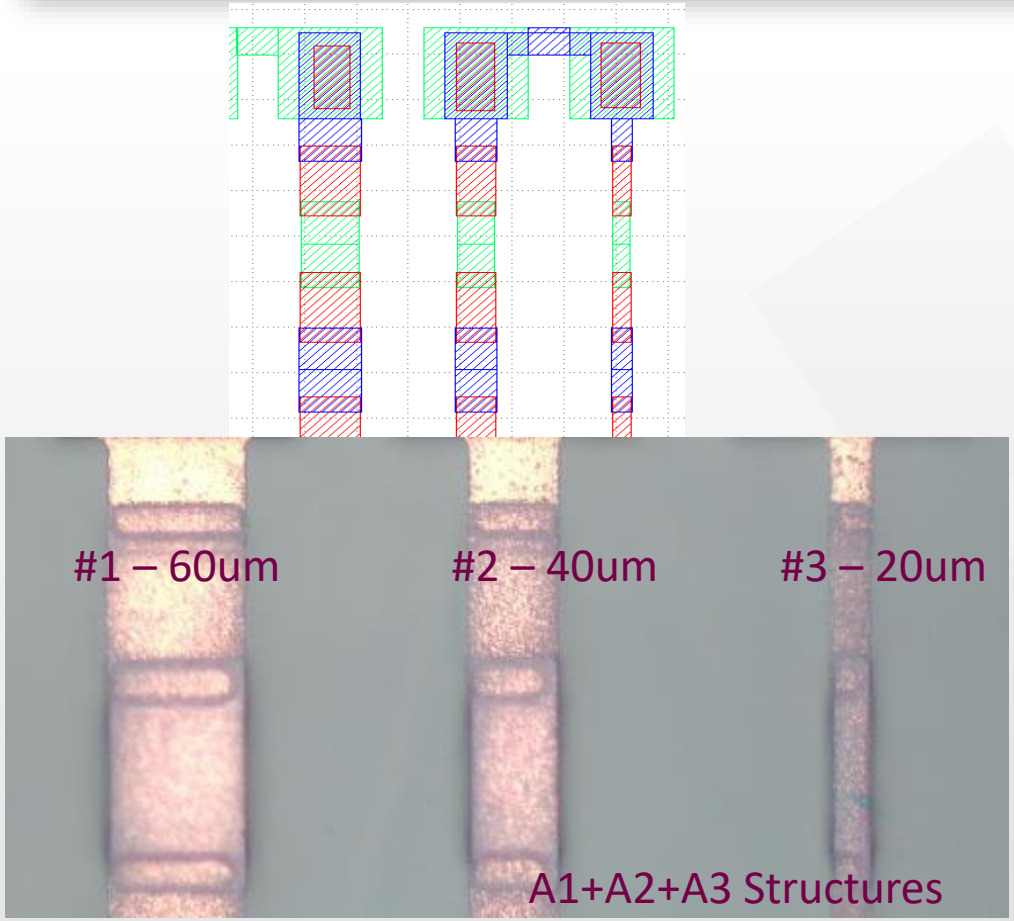
RDLs with balanced metal layers





- Adding A-side RDL layers increases wafer bow
- Adding B-side RDL layers counteracts wafer bow

RDL Electrical Characterization



- Daisy Chain Tests A1- A3 & B1– B2
- Columns of 60, 40 & 20 µm width
- Metals 1,2 & 3

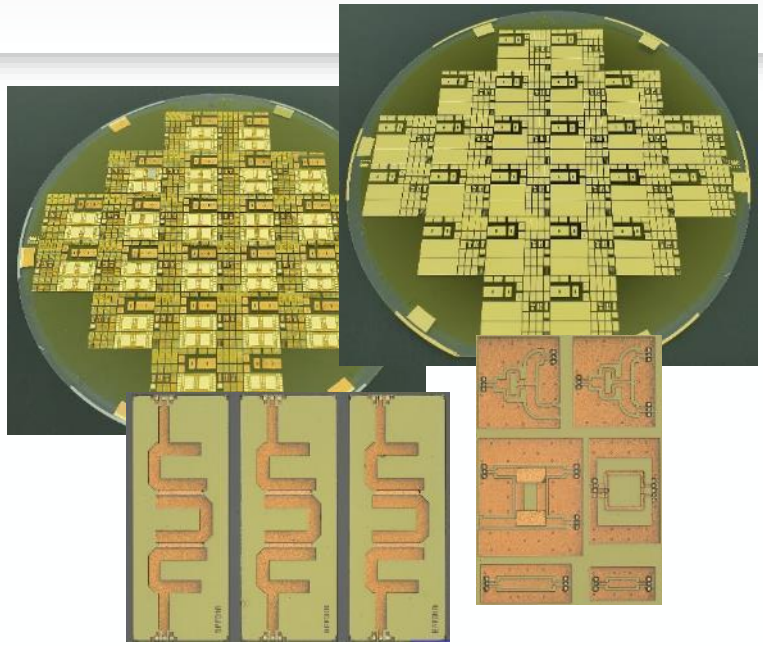
Tested Daisy Chains Fully Connected			
Line Width (um)	**60**	**40**	**20**
A1+A2+A3	10 of 10	10 of 10	6 of 10*
B1+B2	10 of 10	10 of 10	10 of 10

*PBO Alignment

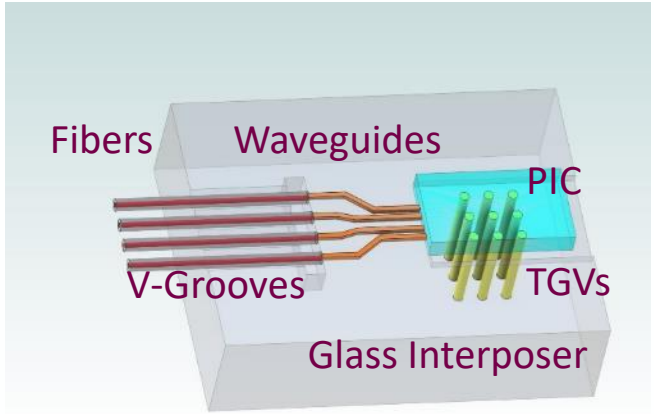
- Preliminary Daisy Chain Tests through entire structure
- Connectivity through all layers

Projects ongoing with a focus on RF

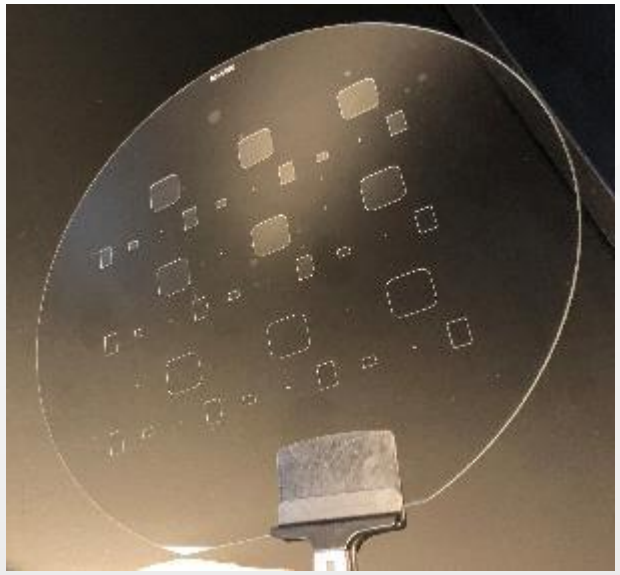
- >100 GHz TGV-based glass packages
  - Push limits for glass at high frequency
  - Wirebond and flip chip assemblies with RFICs
  - **Internally** – further development **on thin glass** of via, RDL, underbump metallization, integrated passives (TaN thin film resistor)



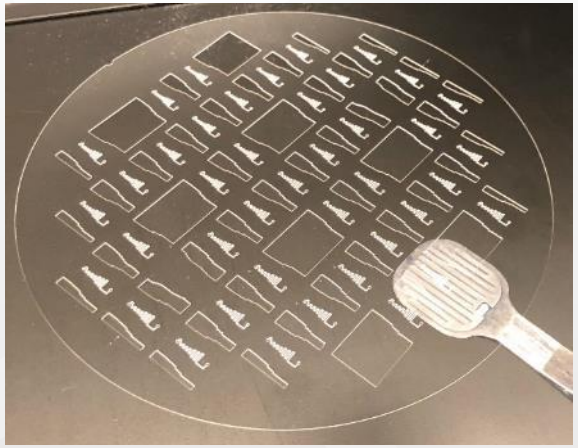
- Projects involving photonics starting
  - Photonic interposer
  - Early stage – development of waveguides on glass, methodologies for chip placement

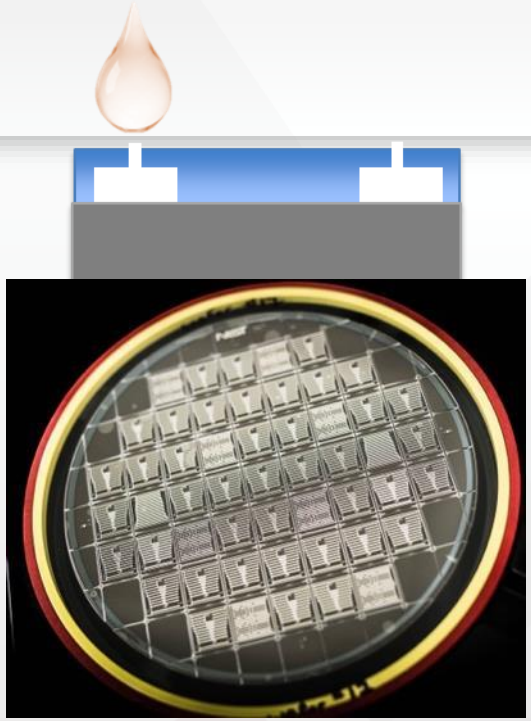


Fusion of stacked structures



3-layer permanent stack with pockets





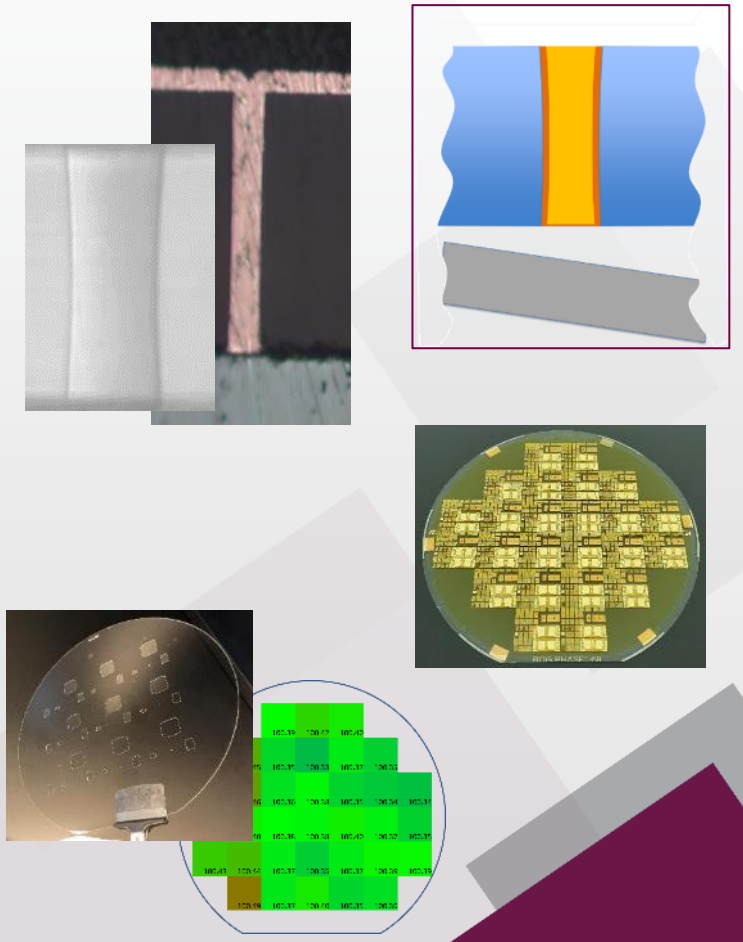
2-layer microfluidic stacks demonstrated, aligned to electrodes on bottom wafer

Enabled by:

- Laser ablative patterning
- Cleaning, etching, handling processes

Summary

- Thin glass (+ TGV) is relevant now, and perhaps in the glass roadmap
- A novel temporary bond enabling industry relevant via fill and RDL processes
- Etching and handling technologies open the door to new opportunities



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- This work was supported by
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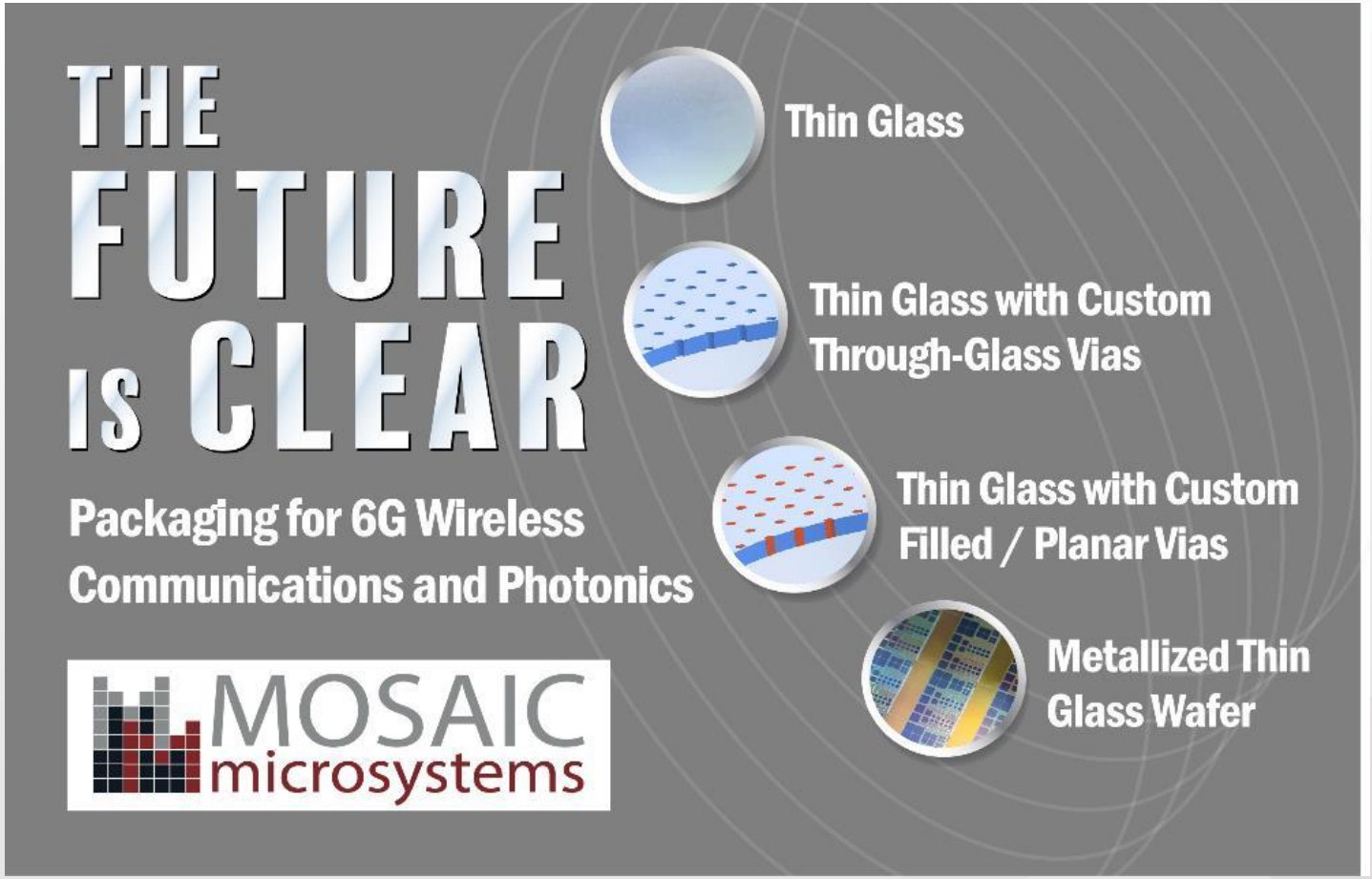
National Science Foundation

Thank you


THE FUTURE IS CLEAR
Packaging for 6G Wireless Communications and Photonics
MOSAIC microsystems
Thin Glass
Thin Glass with Custom Through-Glass Vias
Thin Glass with Custom Filled / Planar Vias
Metallized Thin Glass Wafer

Glass type can be matched to application

The application determines the preferred glass type

Material Property	Mosaic Typical Glass Types	
	High Purity FS	Low alkali (ABS)
Modulus (GPa)	73	74
CTE (ppm/^{0}C)	0.5	3.2
Dielectric constant	3.8	5.3
Loss Tangent (60GHz)	0.0004	0.01