DECA

Achieving Large-Scale HBM Integration with Adaptive Pad Stacks on Molded Embedded Bridge Die Interposers

Benedict San Jose – Pr. Materials, Process, and Integration Engineer

Cliff Sandstrom – SVP of Technology Development

Craig Bishop – CTO

Tim Olson – CEO & Founder

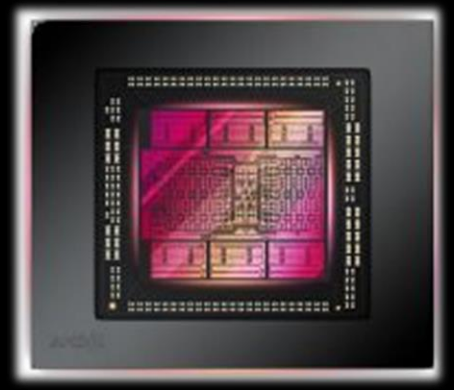
Outline

- Background
- Managing the increase in package sizes
  - Transition away from Si interposers
  - Shift to Fan-out technology
  - Advance toward large panel
  - Extend Adaptive Patterning
- Conclusion

Chiplets are everywhere

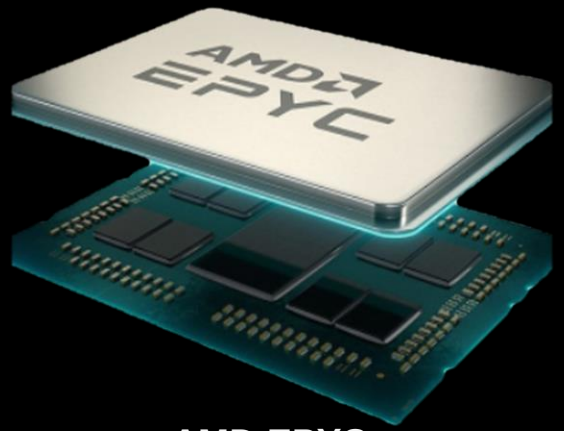
Consumer

M1 Ultra
2x M1 Max die

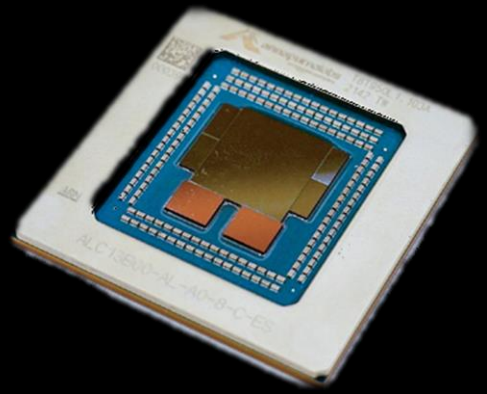


AMD RDNA3
7 chiplets

Data Center

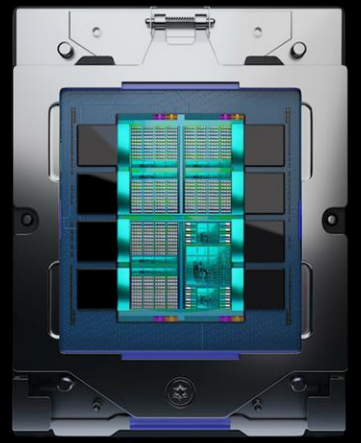


AMD EPYC
9 chiplets

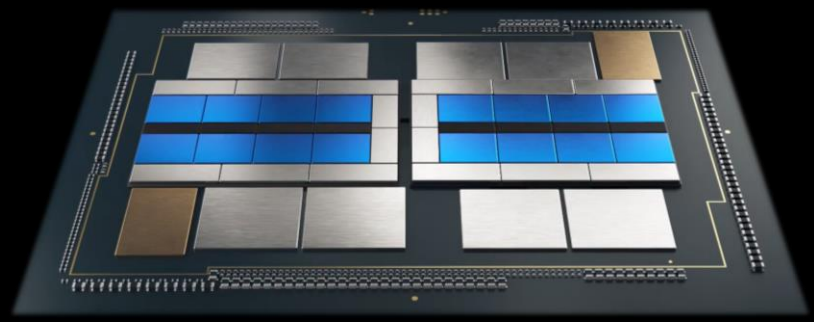


AWS Graviton
7 chiplets

AI

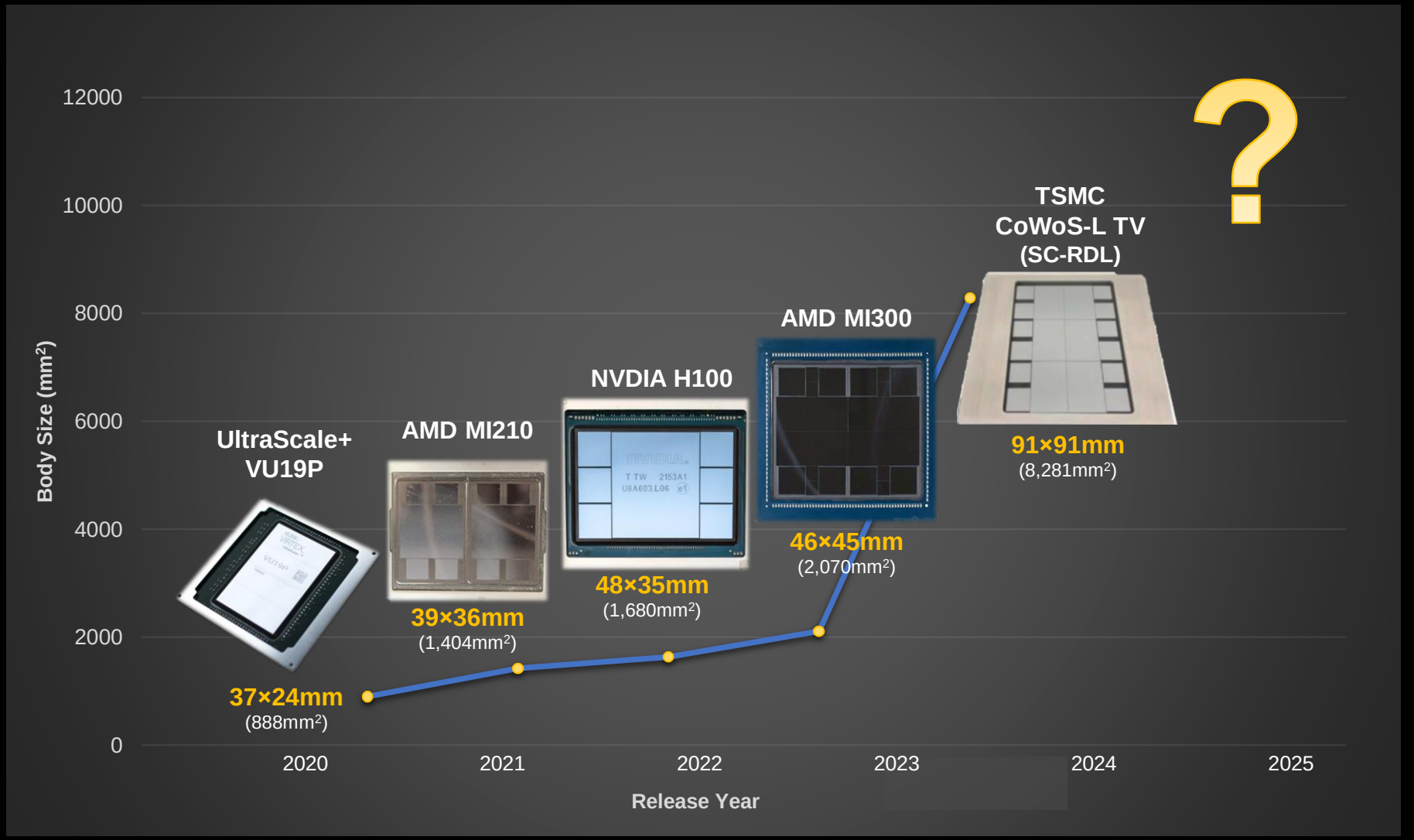


AMD MI300
13 chiplets + 8 HBM



Intel Ponte Vecchio
39 chiplets + 8 HBM

AI driving an explosion in package size



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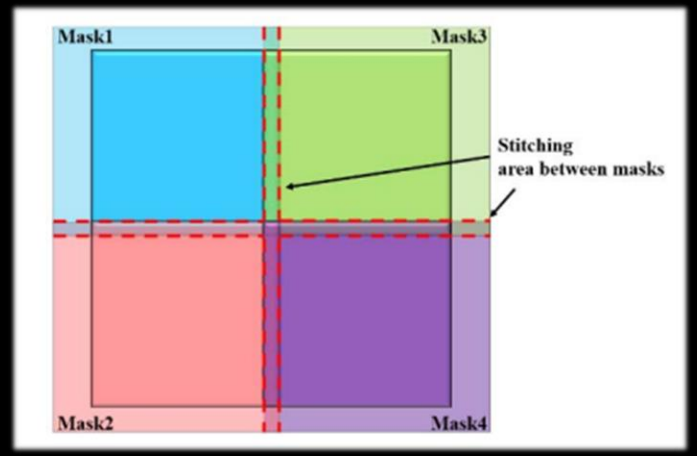
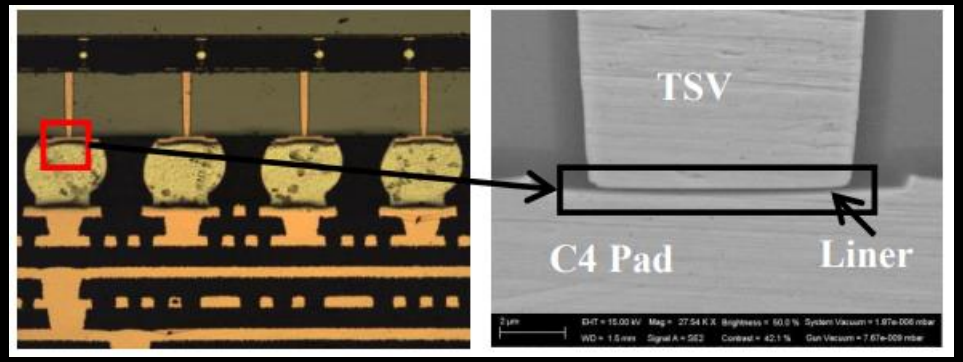
Transition away from Si Interposers

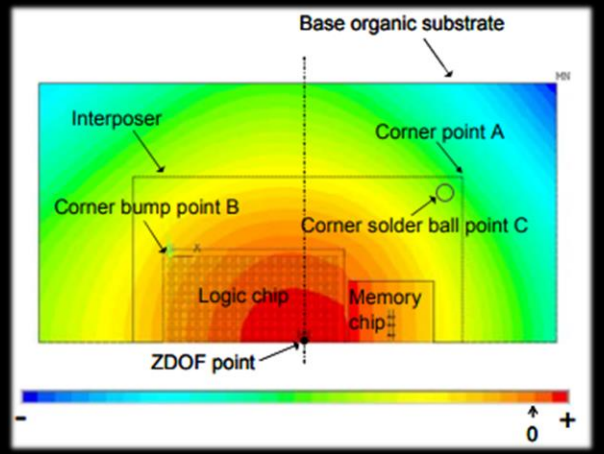
- Key challenges driving the change:
  - Overlay control very difficult for ≥4x mask reticle stitching for large packages[1]
  - Si interposer warpage & scaling to finer pitch[2]
  - CTE mismatch between Si interposer & organic substrate[3]
  - Package co-planarity across temperature range for PCB mounting[1]



4x mask reticle stitching of 5th Gen CoWoS-S



TSV to C4 bump pad open defect due to Si wafer warpage during CMP



Package warpage simulation of Si-interposer

[1]" Wafer Level System Integration of the Fifth Generation CoWoS-S with Performance Si Interposer at 2500mm²". P.K. Huang, et.al. (TSMC), ECTC, 2021

[2]"Assembly Challenges in Developing 3D IC Package…", R. Chaware, et.al. (Xilinx, TSMC), ECTC, 2015

[3]"Study of Warpage and Mechanical Stress of 2.5D Package Interposers…", T. Hisada, et.al. (IBM Japan), IMAPS Symposium on Microelectronics, 2012

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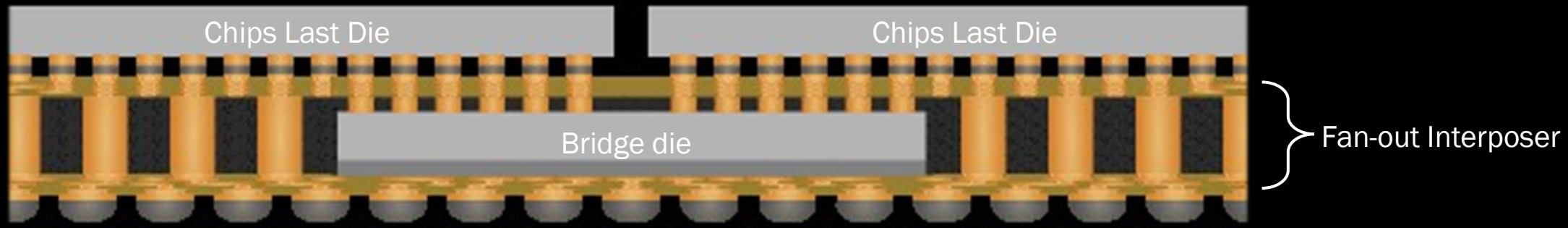
Shift to Fan-out Technology

What?

- Break up the monolithic Si interposer into smaller manageable pieces having high-density interconnects - Si bridge die
- Embed the Si bridge die into a molded fan-out interposer

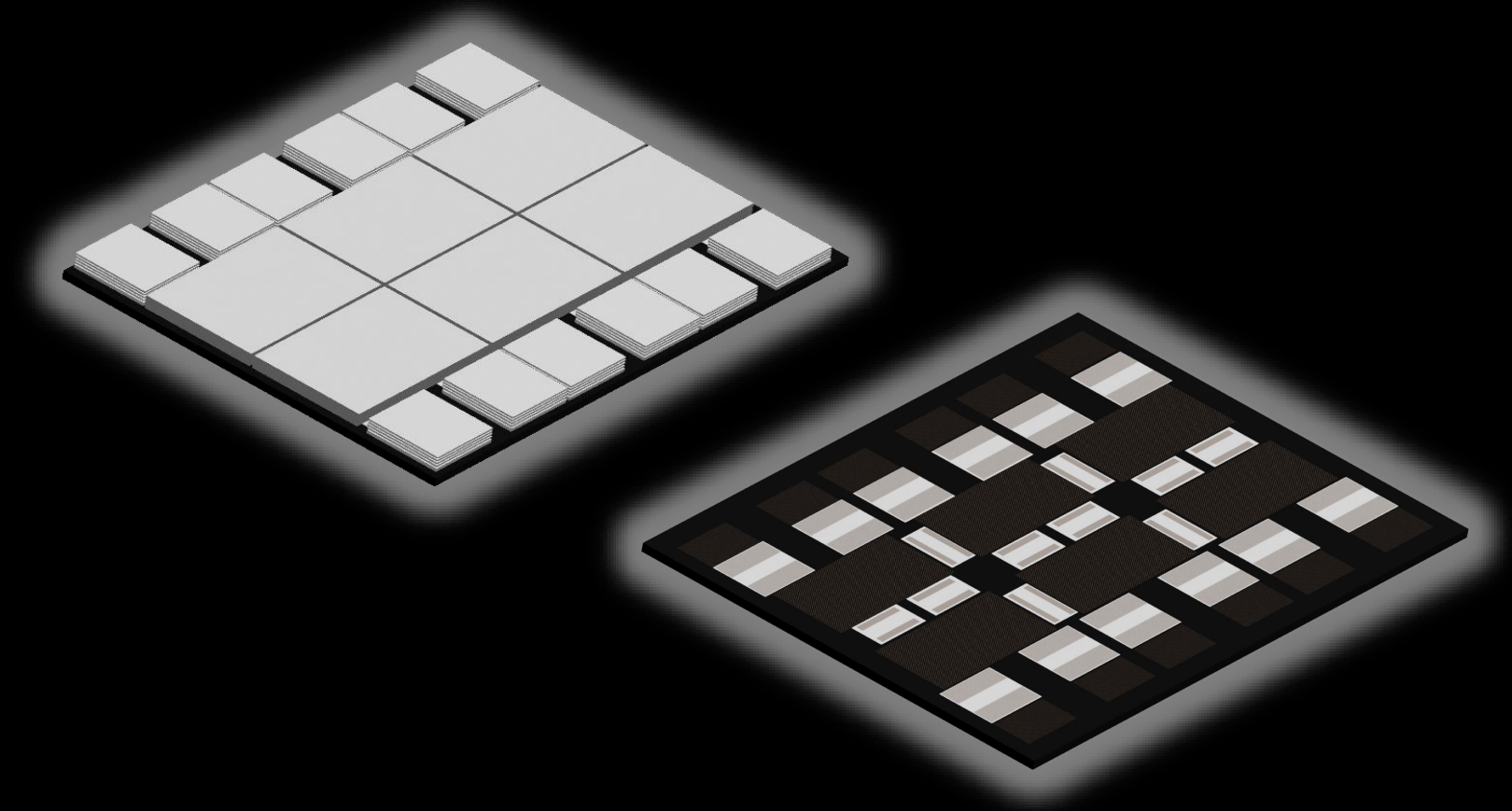
Why?

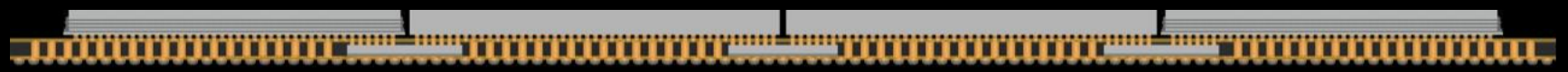
- Provides high-density interconnect where it's needed
- Composite EMC & bridge die reduces impact of CTE mismatch
- Clear path to larger formats (e.g. 600×600mm)



M-Series Embedded Bridge Fan-out Interposer

Application Example: 12 HBM3 Fan-out Interposer (>3,800mm^2)





Example cross-section (not to scale)

- 48mm x 80mm embedded bridge interposer
- 12 embedded bridges for HBM3
  - ~9.5 x 7.5 mm
  - 73 µm HBM3 pitch
  - 43.5 x 55 µm PHY pitch
- 10 embedded die-to-die bridges
  - 35 µm pitch on processors
  - 3 x 8 mm & 3 x 5 mm
- Integrated embedded components
  - Passive devices embedded in the interposer
  - Roadmap to active devices (e.g. V-reg)

HBM3 Interface

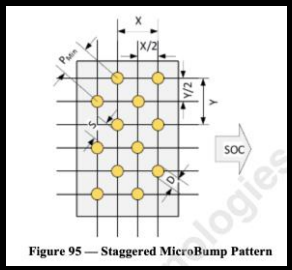


Figure 95 — Staggered MicroBump Pattern

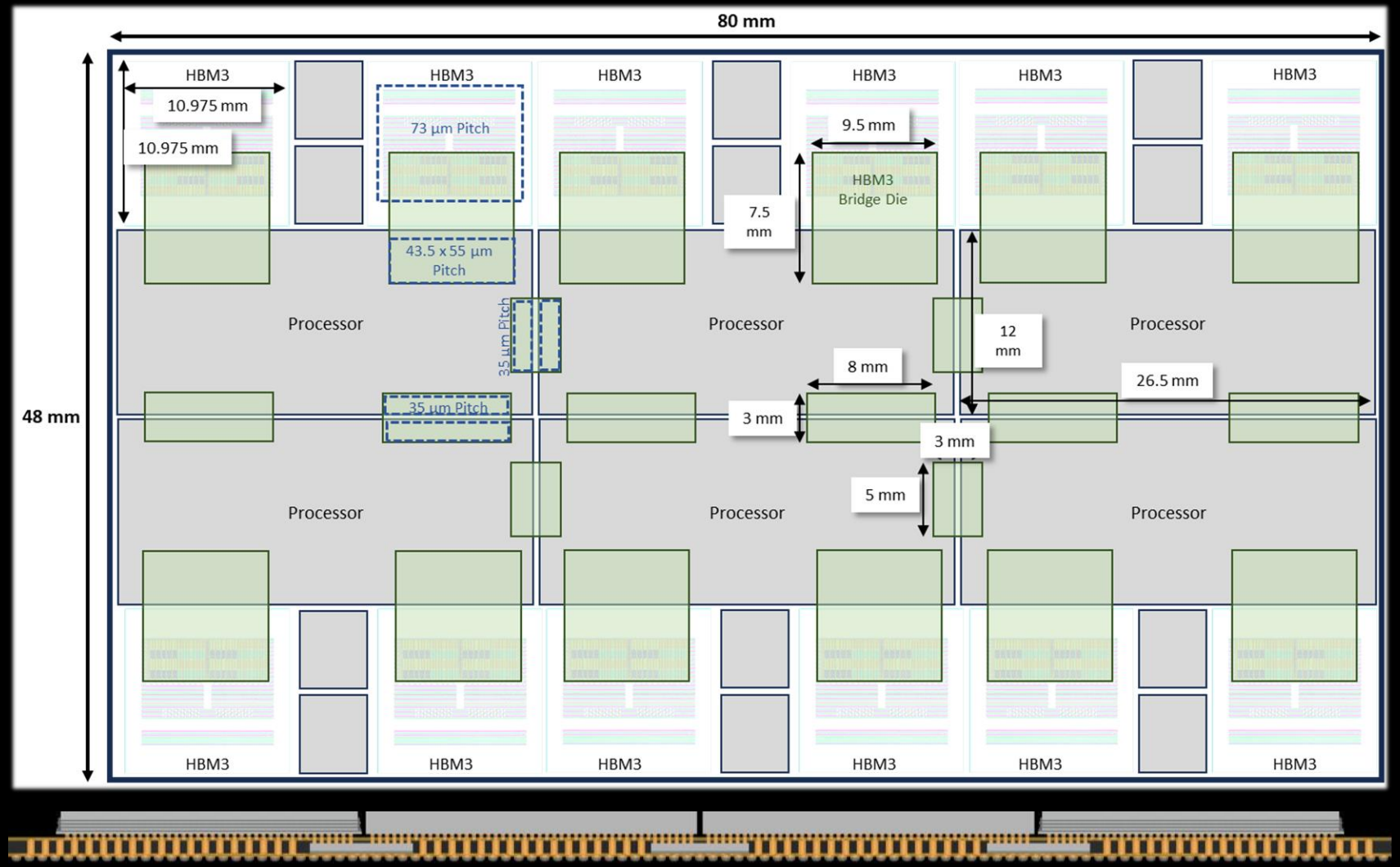
Table 95 — Geometric Parameters of the Staggered MicroBump Pattern

Label	Nominal Value	Description
X	96 um	Horizontal pitch of two adjacent MicroBumps
Y	110 um	Vertical pitch of two adjacent MicroBumps
P_{Min}	73 um	Minimum pitch of the bump field
D	28 um	MicroBump diameter
S		Bump-to-bump air gap; $S = P_{Min} - D$

Note: Patents issued & pending on structures & methods

M-Series Embedded Bridge Fan-out Interposer

22 Embedded Bridge Die – Test Vehicle Design Proposal



12 HBM3 Fan-out Interposer

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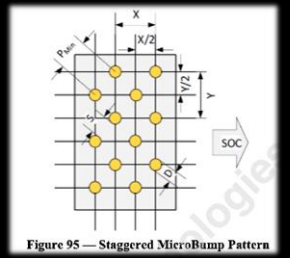

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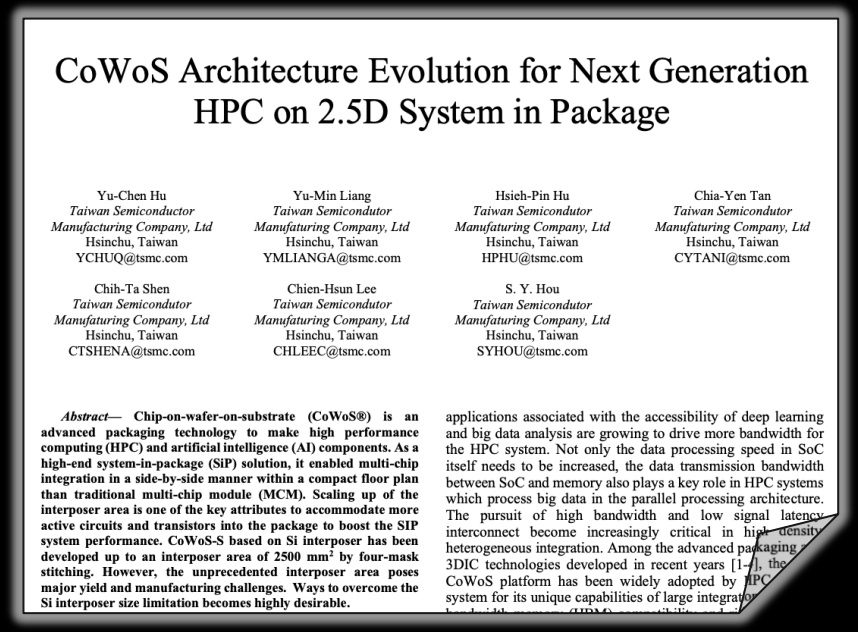
TSMC CoWoS adopts embedded bridge fan-out for > 3X reticle size

*CoWoS-L announced at ECTC 2023**



CoWoS Architecture Evolution for Next Generation HPC on 2.5D System in Package

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Yu-Min Liang, *Taiwan Semicondutor Manufacturing Company, Ltd*, Hsinchu, Taiwan, YMLIANGA@tsmc.com
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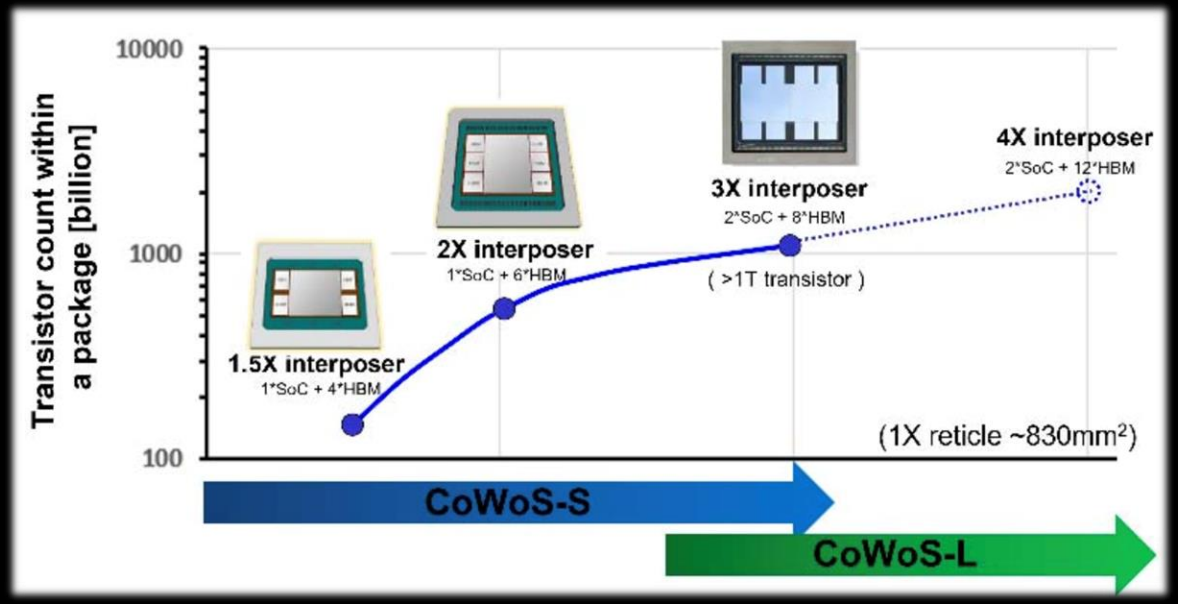
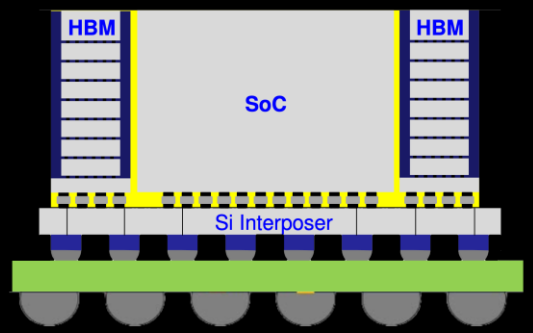
Chia-Yen Tan, *Taiwan Semicondutor Manufacturing Company, Ltd*, Hsinchu, Taiwan, CYTANI@tsmc.com
Chih-Ta Shen, *Taiwan Semicondutor Manufacturing Company, Ltd*, Hsinchu, Taiwan, CTSHENA@tsmc.com
Chien-Hsun Lee, *Taiwan Semicondutor Manufacturing Company, Ltd*, Hsinchu, Taiwan, CHLEEC@tsmc.com
S. Y. Hou, *Taiwan Semicondutor Manufacturing Company, Ltd*, Hsinchu, Taiwan, SYHOU@tsmc.com

***Abstract*— Chip-on-wafer-on-substrate (CoWoS®) is an advanced packaging technology to make high performance computing (HPC) and artificial intelligence (AI) components. As a high-end system-in-package (SiP) solution, it enabled multi-chip integration in a side-by-side manner within a compact floor plan than traditional multi-chip module (MCM). Scaling up of the interposer area is one of the key attributes to accommodate more active circuits and transistors into the package to boost the SIP system performance. CoWoS-S based on Si interposer has been developed up to an interposer area of 2500 mm² by four-mask stitching. However, the unprecedented interposer area poses major yield and manufacturing challenges. Ways to overcome the Si interposer size limitation becomes highly desirable.**

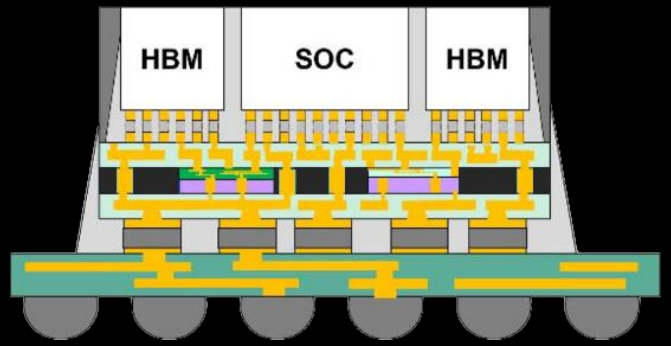
applications associated with the accessibility of deep learning and big data analysis are growing to drive more bandwidth for the HPC system. Not only the data processing speed in SoC itself needs to be increased, the data transmission bandwidth between SoC and memory also plays a key role in HPC systems which process big data in the parallel processing architecture. The pursuit of high bandwidth and low signal latency interconnect become increasingly critical in high density heterogeneous integration. Among the advanced packaging 3DIC technologies developed in recent years [1-], the CoWoS platform has been widely adopted by HPC system for its unique capabilities of large integrator



Silicon Interposer
CoWoS-S



Molded Bridge Interposer
CoWoS-L



CoWoS moving away from Si interposer to molded bridge die fan-out

*"CoWoS Architecture Evolution for Next Generation HPC on 2.5D System in Package". Y.C. Hu, et.al. (TSMC), ECTC, 2023

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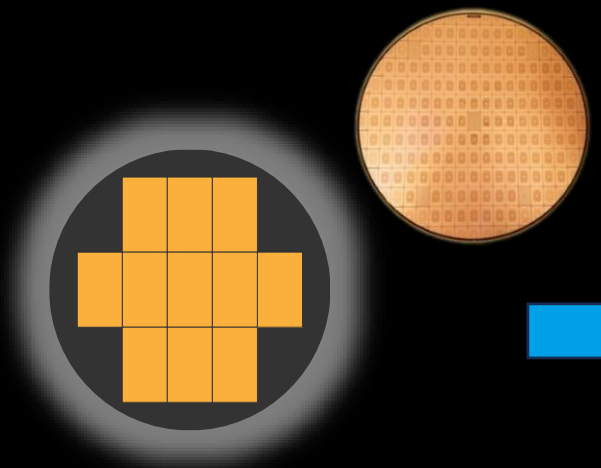
Scaling up to 600mm large panel for growing body sizes

600mm is a semi standard (SEMI 3D20)

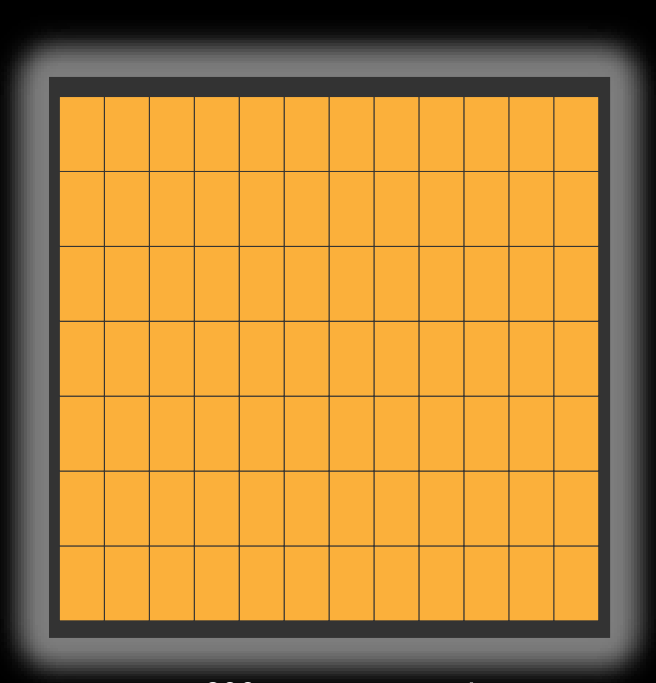
- 600mm x 600mm delivers:
  - 500% increase in active area (vs. 300mm round)
  - Estimated 25% reduction in the cost of capital per unit output
  - Estimated 15% reduction in the cost of materials (higher utilization of PI & PR)
  - Projected 20% base cost reduction vs. 300mm round
- Example: 48mm x 80mm body size (3,840mm^2)

When considering area efficiency, potential for up to 40% savings



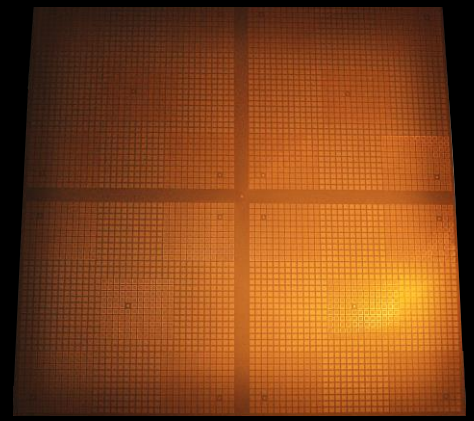
300mm round wafer

60% area efficiency*
11 packages



600mm square panel

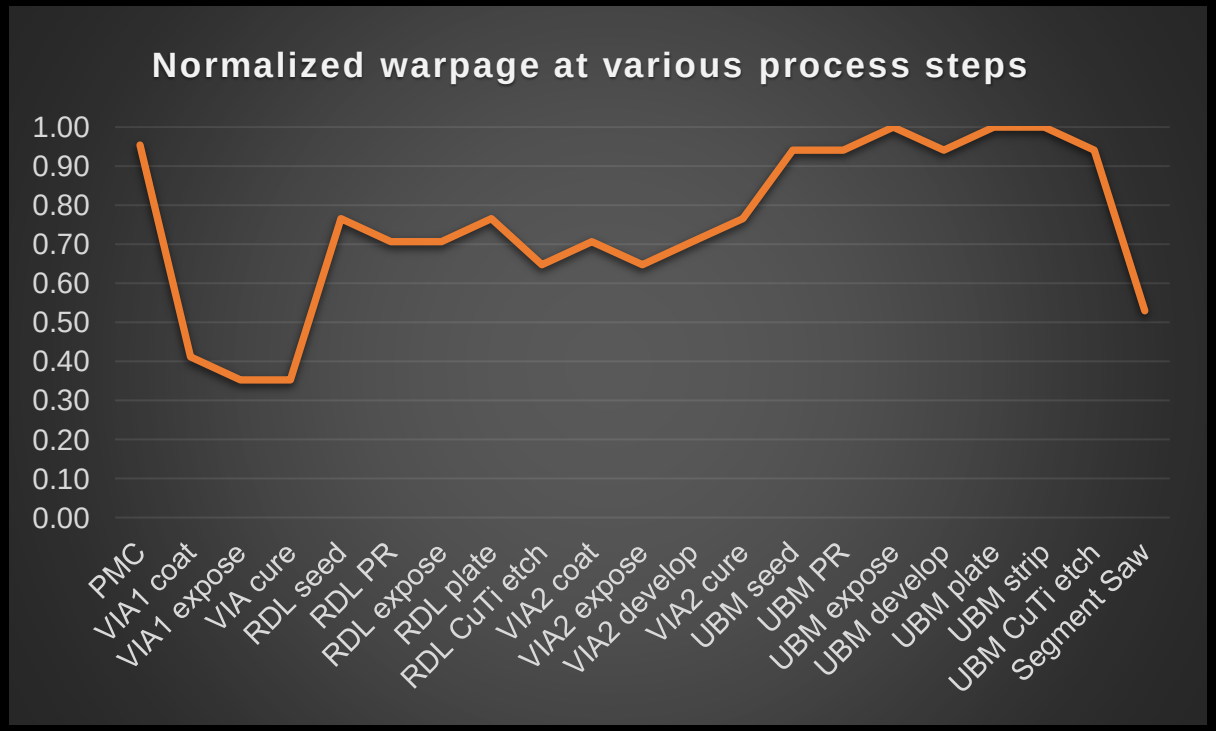
90% area efficiency*
84 packages



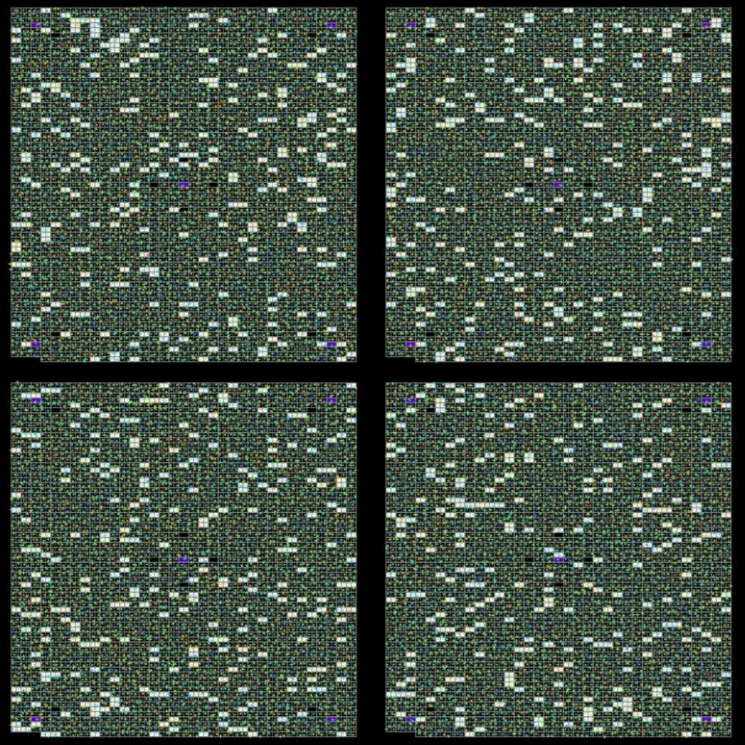
*Area efficiency = area of potential packages per panel ÷ panel active area

Key Challenges of Large Panels

- Handling panel level warpage & sag
- Improving process yield
- Critical dimension (CD) control
- Technology maturity
- Die shift



M-Series FOPLP warpage data

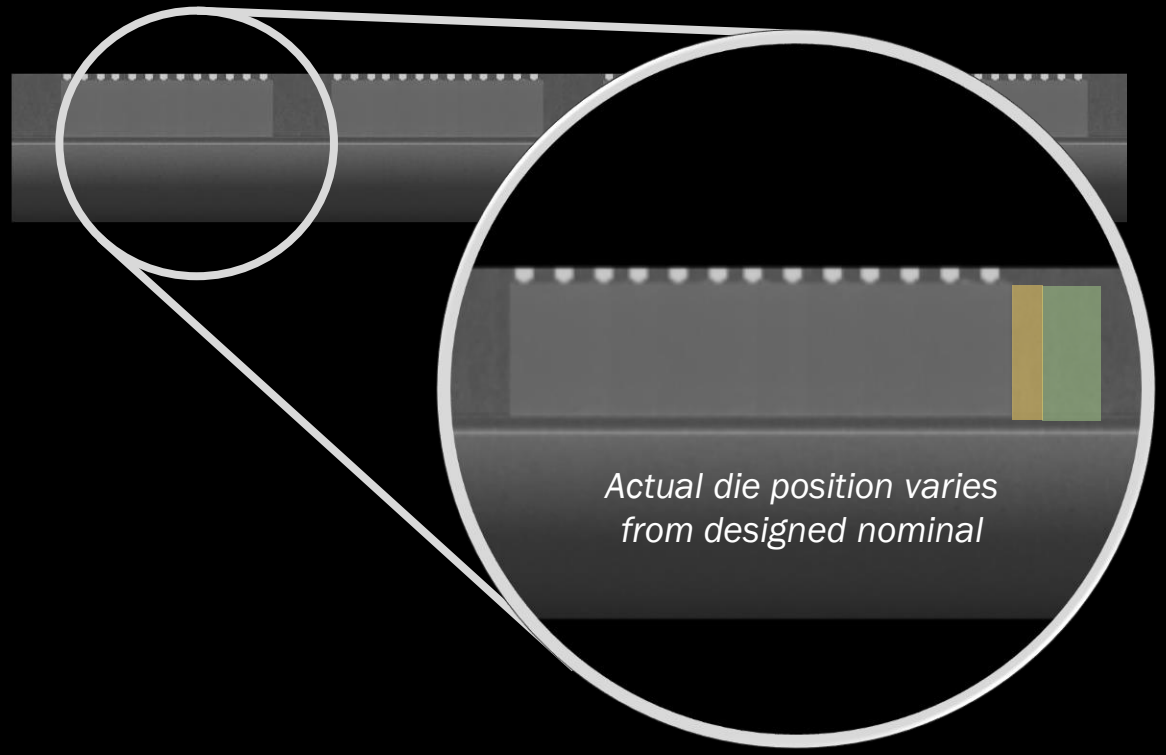


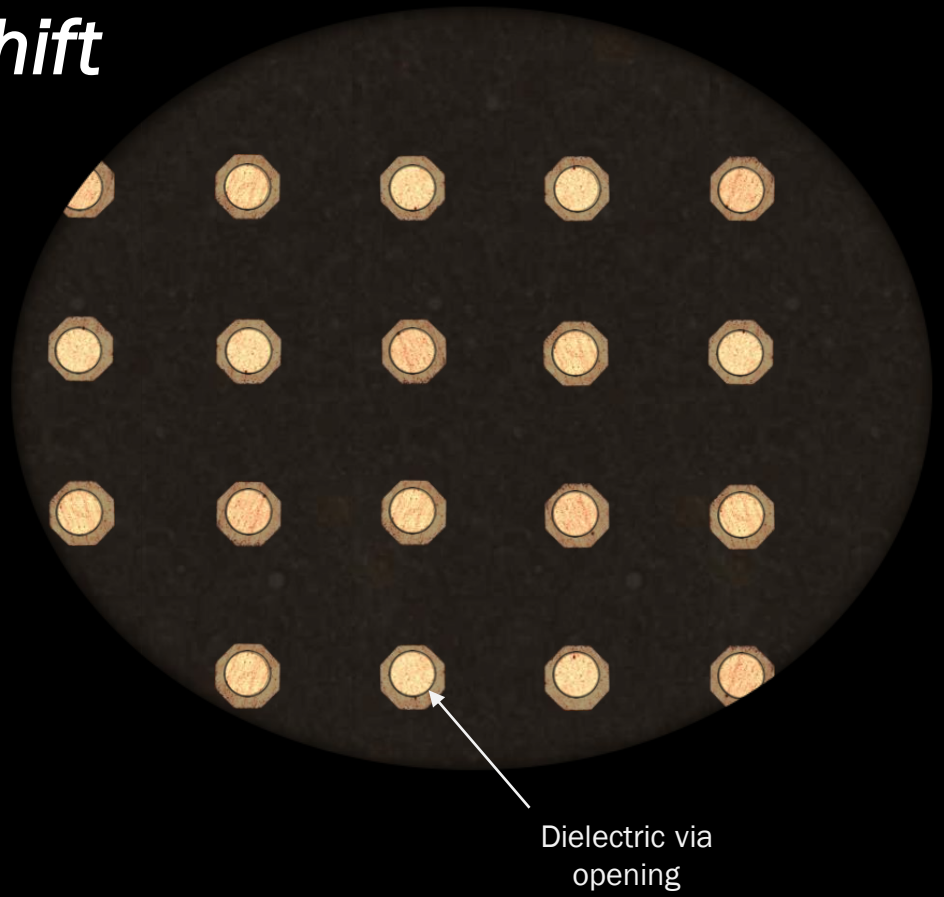
M-Series FOPLP die shift data

#1 Challenge in embedded devices – Die shift

1. Variation in mechanical placement of die

2. Displacement during encapsulation (molding)



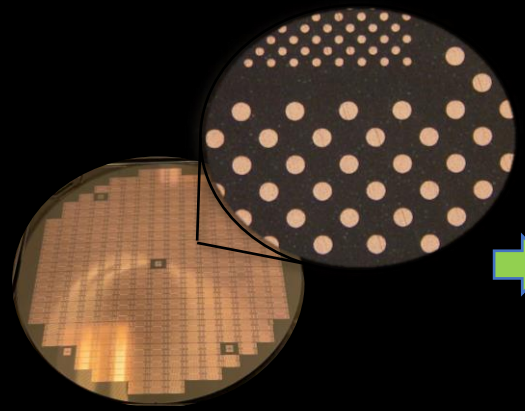


Solving die shift with Adaptive Patterning (AP)

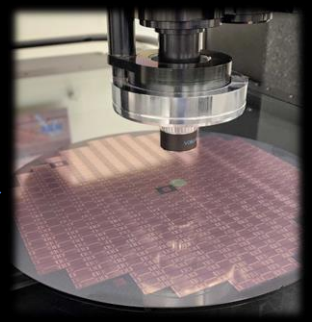
Adaptive Patterning™

→ Unique lithography optimized to account for die shift on every device on every wafer or panel

Adaptive Patterning Process Flow

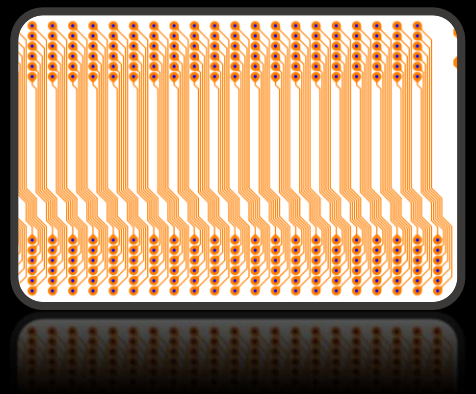


Measure actual die position using high-speed optical scanner



Sr. No.	XCenter Act.	YCenter Act.	Angle Act.
1	-128506.06	-52200.061	0.086113
2	-128505.26	-64489.845	0.049008
3	-128506.23	-46120.433	0.093464
4	-128505.41	-39914.371	0.12255
5	-128506.21	-33833.133	0.047414
6	-128507.24	-21546.428	0.150841
7	-128506.04	-15340.473	0.082432
8	-128506.51	-9260.5775	0.041291
9	-128506.02	3025.84524	0.10377
10	-128505.58	9232.34242	0.112701
11	-128507.17	15313.5118	0.083535
12	-128506.64	27598.1797	0.098358
13	-128506.61	33806.508	0.038946
14	-128507.06	39887.662	0.062364
15	-128506.74	52174.2068	0.110017
16	-128507.54	58383.4965	0.08775

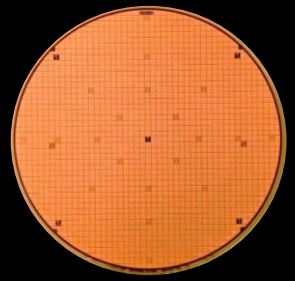
Die measurement data



Dynamically generate lithography pattern

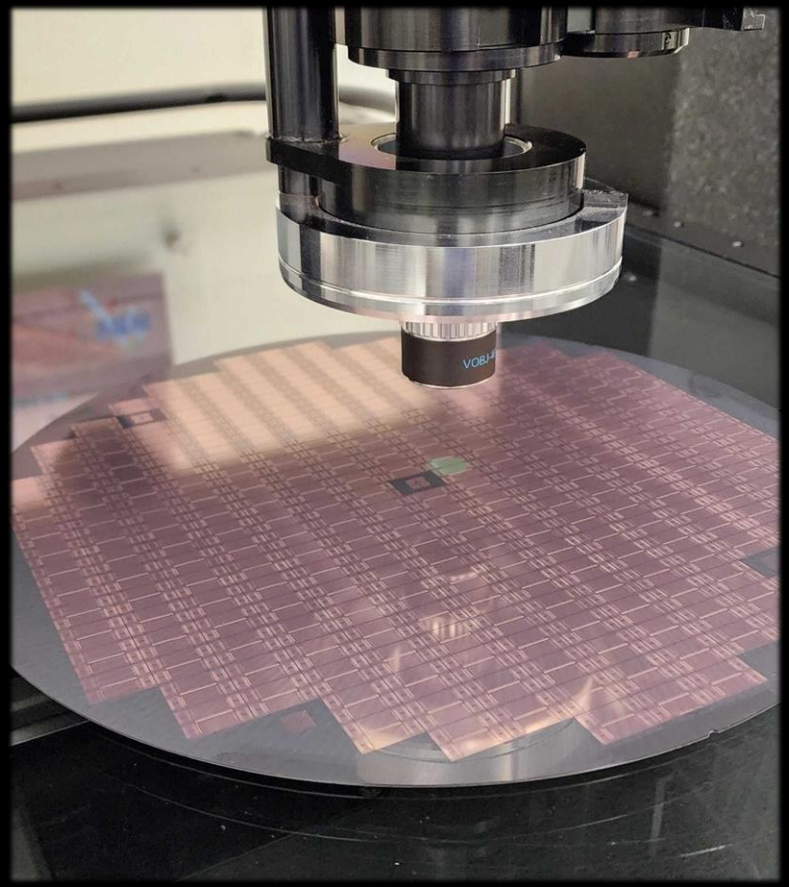
ENGINE

LDI Expose tool



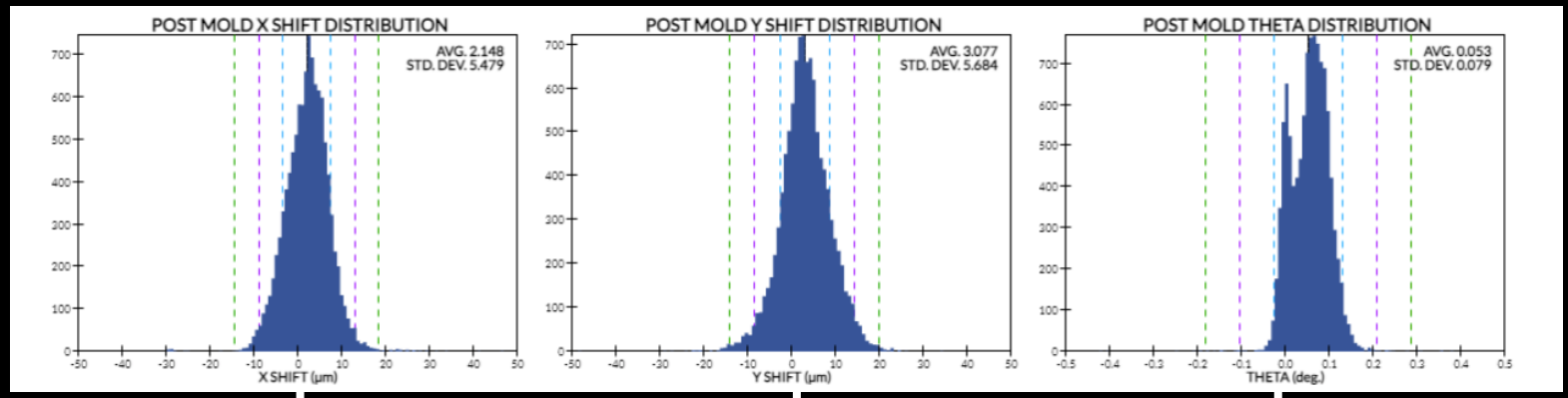
Unique lithography pattern per wafer
(no reticle size limitations)

Step #1 - Die Measurement *(data from Gen 2 M-Series TV*)*

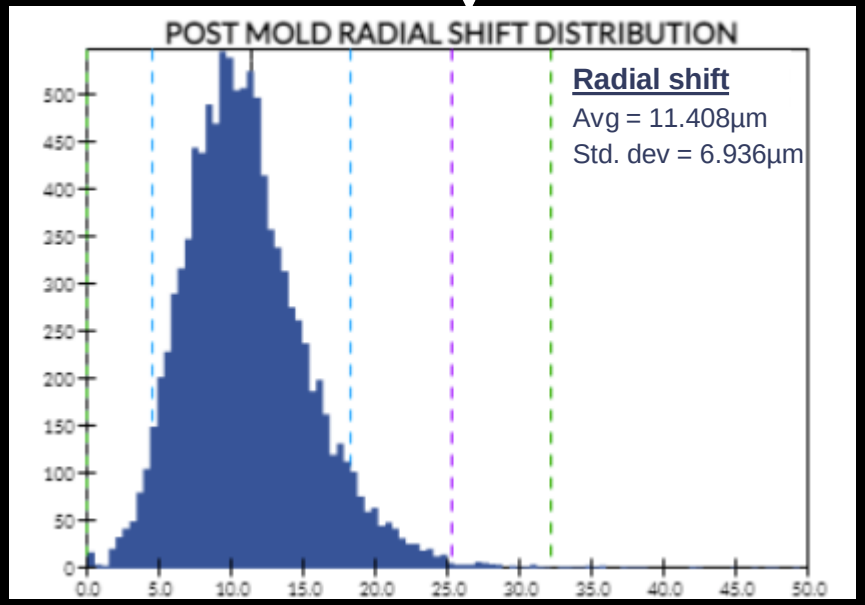


DMS = High speed precision X, Y, and Θ measurement of each device

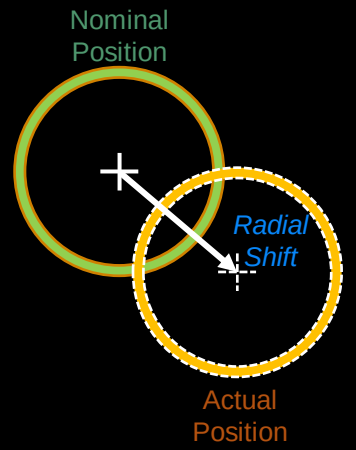
X, 5σ = 27.4µm **Y, 5σ = 28.4µm** **θ, 5σ = 0.04°**



X, Y, Θ combined to radial shift



Radial Shift

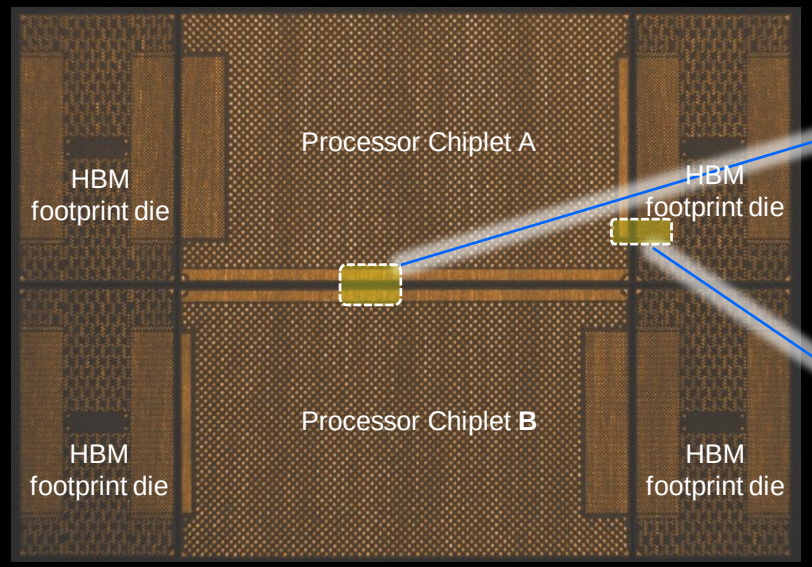


Typical DMS precision
≤ 0.5µm @ 3σ

*"Integrating Chiplets using Chips First UHD Fan-out...", B. San Jose, C. Sandstrom, T. Olson, et.al. ECTC 2023

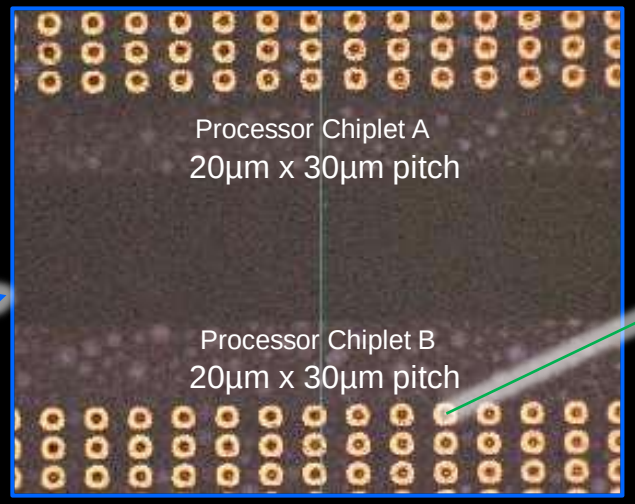
Step #3 – LDI PI dielectric exposure

Vias perfectly aligned to Cu studs (die pad contacts) using Adaptive Patterning

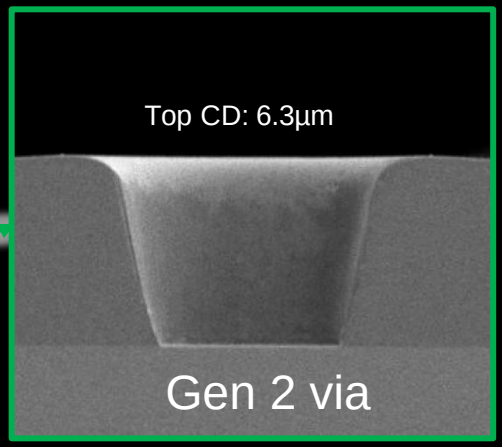


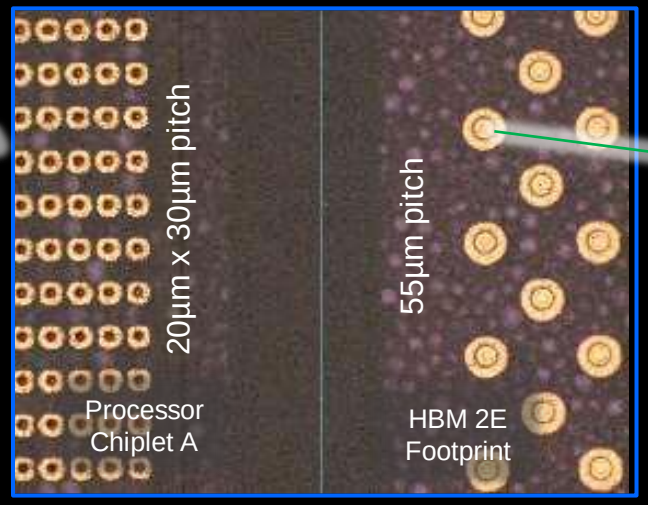
Layout of Gen 2 Test Vehicle

*"Integrating Chiplets using Chips First UHD Fan-out…", B. San Jose, C. Sandstrom, T. Olson, et.al. ECTC 2023

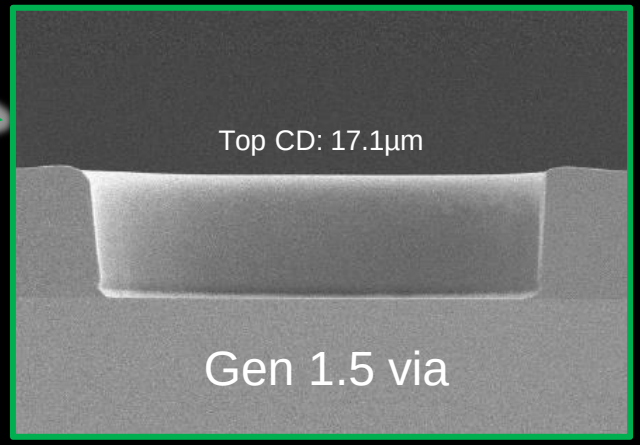


Gen 2 vias on 12µm Cu studs

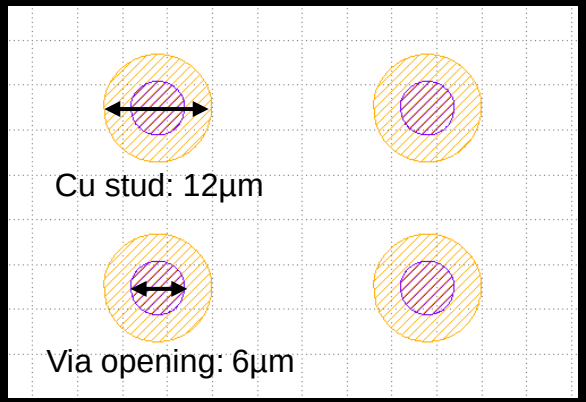




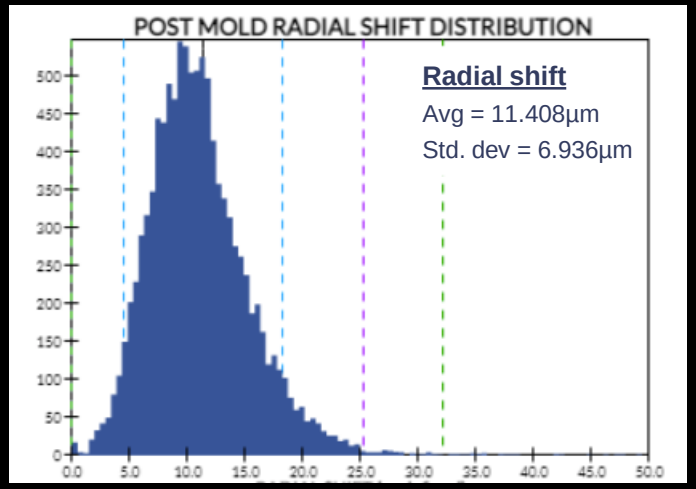
Gen 1.5 vias



Step #3 – LDI PI dielectric exposure (reduction of radial shift)

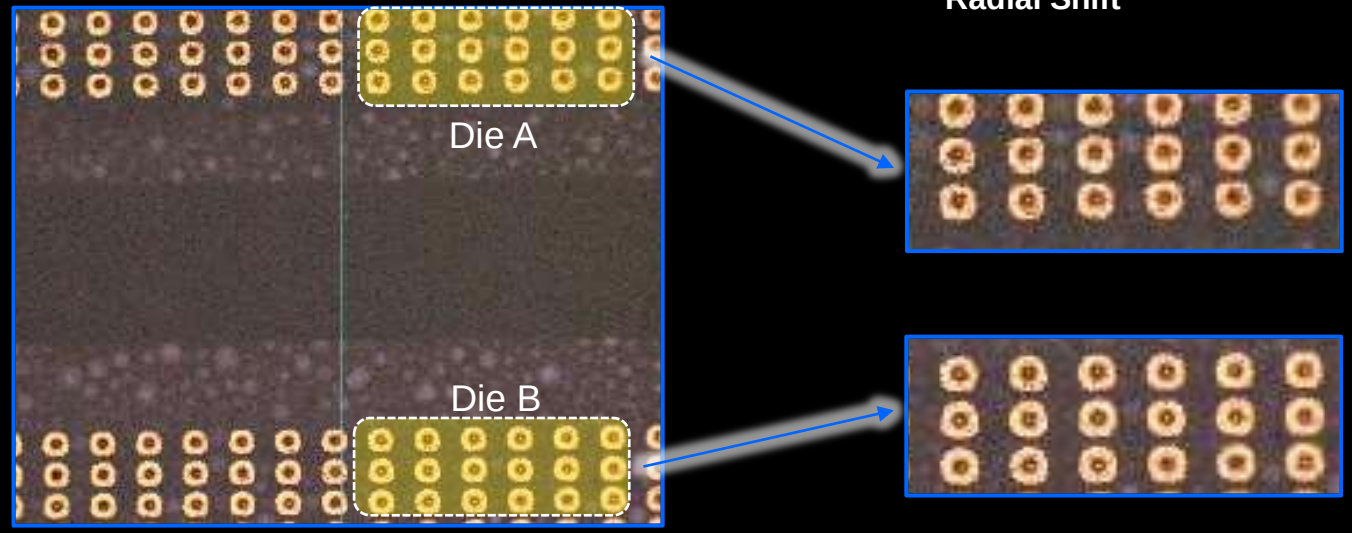


20×30µm pitch design



Radial Shift

Up to 35µm of radial shift can be compensated



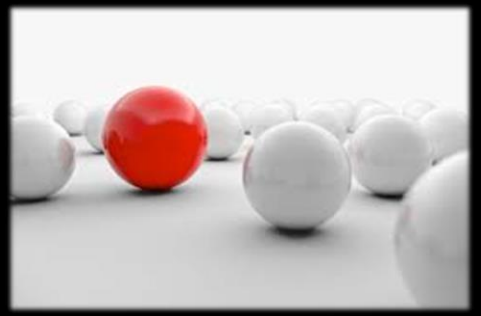
Interface A: Via opening image

Adaptive Patterning effectively removes the radial shift with precise alignment of all features from 35µm → 1.2µm

Outline

- Background
- How to manage increasing package sizes
  - Transition away from Si interposers
  - Shift to Fan-out technology
  - Advance toward large panel
  - Extend Adaptive Patterning
- Conclusion

Extend Adaptive Patterning



Deming's Red Bead Game

Dr. Deming's System of Profound Knowledge

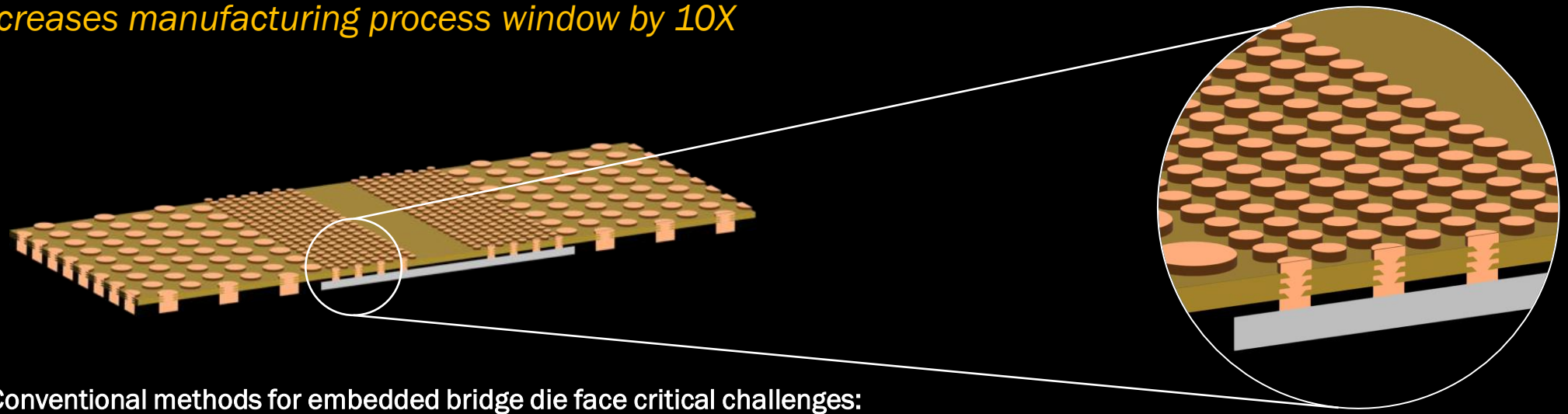
"Life is variation, variation there will always be"

W. Edwards Deming
1900 - 1993

- Adaptive Patterning was created from a completely new mindset – to accommodate vs. fight natural variation
- Real-time design-during-manufacturing for every wire on every device on every wafer
- Adaptive Patterning solves the most critical challenge for fan-out: die shift

M-Series Embedded Bridge (with Adaptive Pad Stacks)

Increases manufacturing process window by 10X



Adaptive Pad Stacks in cross-section

Conventional methods for embedded bridge die face critical challenges:

- Requires tight ±1µm or less bridge die location as fabricated
- Bridge die size limited due to rotation criticality
- Scaling number of bridge die presents significant yield challenge

The new Adaptive Pad Stacks technique uses Adaptive Patterning (AP) to solve these challenges:

- Adapts RDL layer patterns to ensure highly manufacturable product
- Compensates for each bridge die independently, improving yield for interposers with growing number of bridge die
- Allows continual scaling down in flip chip pitch

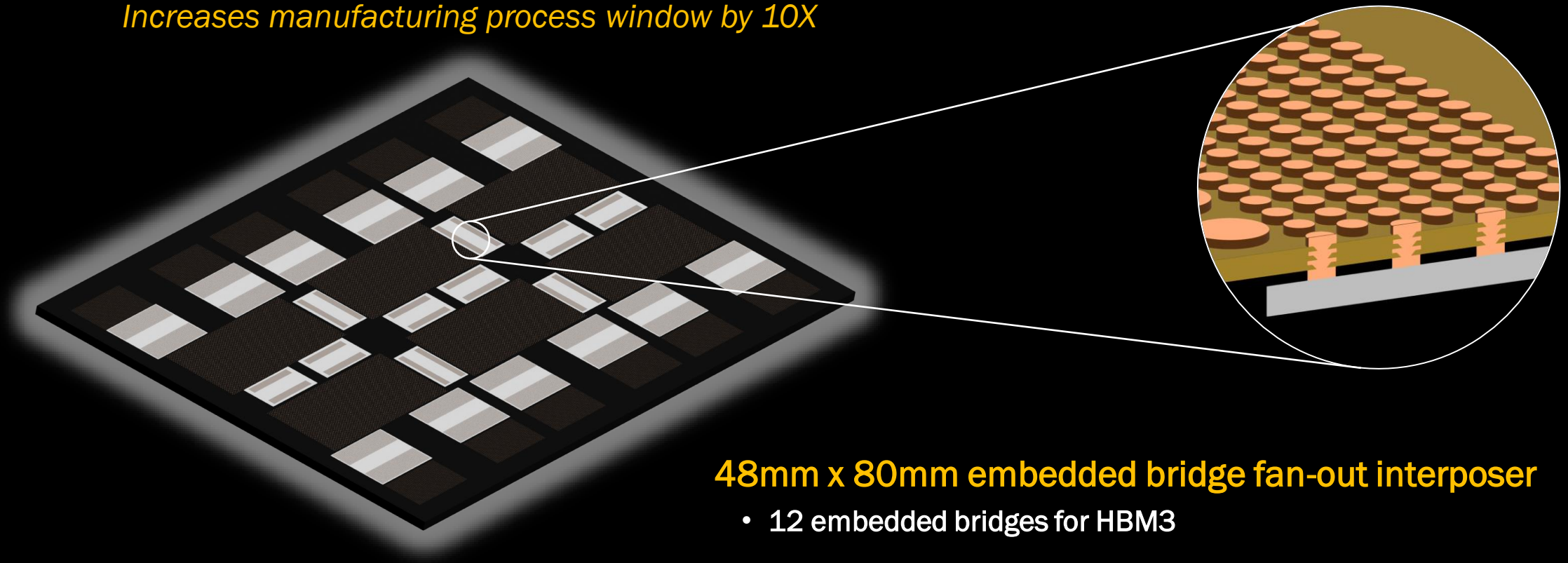
Adaptive Pad Stacks allow wide manufacturing tolerances

	Flip chip pitch	Bridge die position tolerance	
		XY @ 3σ	Θ @ 3σ
Gen 1.5	35 µm	±12 µm	±0.1°
	45 µm	±20 µm	±0.2°
Gen 2	20 µm	±10 µm	±0.1°
	25 µm	±15 µm	±0.1°
	35 µm	±25 µm	±0.25°
	45 µm	±40 µm	±0.4°

Deca (10x) increase in manufacturing tolerance for 100% yield

M-Series Embedded Bridge (with Adaptive Pad Stacks)

Increases manufacturing process window by 10X



48mm x 80mm embedded bridge fan-out interposer

- 12 embedded bridges for HBM3
- 10 embedded die-to-die bridges

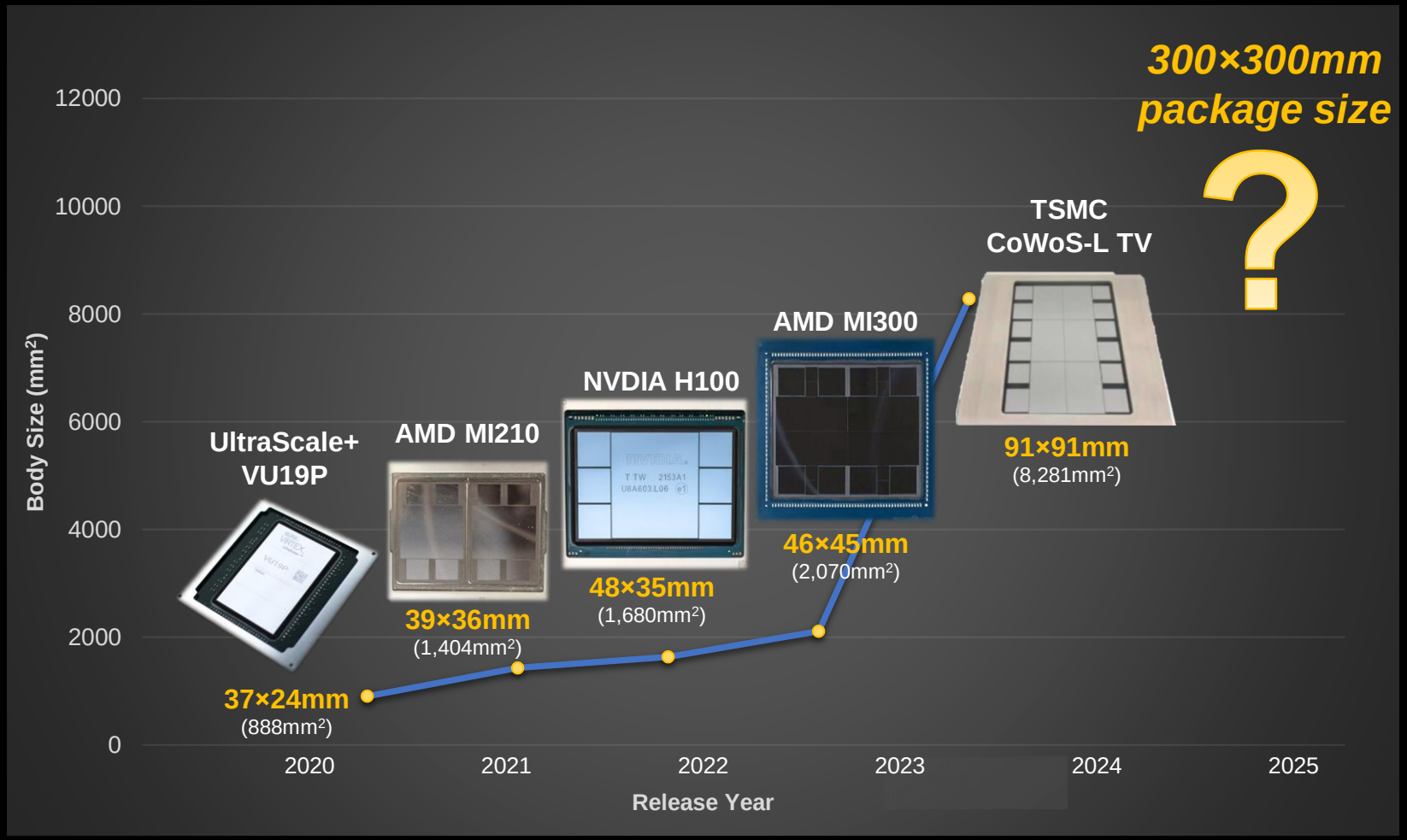
Adaptive Pad Stacks allows continual scaling to larger & larger package sizes

Outline

- Background
- How to manage increasing package sizes
  - Transition away from Si interposers
  - Shift to Fan-out technology
  - Advance toward large panel
  - Achieve technology breakthroughs
- Conclusion

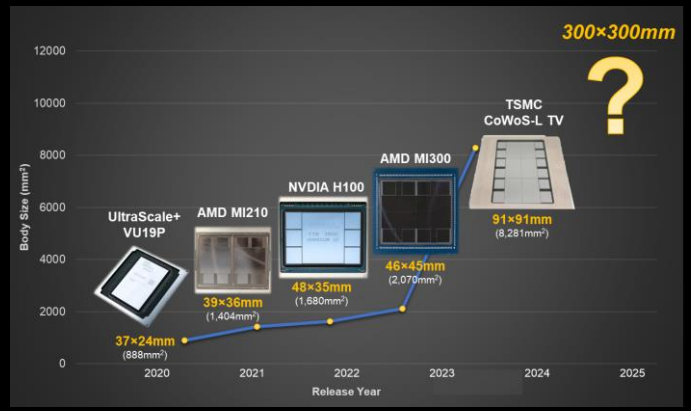
Conclusion

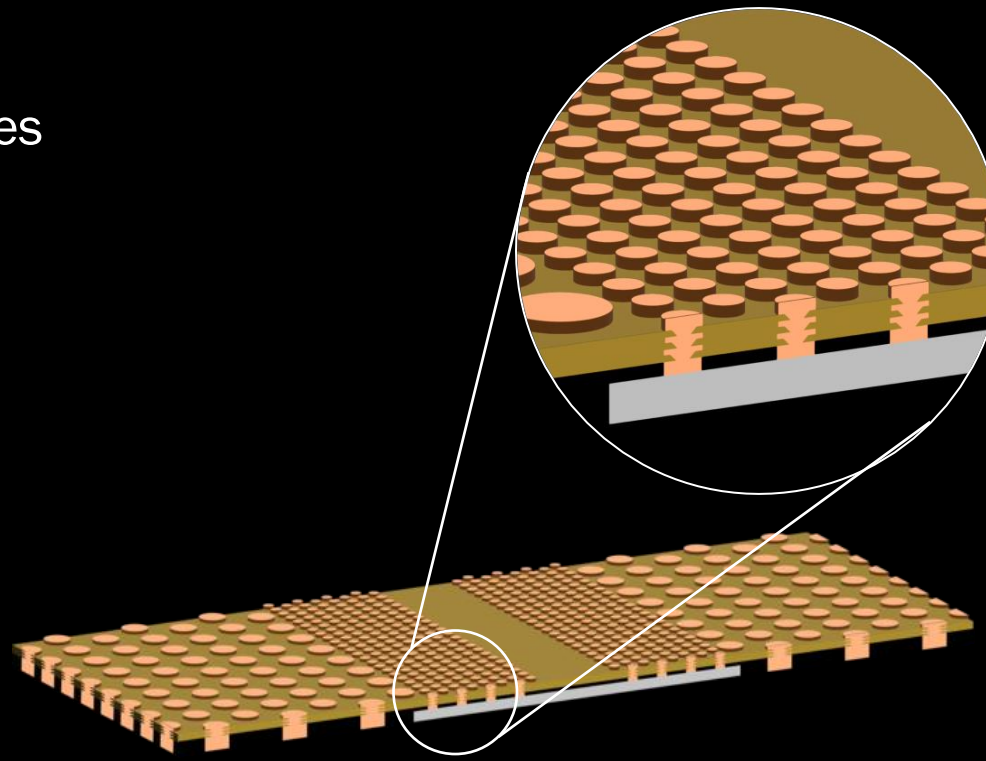
- The industry is moving to larger and larger package sizes



Conclusion

- The industry is moving to larger and larger package sizes
- With this trend, overcoming challenges is key
- Trend toward large panel Fan-out technology
- Deliver Adaptive Pad Stacks





Expand What's Possible

Thank you

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