Scalable Core Package for Power module with Double-Sided Cooling Capability Applying Fan-out Panel-Level Process Suitable for SiC and GaN

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Outline

1. Background

2. Introduction of Our Core Power Module Package

3. Trial Production and Evaluations for a Prototype

- Prototype package structure
- Manufacturing locations
- Process flow
- Simulation analysis (Thermal stress and heat dissipation)
- Results of prototype

4. Summary

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Background

■ Applications : Power Supply Systems

Source : KYOCERA

Source : e-Mobility Power

Source : TOYOTA

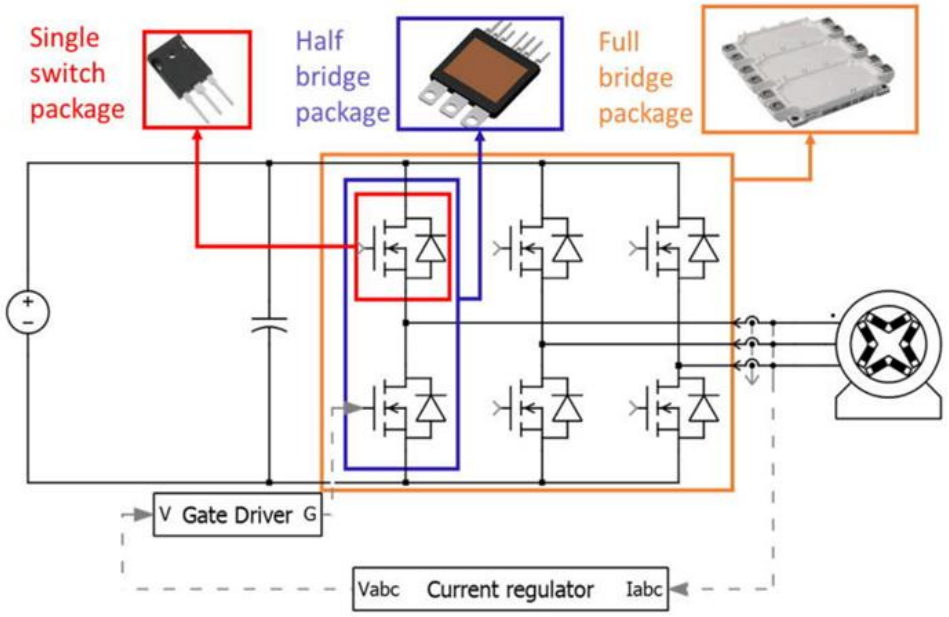
- ✓ Recently, the demand for electric vehicles (EVs), charging infrastructure, and renewable energy has been expanding toward energy conservation and a low-carbon society.
- ✓ Power consumption is increasing year by year, and there is an urgent need to reduce the energy loss generated during power conversion.
- ✓ There is growing interest in Silicon Carbide (SiC) and Gallium Nitride (GaN) wide bandgap semiconductors, which offer advantages such as high temperature operation, high-speed operation and low on-resistance.

Background

■ Packaging Technologies

Several SiC inverter modules (packages) have been proposed, but further concept development is needed in terms of heat dissipation, high current, parasitic resistance, inductance and scalability.

Current module (package) trends at other IDM and OSAT



Source：IEEE/Comprehensive_Review_and_State_of_Development_of_Double-Sided_Cooled_Package_Technology_for_Automotive_Power_Modules

Case module (package) type

- *High customizability*
- *Complicated wiring*
- *Thinning down is limited due to wire loops*
- *Wire bonding junction failure in reliability*

Discrete type

- *Larger mounting space*
- *Need many packages (Cost)*

Background

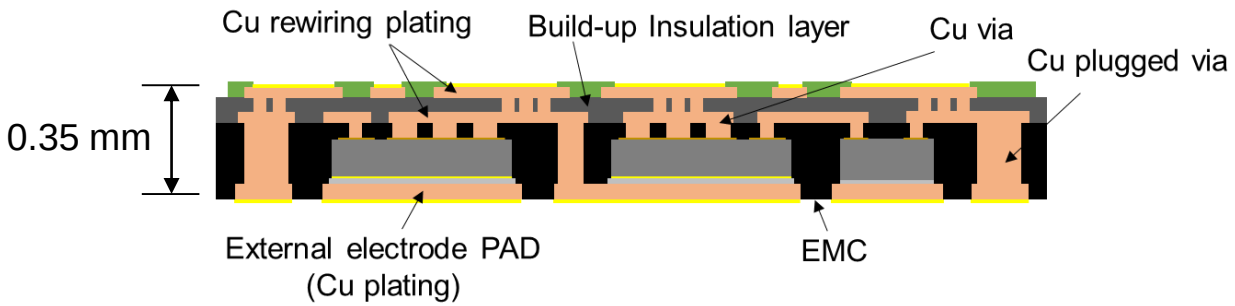
■ Packaging Technologies

We focus on power module packages with chip embedded technology

- *Higher power (current) density*
- *Low parasitic resistance and inductance due to short interconnections*
- *Miniaturization*
- *Thinner*
- *Excellent double-sided cooling concept*
- *Robust interconnection technology(no wire-bonding)*
- *Higher scalable integration*

Previous report) Our chip-embedded structure presented at the last DPC2023

DC-DC half-bridge application



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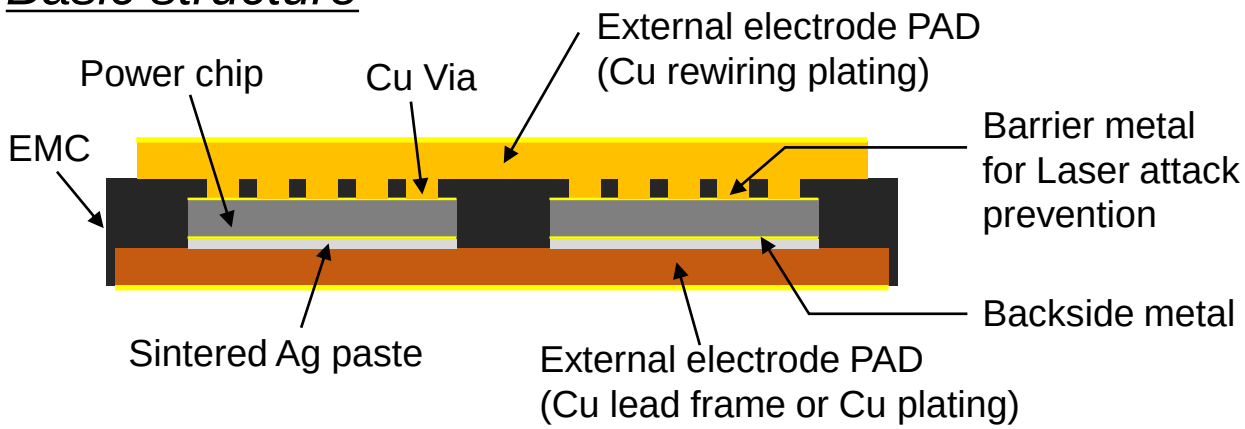
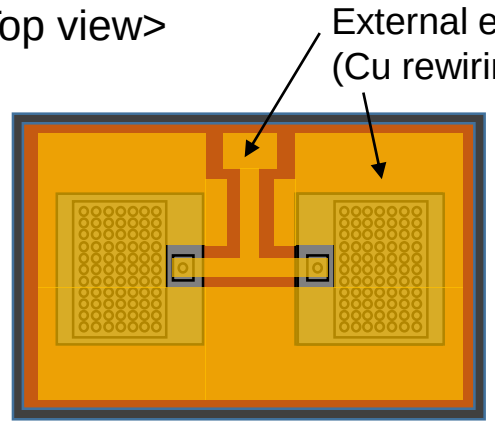
Introduction of Our Core Power Module Package

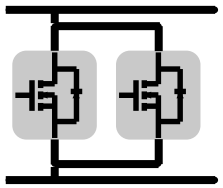
Proposal for Core Power Module Package using chip-embedded technology with high scalability for inverter applications

Basic structure



<Top view>





Power chip
Parallel connection ;
2, 3, … N parallel

Features

- Core power module package uses a semi-additive fan-out panel-level process (FOLP ® technology) customized for power applications.
- Cost-effective 300 mm square panel manufacture format.
- Uniquely epoxy coreless substrate and chip embedding technology.
- High current density by power chiplet like (chip parallel connection) technology
- Robust Cu-plated (Via and rewiring) interconnect technology.
- Enhanced High heat dissipation, High current density, low resistance and inductance.
- Integrated in-house production from panel substrate to package assembly.

Actual panel after molding

300 mm square panel format

Introduction of Our Core Power Module Package

■ Core power module Variations

- ***Core power module with high thermal conductivity and high voltage insulation layer***

Insulation layer (Epoxy based)

・High dielectric voltage ; 4.2kV/100μm
・High thermal conductivity ; ～6W/m・k

✓ ***Lower warpage and stress than conventional DBC***
✓ ***Smaller and thinner than conventional DBC***

- ***Double side direct Cu plating connection structure***

Direct Cu connection to SiC chip
(without solder and sintered Ag paste)

✓ ***Improved BLT, spread, and void control issues***
✓ ***Lower resistance and higher heat dissipation***

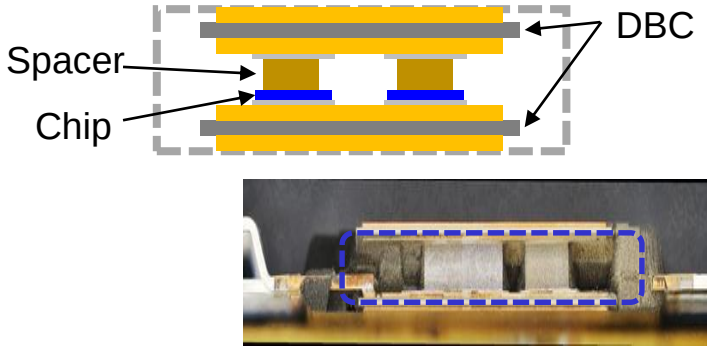
Introduction of Our Core Power Module Package

■ Applications

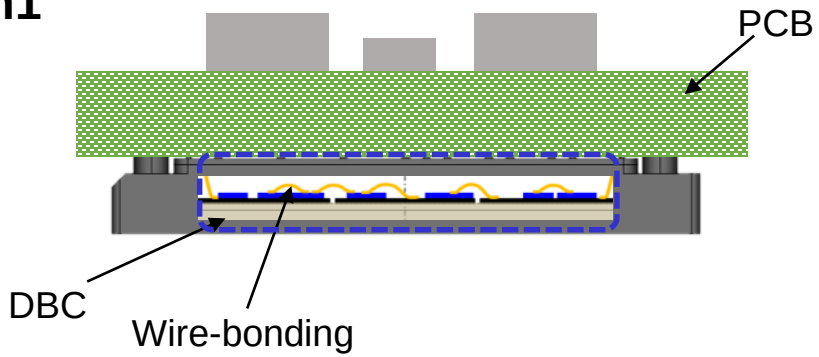
Versatile and scalable integration with core power modules

Conventional

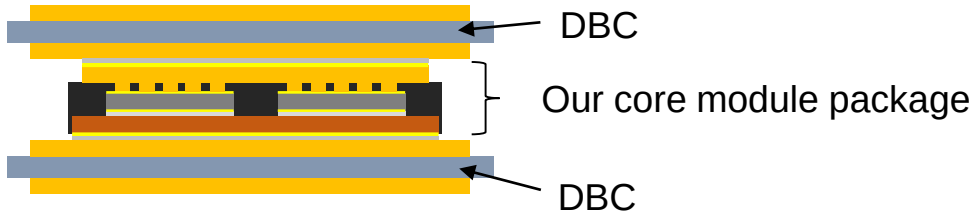
2in1



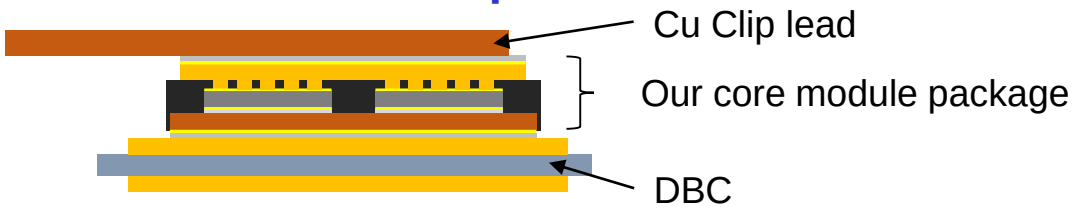
6in1



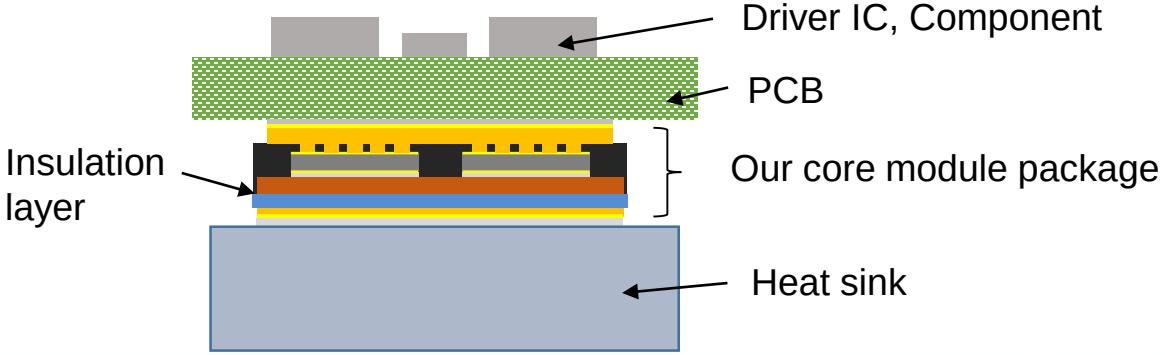
i. Connection with DBC



ii. Connection with Cu Clip lead



iii. Connection with PCB



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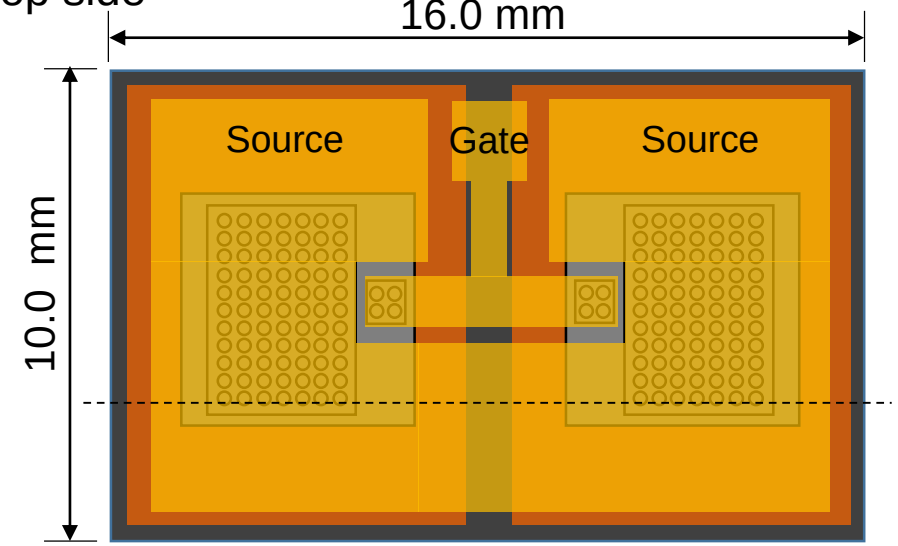
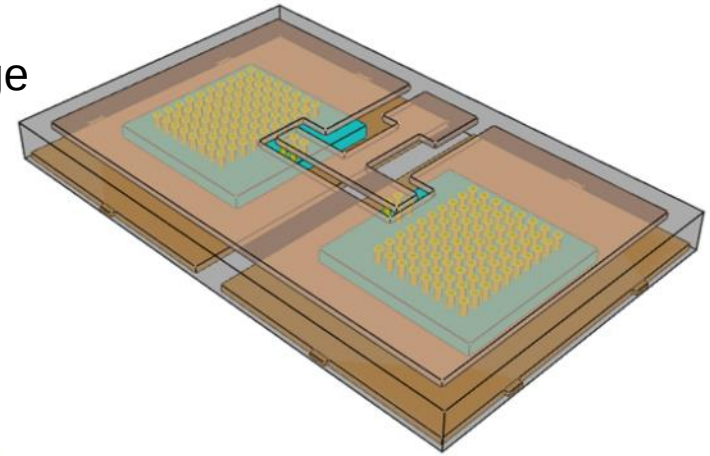
Trial production and evaluations for a Prototype

■ Prototype package structure

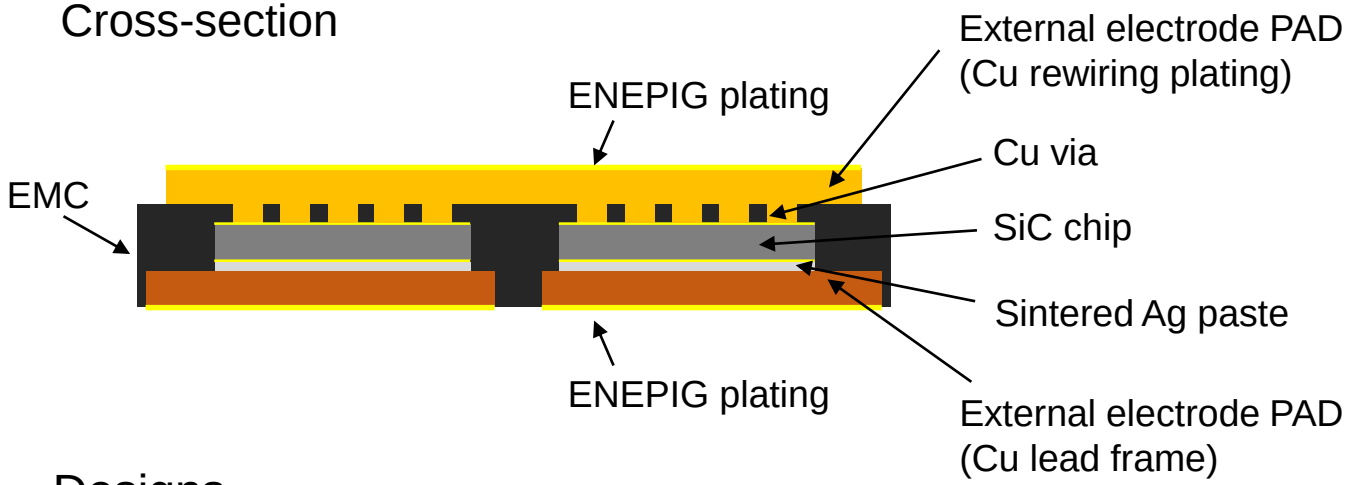
Top side



3D image



Cross-section

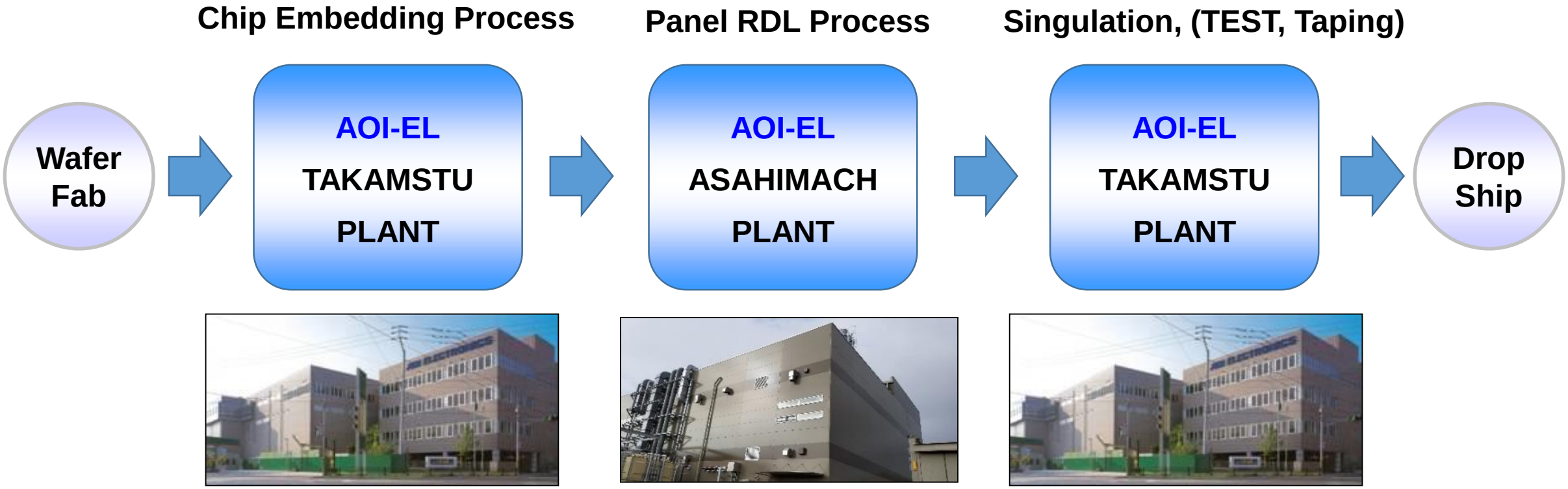


Designs

Item	Size (mm)	Thickness (mm)
Cu lead frame	-	0.20
SiC chip ×2	5.0×5.0	0.10
Sintered Ag paste	-	0.05
Cu via (on SiC chip)	Φ0.10	0.05
Cu rewiring plating	-	0.10 (or 0.20)

Trial production and evaluations for a Prototype

■ Prototype manufacturing flow and location

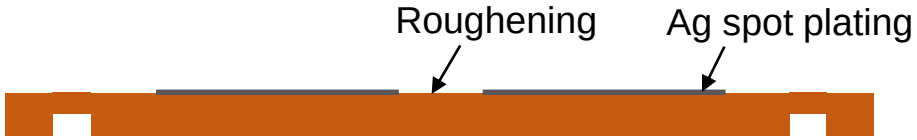


We can perform one-stop production in-house, from panel substrates to chip embedding process, panel RDL process and package assembly.

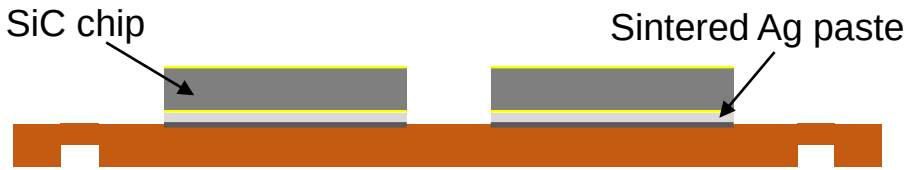
Trial production and evaluations for a Prototype

■ Prototype process flow (1)

1. Cu Lead frame (Already etched)



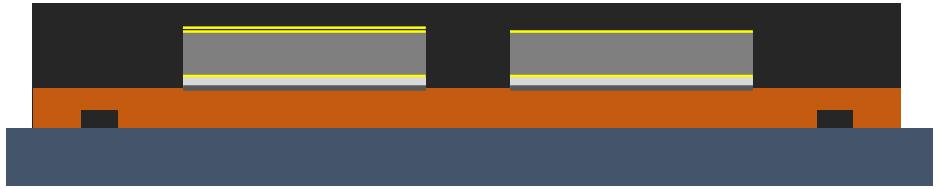
2. Paste Printing and Power chips Bonding



3. Cu Lead frame on Temporary Carrier

4. Molding (EMC)

5. EMC Grinding



6. Laser Via Drill (UV Laser)

Our Experiences
Cu Via min size : Φ25 μm (Bottom)

Trial production and evaluations for a Prototype

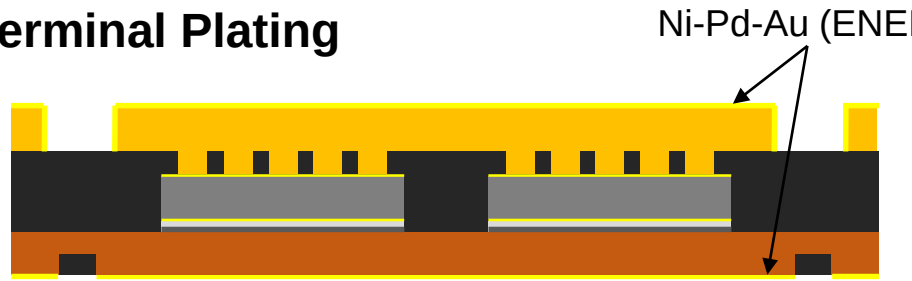
■ Prototype process flow (2)

7. Seed Plating

8. Cu Plating for Via and Rewiring

9. Temporary Carrier Debonding

10. Terminal Plating



11. Singulation/Finished

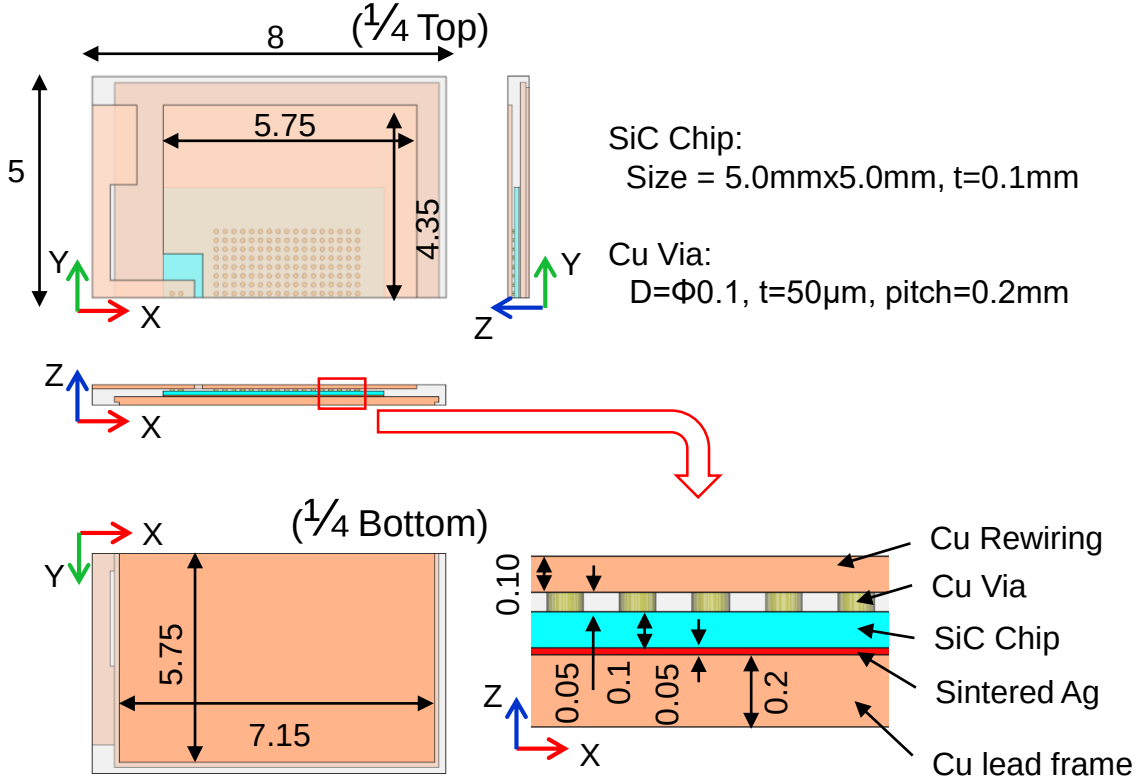
Our usual inspection or test

- Pattern inspection for each process
- Open/short test for checking internal connection
- Optional function test

Trial production and evaluations for a Prototype

■ Simulation analysis ; Thermal stress

Simulation model ; ¼ structure



Analysis software : ANSYS
Temperature condition : 175℃→25℃

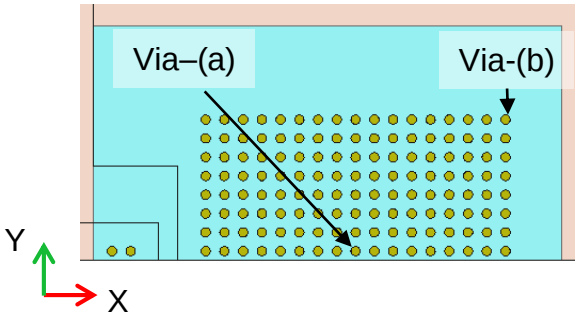
Simulation material properties

Item	Material	Young's modulus [MPa]		CTE [ppm/℃]		Tg [℃]
		@25℃	@260℃	α1	α2	
Lead frame Via, Rewiring	Cu	131000	—	17.0	—	—
Paste	Sintered Ag	22000	—	19.7	—	—
Chip	SiC	476000(X), 476000(Y), 526000(Z), 199000(XY), 159000(YZ), 159000(XZ)		4.4	—	—
EMC	Epoxy Resin (Prototyping)	21000	—	9.0	25.0	190
	Prepreg (for comparison)	24000	—	12(X,Y) 40(Z)	14(X,Y) 180(Z)	190

Trial production and evaluations for a Prototype

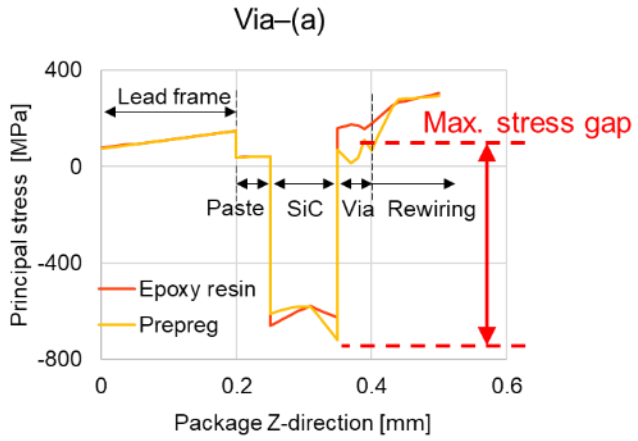
■ Simulation analysis ; Thermal stress

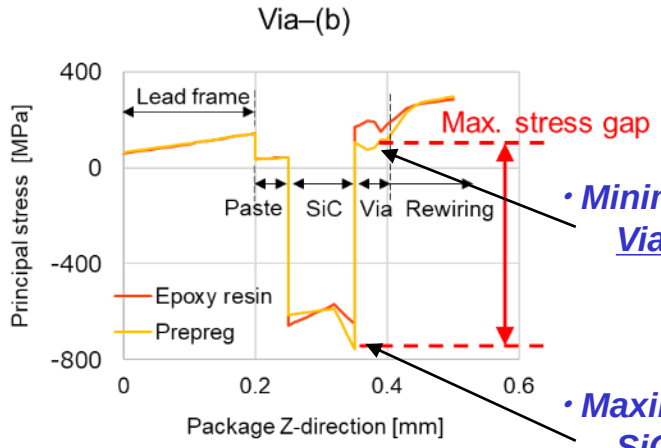
Thermal stress analysis point



(a) Chip center via; (b) Chip corner via

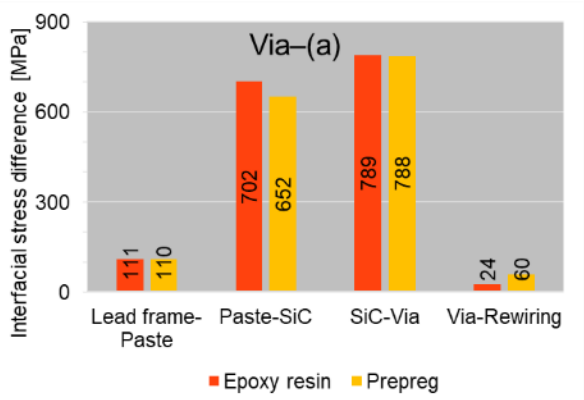
Principal stress and Interfacial Stress Gap value

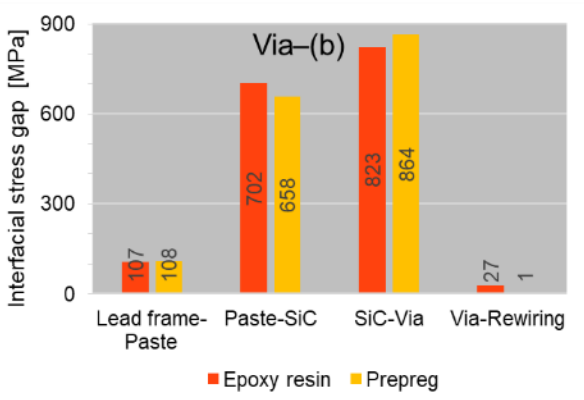




・Minimum principal stress : Via (tensile stress)

・Maximum principal stress : SiC chip (compressive stress)



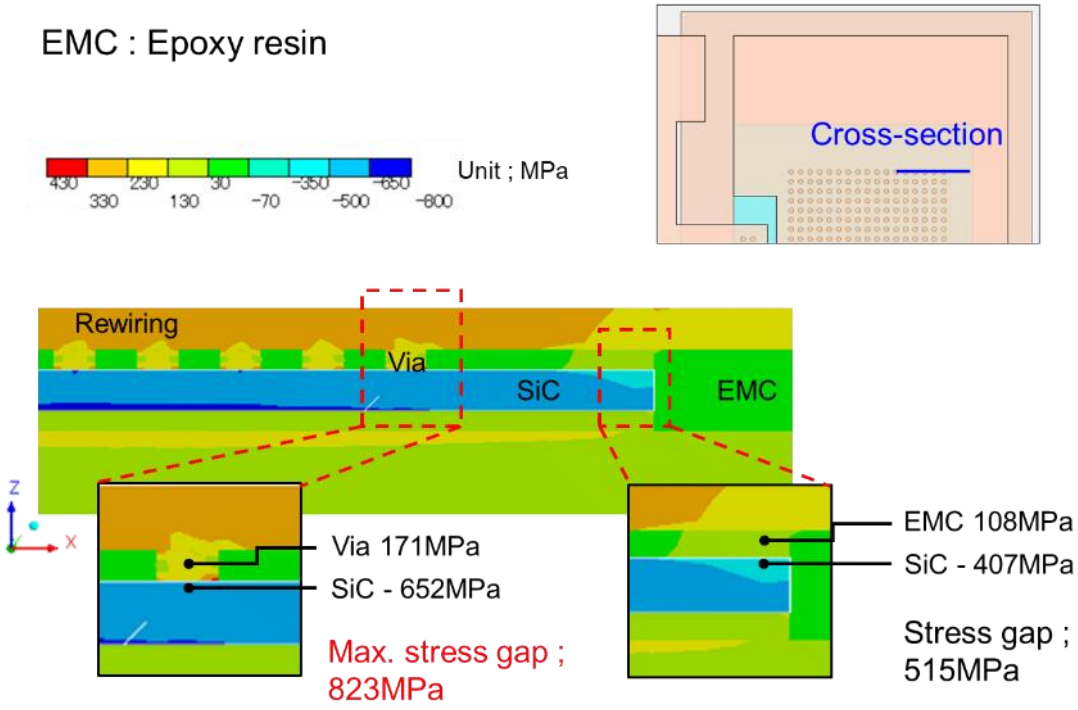


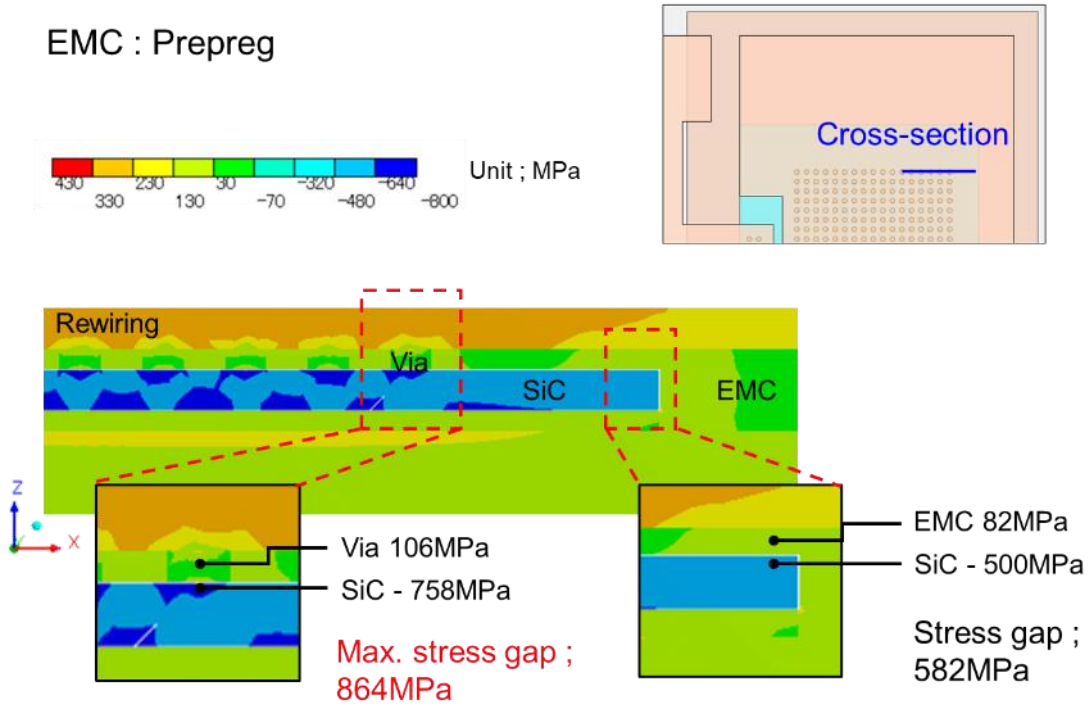
The maximum gap values of principal and interface stresses are at the junction of the SiC chip and Via.
The interfacial stress gap is larger at the SiC chip corner via-(b) than at the SiC chip center via-(a).

Trial production and evaluations for a Prototype

■ Simulation analysis ; Thermal stress

The stress distribution on SiC chip corner cross section



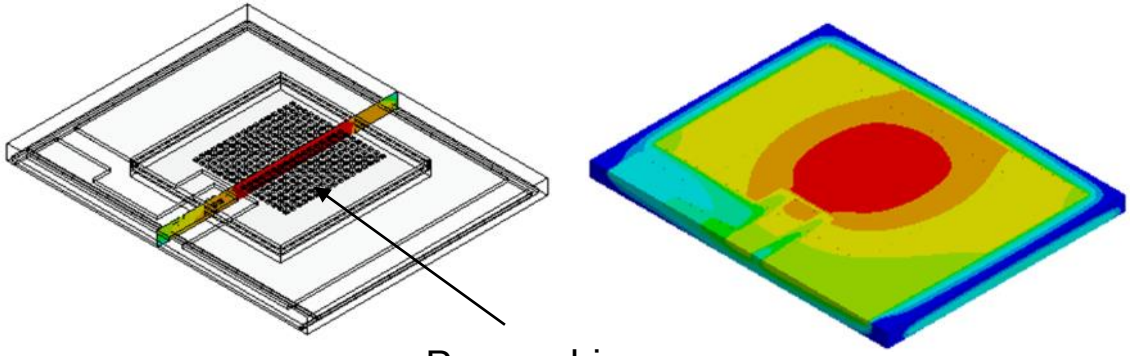


The maximum stress gap is smaller for epoxy resin than for prepreg at the junction of SiC chip and via (about 5%). The maximum stress difference is smaller for epoxy resin than for prepreg at the junction of SiC chip and EMC (about 10%).

Trial production and evaluations for a Prototype

■ Simulation analysis ; Thermal resistance

Simulation model ; ½ structure



Analysis conditions

Using ANSYS

Item	Boundary condition
Atmosphere temperature	25℃
Heat transfer coefficient (Other)	10 W/(m²℃) Assuming natural air cooling
Chip Power	Total 1.0W 0.5W/power chip

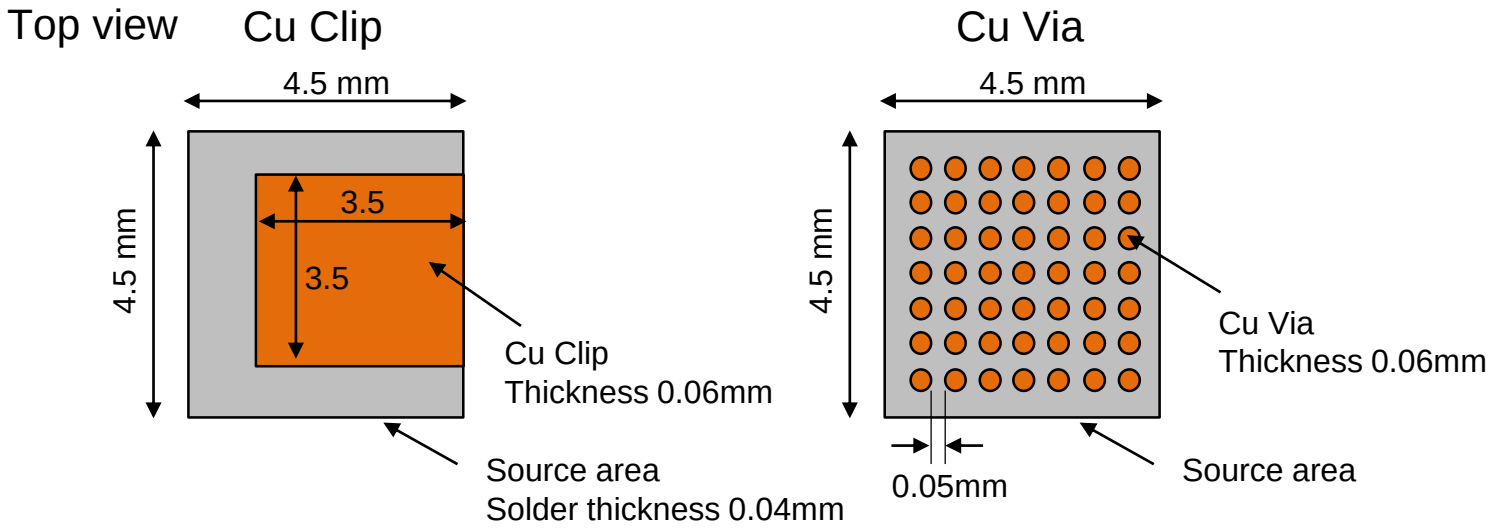
Material properties

Item	Thermal conductivity [W/(m.℃)]	Electric resistivity [Ω・m]
SiC chip	270	0.00015, 0.17(chip surface 10μm)
Sintered Ag paste	250	0.04×10^{-6}
Electrode PAD(Cu)	360	0.023×10^{-6}
Cu via and rewiring	360	0.017×10^{-6}
EMC	1.0	-

Thermal resistance is very low, allowing uniform heat dissipation from both top and bottom sides.

Trial production and evaluations for a Prototype

■ Wiring Resistance calculation



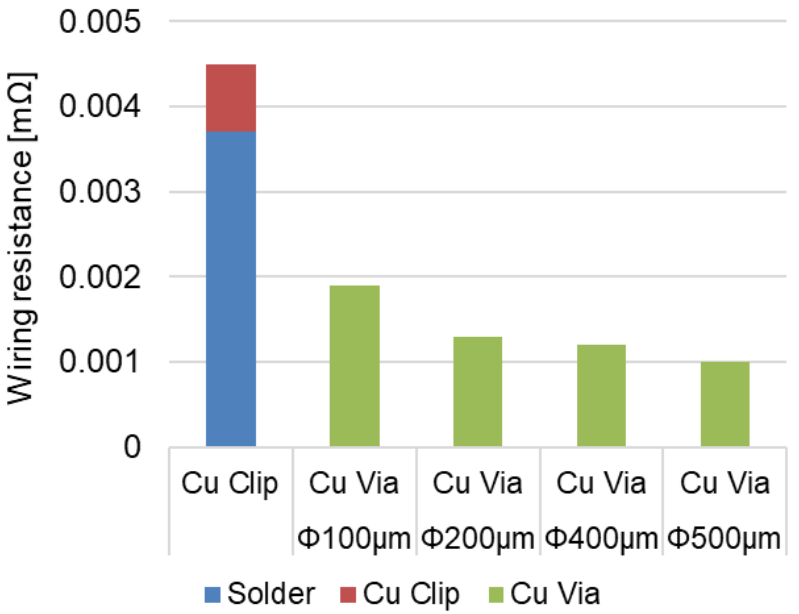
■Cu Clip

	No.	Wiring thickness	Unit	Cross-sectional area	Unit	Wiring resistance	Unit	Wiring contact ratio (Clip area/Source area)
Solder	1	0.000400	m	1.20E-05	m^2	0.0037	mΩ	60%
Cu Clip	2	0.000600	m	1.20E-05	m^2	0.0008	mΩ	60%
					Total	0.0045	mΩ	

■Cu Via

	No.	Wiring thickness	Unit	Cross-sectional area	Unit	Wiring resistance	Unit	Wiring contact ratio (Via area/Source area)
Cu viaΦ100	1	0.000600	m	5.20E-06	m^2	0.0019	mΩ	25%
Cu viaΦ200	2	0.000600	m	7.80E-06	m^2	0.0013	mΩ	38%
Cu viaΦ400	3	0.000600	m	8.20E-06	m^2	0.0012	mΩ	41%
Cu viaΦ500	4	0.000600	m	1.00E-05	m^2	0.0010	mΩ	50%

Cu Clip vs Cu Via wiring resistance



Wiring resistance is lower for Cu via than for Cu clip.

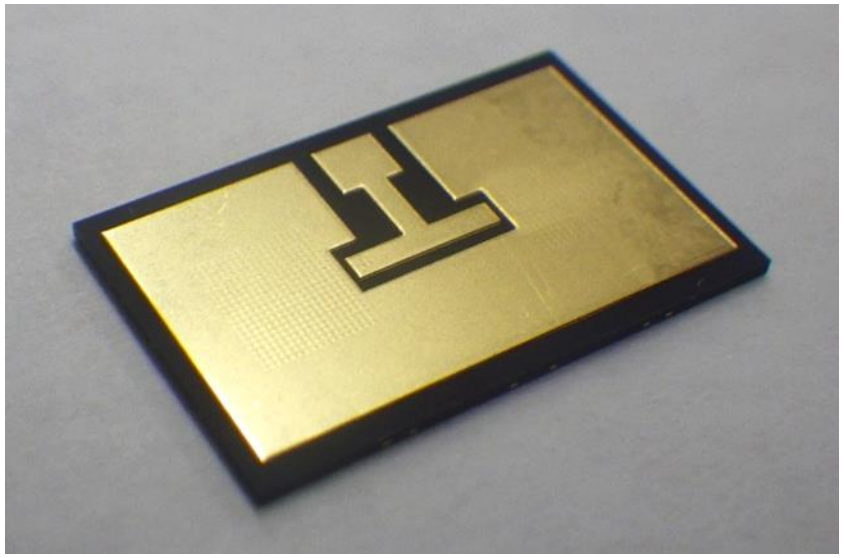
Cu via have sufficiently low wiring resistance even at Φ0.10μm.

Trial production and evaluations for a Prototype

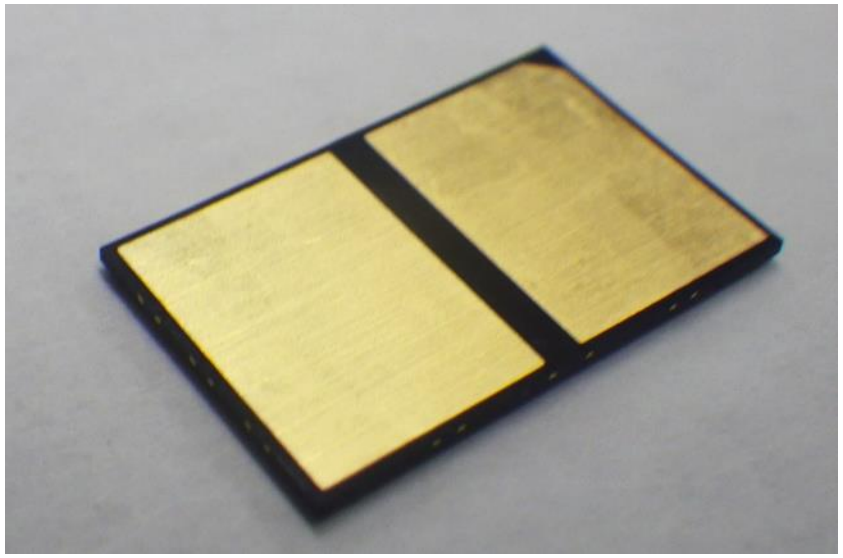
■ Results of prototype

External view

Top



Bottom



Side

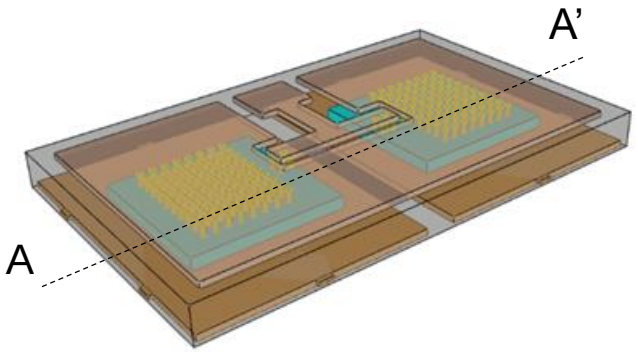
Top

Bottom

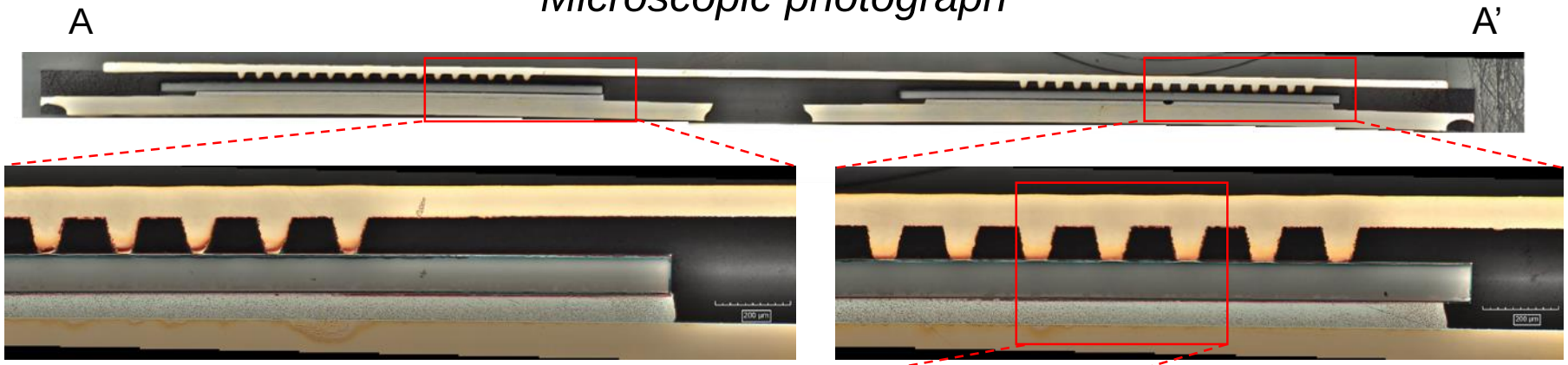
Trial production and evaluations for a Prototype

■ Results of prototype

Actual Cross-section



Microscopic photograph



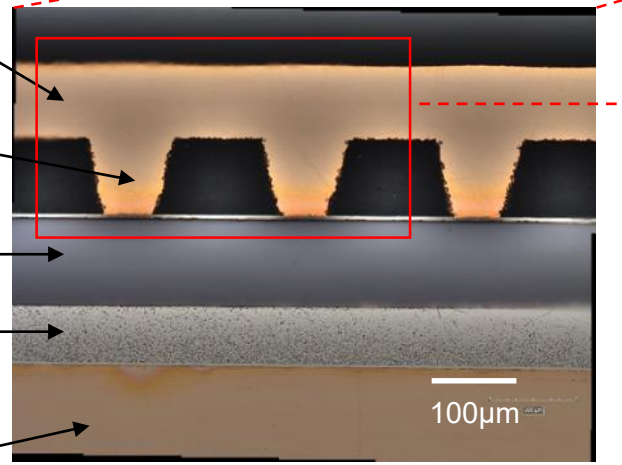
External electrode PAD
(Cu rewiring plating)

Cu via

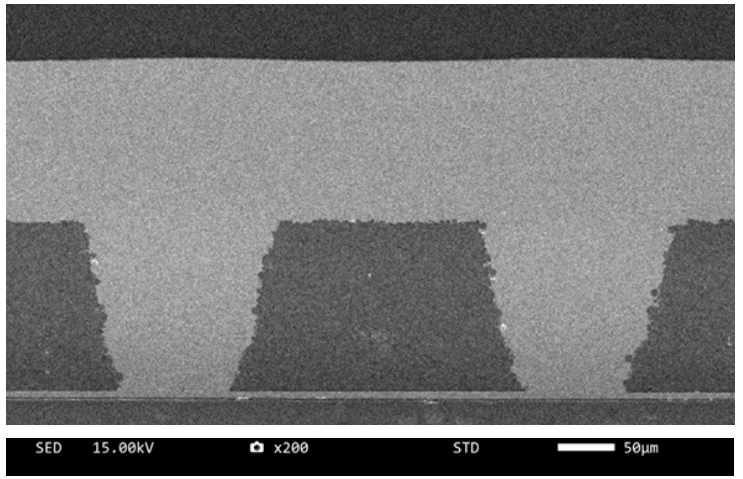
SiC chip

Sintered Ag paste

External electrode PAD
(Cu lead frame)



SEM



Good connection!

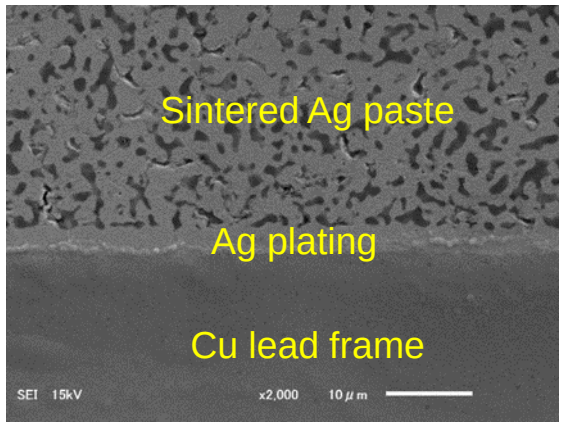
Trial production and evaluations for a Prototype

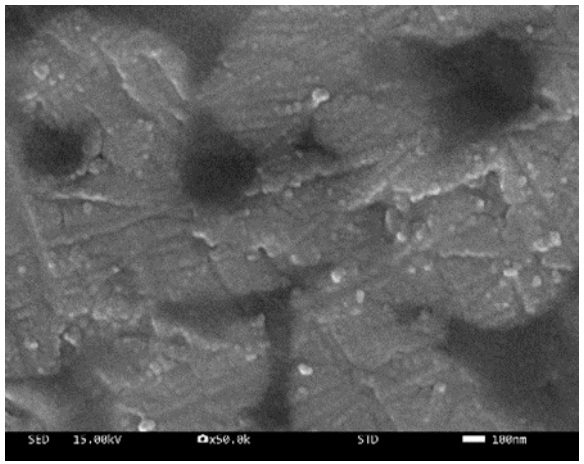
■ Results of prototype

Actual Cross-section

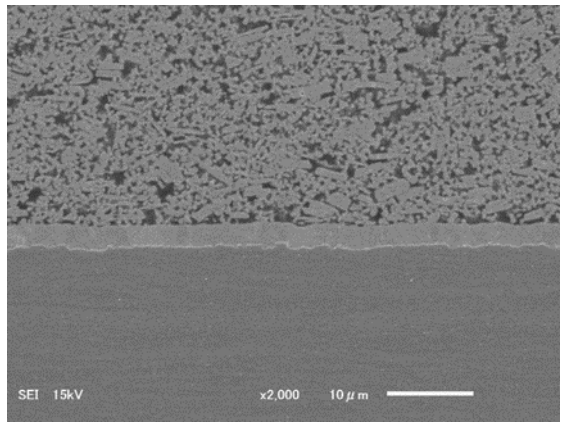
Sintered Ag Paste Bondability Confirmation

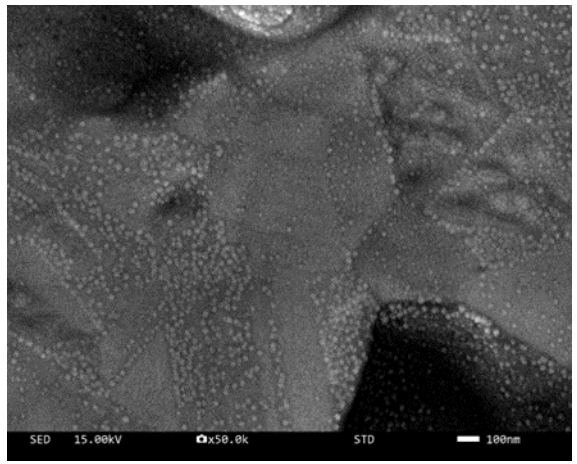
Pressureless





Pressure





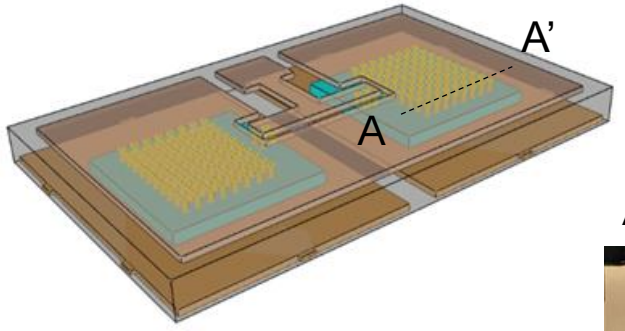
In both cases, good necking was observed.
There seems to be a difference in densification between pressureless and pressure.

Trial production and evaluations for a Prototype

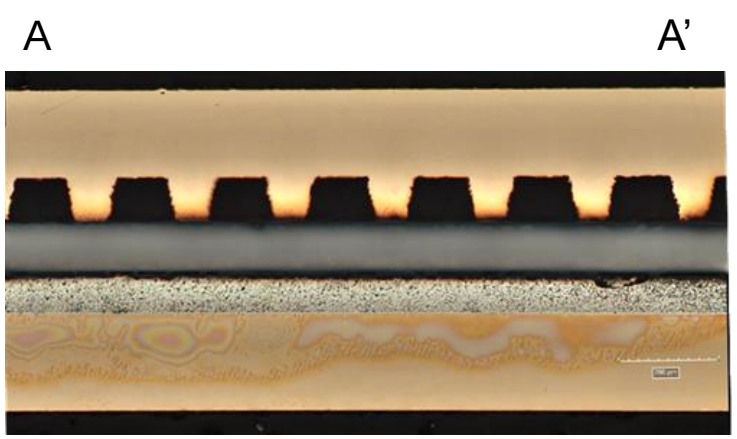
■ Results of prototype

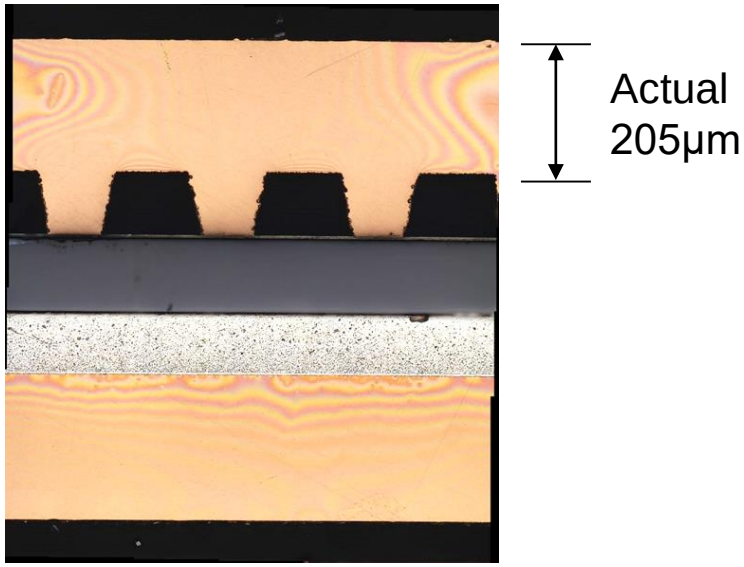
Actual Cross-section

Verification results of the thicker Cu rewiring plating process



Microscopic photograph





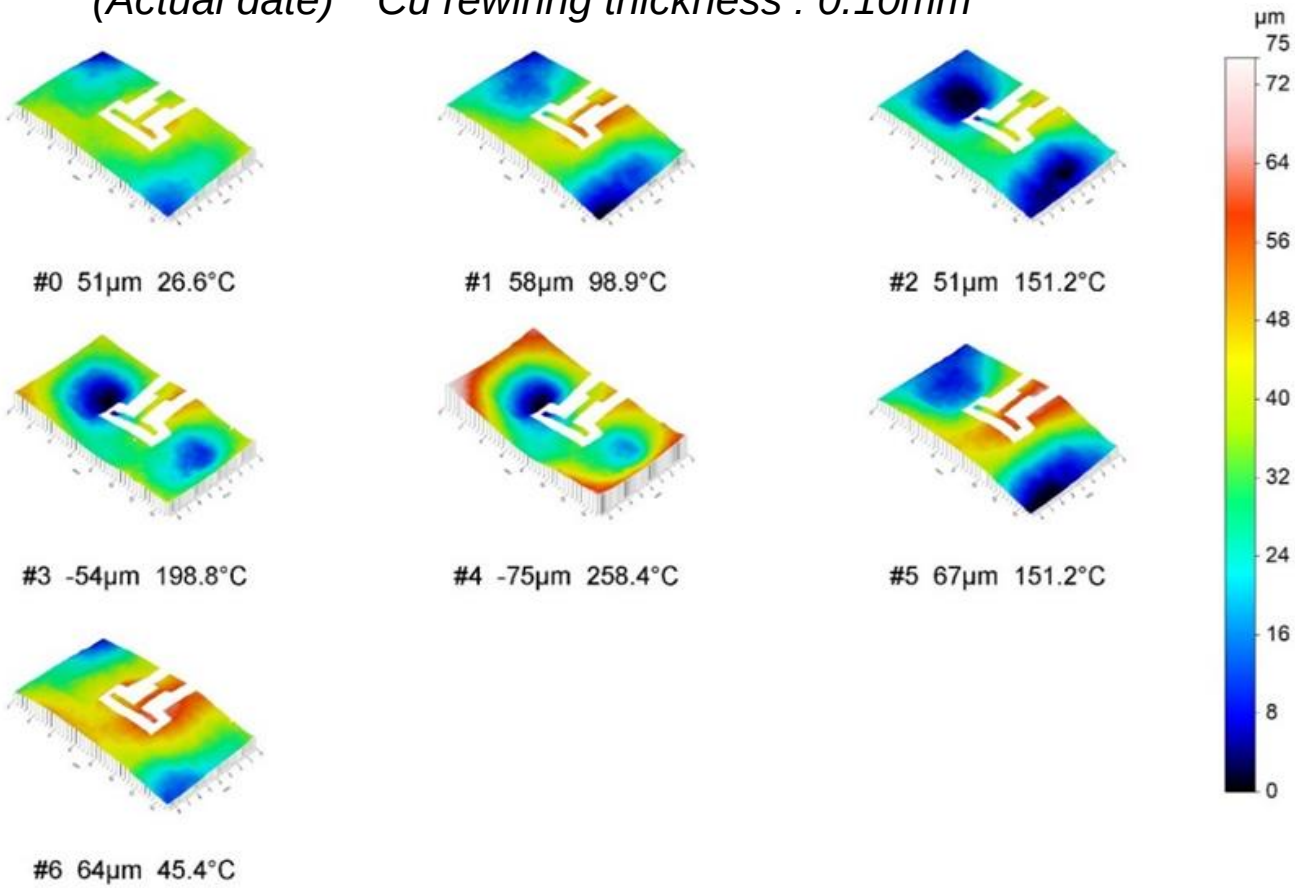
Good thick Cu rewire plating without voids was observed.

Trial production and evaluations for a Prototype

■ Results of prototype

Package warpage behavior in the reflow temperature Range using the projection moiré method

(Actual date) Cu rewiring thickness : 0.10mm



Warpage improvement

Relative warpage to Cu rewiring thickness 0.10mmt (prototype)

- *Cu rewiring 0.03mm (Standard) : 2.5 times*
- *Cu rewiring 0.20mm (Optional) : 0.25 times*

※*Simulation data*

Toward further low warpage

Double-Side Direct Cu Plating Connection to power chips
(CTE Mismatch Minimization)

Convex warpage on the Top side at room temperature and concave warpage at reflow temperature.

Trial production and evaluations for a Prototype

■ Reliability Test

Test Items	Test Condition	Duration	Judgment	Status
Precondition	1. 85℃, 85%RH, 168hr ⇒ >260℃, 30sec. 3X (JEDEC J-STD-020 MSL Level1)	-	-	Ongoing
	2. 85℃, 60%RH, 168hr ⇒ >260℃, 30sec. 3X (JEDEC J-STD-020 MSL Level2)	-	-	Ongoing
Unbiased HAST	Precondition (MSL1 or 2) ⇒ 121℃, 100%RH, 2atm	100hr	SEM Cross-section	Ongoing
HTS	Precondition(MSL1 or 2) ⇒ 150℃	1,000hr	SEM Cross-section	Ongoing
TC	Precondition(MSL1 or 2) ⇒ -65℃～150℃	500cycle	SEM Cross-section	Ongoing

There is no initial failure at Unbiased HAST 48hr, TC 50cycle.

Summary

- ✓ We demonstrated a core power module package in a 300 mm square panel-level process with chip-embedded double-sided heat dissipation and all Cu-plated internal connections (no wire-bonding).
- ✓ Prototype results confirmed that Cu via plating and sintered Ag paste are good connections to the power chips.
- ✓ Simulation results show very low thermal resistance and uniform heat dissipation from both package top and bottom sides.
- ✓ The simplicity and scalability of the core power module package will enable the development of many future wide-bandgap power devices.

Thank you for your attention.

Our presentation will also be in Poster Session.
Please join and discuss!