Patterning Fine Pitch L/S on Photosensitive PBO Using Laser Direct Imaging for High-Density Interconnect Applications

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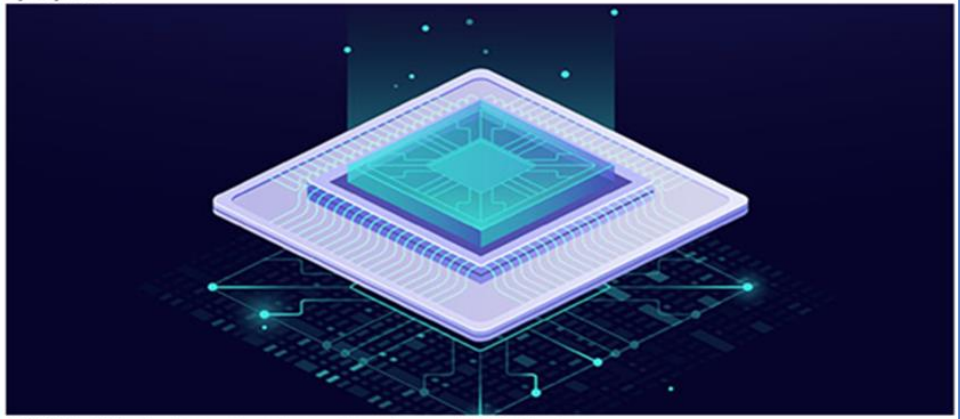
Recent News

Next-Generation Microelectronics Manufacturing Aims to Sustain R&D Ecosystem

DARPA names eleven teams to kick off groundbreaking U.S. chips-of-the-future effort

OUTREACH@DARPA.MIL
7/20/2023



NGMM will fuel microsystem innovations beyond 2D limitations

With a focus on the future wave of microsystems innovation, DARPA has selected 11 organizations to begin work on the Next-Generation Microelectronics Manufacturing (NGMM) program. The Phase 0 effort will establish foundational research to inform next steps toward creating a domestic center for fabricating 3D heterogeneously integrated (3DHI) microsystems.

Selected teams are Applied Materials, Inc., Arizona State University, BRIDG, HRL Laboratories, Intel Federal, North Carolina State University, Northrop Grumman Space Systems, Northrop Grumman Mission Systems, PseudolithIC, Raytheon Technologies, and Teledyne Scientific & Imaging.

ASU Arizona State University — ASU News

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September 20, 2023

1. Northeast Microelectronics Coalition (NEMC) Hub

   Awardee (Hub Lead): The Massachusetts Technology Collaborative (MassTech)
   Hub Lead State: Massachusetts
   FY23 Award: $19.7 M
   90 Hub Members

2. Silicon Crossroads Microelectronics Commons (SCMC) Hub

   Awardee: The Applied Research Institute (ARI)
   Hub Lead State: Indiana
   FY23 Award: $32.9 M
   130 Hub Members

3. California Defense Ready Electronics and Microdevices Superhub (California DREAMS) Hub

   Awardee: The University of Southern California (USC)
   Hub Lead State: California
   FY23 Award: $26.9 M
   16 Hub members

4. Commercial Leap Ahead for Wide Bandgap Semiconductors (CLAWS) Hub

   Awardee: North Carolina State University (NCSU)
   Hub Lead State: North Carolina
   FY23 Award: $39.4 M
   7 Hub members

5. Southwest Advanced Prototyping (SWAP) Hub

   Awardee: Arizona Board of Regents on behalf of Arizona State University
   Hub Lead State: Arizona
   FY23 Award: $39.8 M
   27 Hub members

6. Midwest Microelectronics Consortium (MMEC) Hub

   Awardee: MMEC
   Hub Lead State: Ohio
   FY23 Award: $24.3 M
   65 Hub members

7. Northeast Regional Defense Technology Hub (NORDTECH)

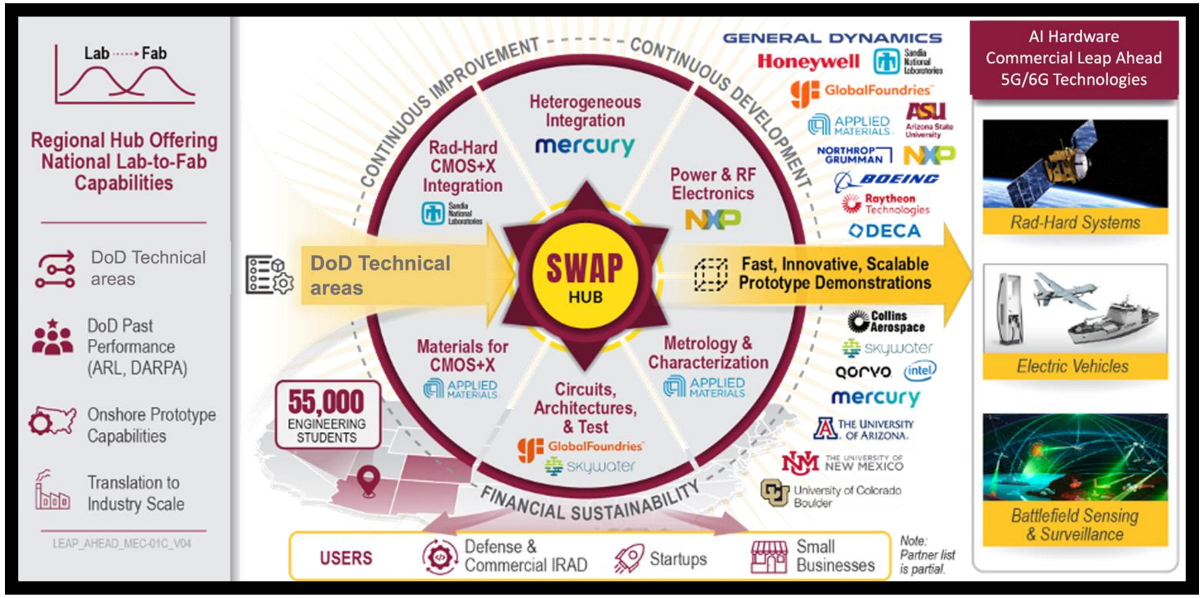
   Awardee : The Research Foundation for the State University of New York (SUNY)
   Hub Lead State: New York
   FY23 Award: $40.0 M
   51 Hub members

8. California-Pacific-Northwest AI Hardware Hub (Northwest-AI Hub)

   Awardee: The Board of Trustees of the Leland Stanford Junior University
   Hub Lead State: California
   FY23 Award: $15.3 M
   44 Hub members

Southwest Advanced Prototyping (SWAP) Hub

Semiconductor | Aerospace & Defense | Educational Institution | National Laboratories



Heterogeneous Integration

- High-density integration of chiplets, discrete devices, and power devices via chip-first 300 mm FOWLP
- Detailed electrical-thermal-mechanical simulation of packages
- Addressing size, weight, and power via packaging

Radiation-hardened CMOS+X Integration

- Proven rad-hard CMOS process at Sandia
- Flexibility to interrupt the BEOL process and integrate new functional materials (e.g., CMOS+X)
- State-of-the-art radiation and other extreme testing environments

Materials for CMOS+X

- $270M AMAT-ASU partnership makes dozens of 300 mm advanced deposition chambers available for new materials
- Emerging memory materials and device stacks
- 2D layers scaled to full-wafer processing

Circuits, Architecture, and Test

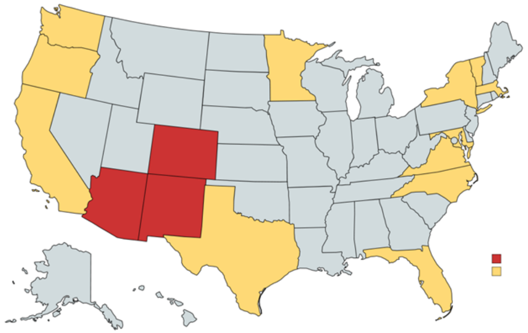
- State-of-the-art EDA and IP for co-design, including with new materials/layers
- RF IP blocks
- Design for heterogeneous integration and packaging
- Rad-hard and trusted and assured by design

Metrology & Characterization

- Electronic, morphological, chemical, thermal analysis of materials, devices, chips, and packages
- Up to 300 mm inline wafer monitoring and QC
- Offline advanced electron microscopy, X-ray analysis

Power & RF Electronics

- Wide-bandgap materials, devices, and circuits
- III-V R&D fab at Sandia; GaN fab at NXP; GaO, AIN, diamond MOCVD at ASU
- Very high frequency test
- Power converter design, assembly, and test



Southwest Region

National Members

Members

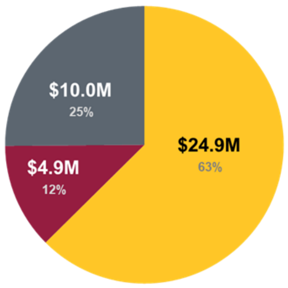
Hub Lead:
Arizona State University
Tempe, AZ / University (Non-Traditional)

Number of Hub Members:
70

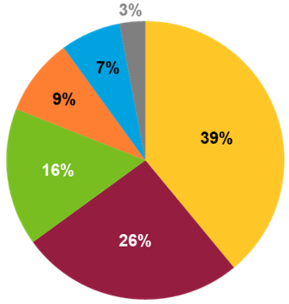
Total Commons Funding:
$39.8m year 1 / $99m 5 year total

Total Estimated Hub Value:
$500M+

Financial Breakdown

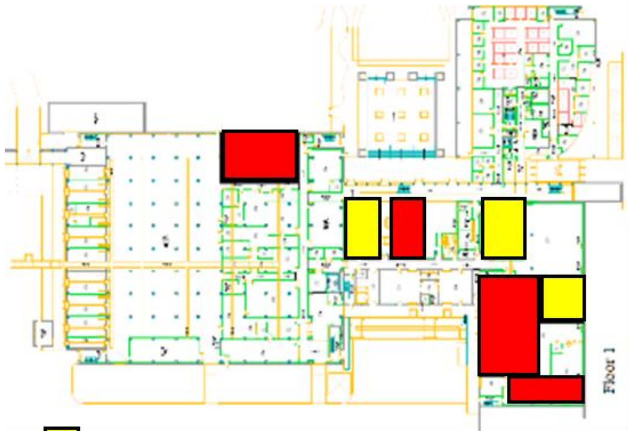


Membership by Category



Packaging and Assembly Capabilities - MTW

- ASU Macro Technology Works (MTW) Facility
  - 250k sq ft capacity; 43.5k sq ft cleanroom
  - Substantial H6 capacity
  - R&D, pilot, and production capability
- Lab renovations
  - Add 1800 sq ft cleanrooms (class 10,000) for Advanced Electronics and Photonics (AEP) core
  - 2600 sq ft of faculty labs (including Packaging)
- Home to world-leading equipment vendors AMAT, EVG



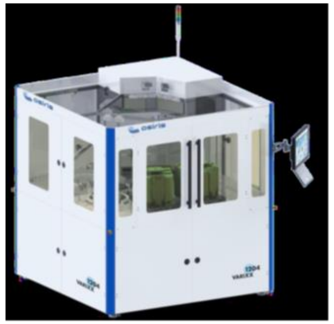
New Packaging Research Spaces

Other AEP Core lab space

Packaging and Assembly Capabilities

- New 300mm FOWLP and 3D processing line will enable prototyping and productivity enhancements
- Evolving Capabilities
  - 4+ RDL layers; 2um L/S
  - <20um die bond pad pitch
  - <75um die spacing
  - C4 solder bumping
  - Cu pillar u-bumps
  - Flip-chip TCB & Direct bonding
  - Reflow assembly
  - Capillary underfill
  - Reliability Characterization

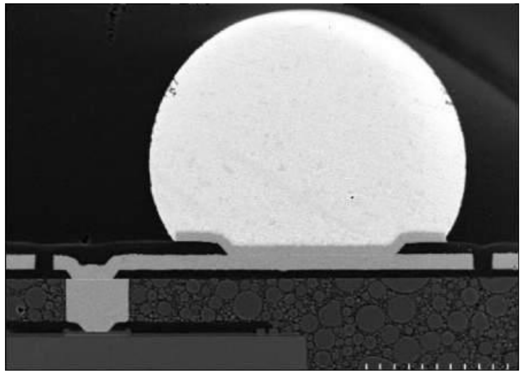
- Heidelberg MLA 300
  - Training in progress



- Osiris 1204 Coat/Develop
  - Arriving in June 2023
  - Additional Wet Etch and Solvent Etch arriving early 2024

- AMAT Centura Etch
  - Facilitization in Process

- Yamada WCM-300 Molding System
  - Acquisition in Progress



- Additional Equipment being specified:
  - Laminators
  - Grinding
  - Dicing
  - AOI
  - Chip Attach
  - Ball Drop

Outline

Title: Patterning Fine Pitch L/S on Photosensitive PBO Using Laser Direct Imaging for High-Density Interconnect Applications

- Background – PBO, photosensitive polymer, laser direct imaging (LDI)
- Experiments – Design and fabrication of fine pitch L/S pattern
- Results – Metrology and analysis
- Conclusion

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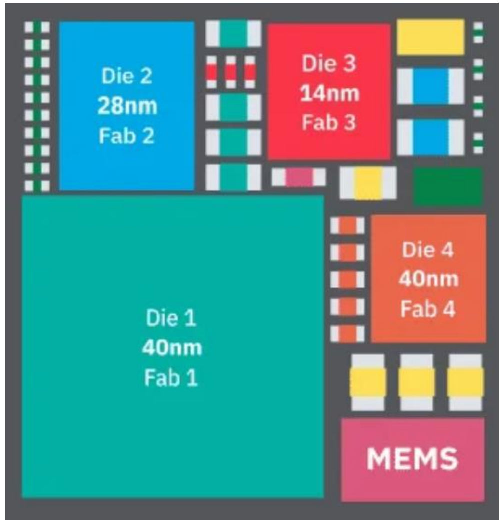
Motivation

- Prevalence of chiplets and heterogeneous integration for higher performance and other demands.
- Redistribution layers (RDL) with high density interconnect allow high speed signaling between the chiplets.



Heterogeneous integration of chiplets

Source: ASE

Dielectric material between interconnects

Non-organic dielectric

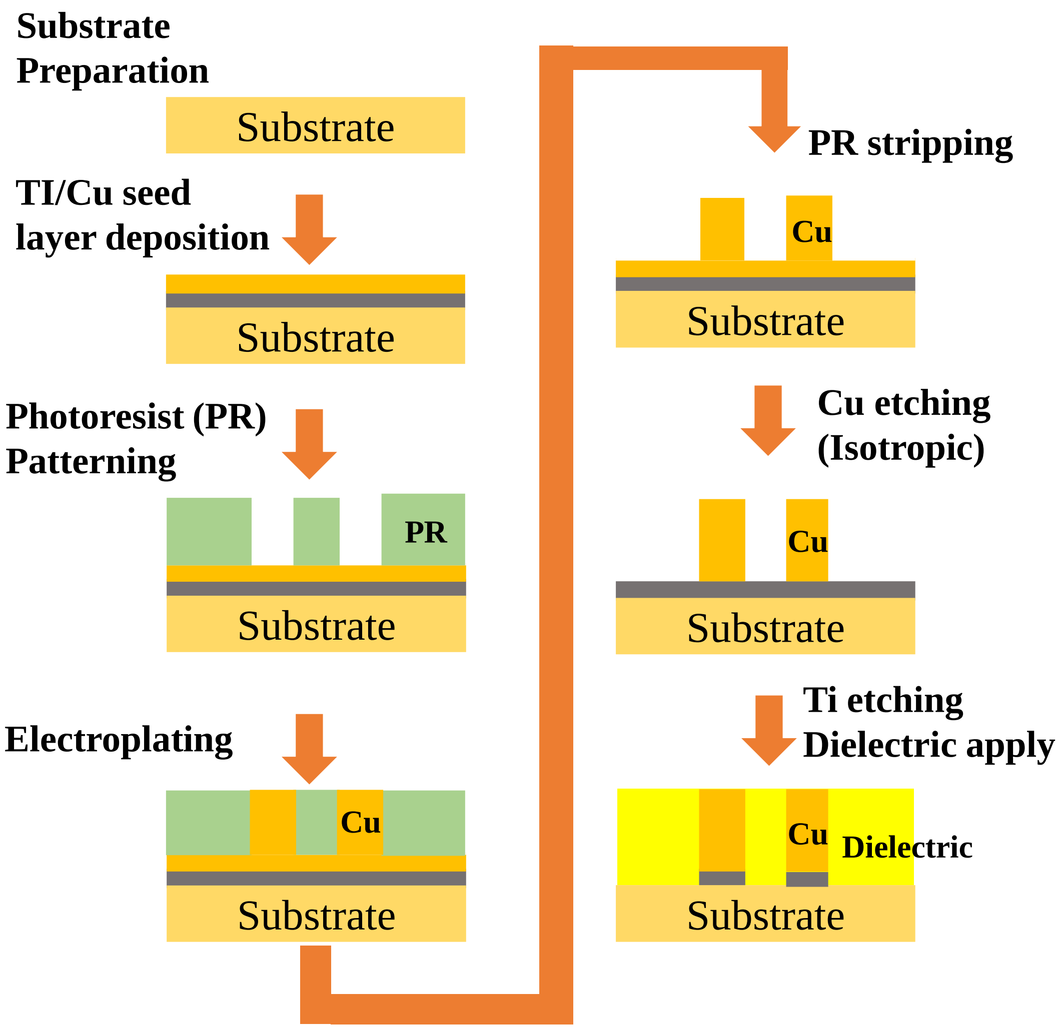
- SiN and SiO_2
  - SiN: excellent chemical resistance and thermal stability
  - SiO2: lower dielectric constant
  - Deposition requires high-temperature process like Chemical Vapor Deposition (CVD)
- Glass
  - Strengths: low dielectric constant, loss tangent; tailorable coefficient of thermal expansion (CTE) to Si die
  - Drawback: processing difficulties and poor thermal conductivity

Dielectric material between interconnects

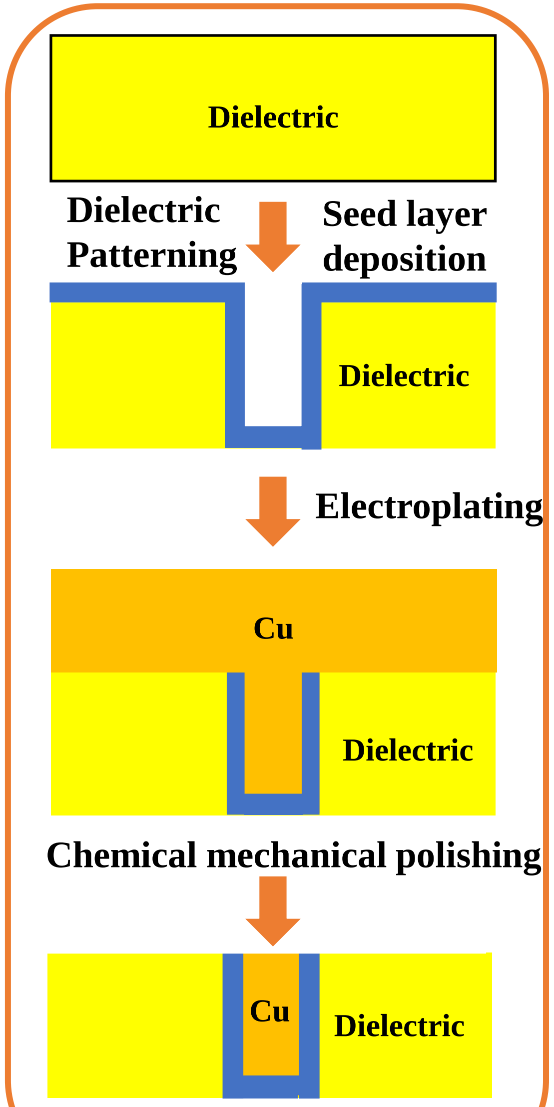
Organic dielectric

- Polyimide
  - Good chemical resistance, thermal and mechanical properties, and copper compatibility
  - Solvent-developed, not environmentally friendly
- Polybenzoxazoles (PBO)
  - Similar performance to polyimide, lower curing temperature
  - Can be developed in aqueous based developer (used for photoresists)

Semi-Additive Process VS Damascene Process



Semi-additive process (SAP)



Damascene process

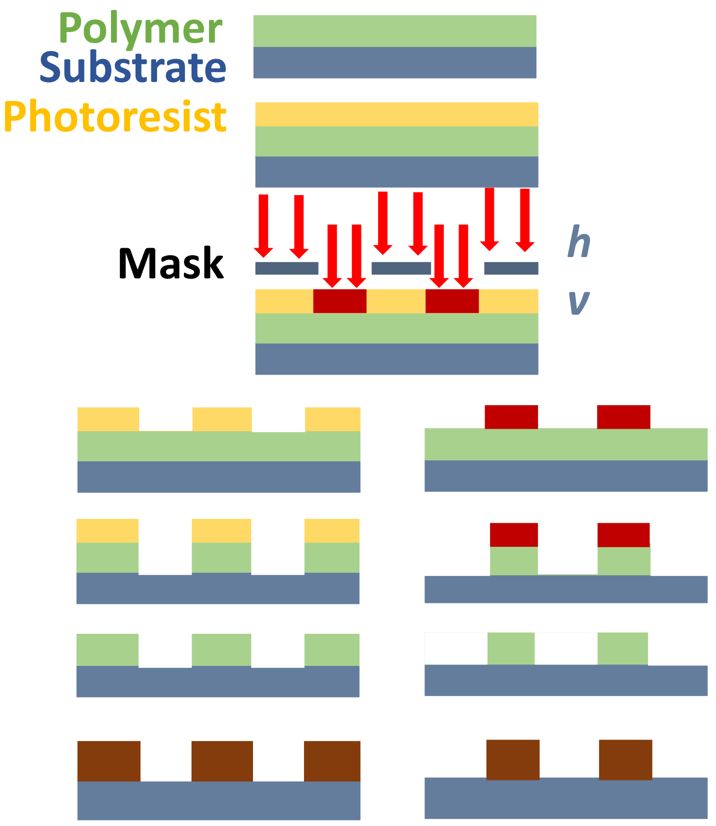
Why damascene process over SAP?

- Dielectric is deposited and patterned first.
- No Cu etching is needed.

Efficient polymer patterning is demanded.

Conventional Polymer VS Photosensitive Polymer

Conventional Polymer



Positive-tone Negative-tone

Process

Polymer Coating

⇩

Photoresist Coating

⇩

Exposure

⇩

Development

⇩

Etching

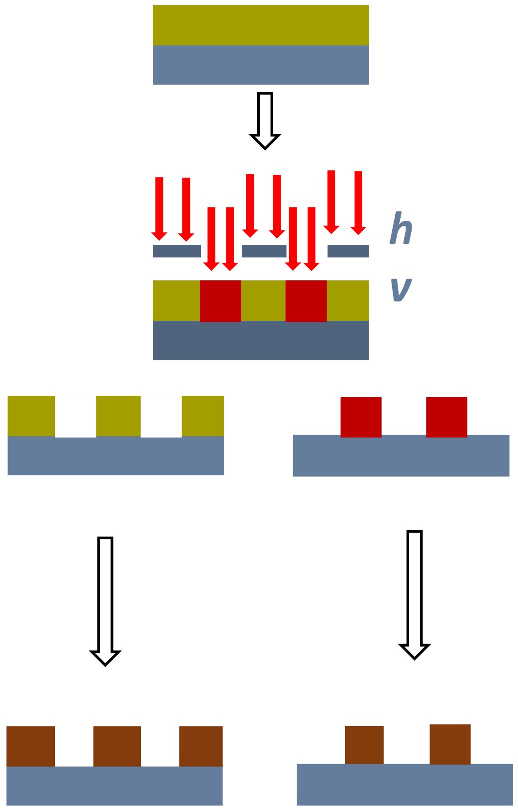
⇩

Resist Removal

⇩

Curing

Photosensitive Polymer



Positive-tone Negative-tone

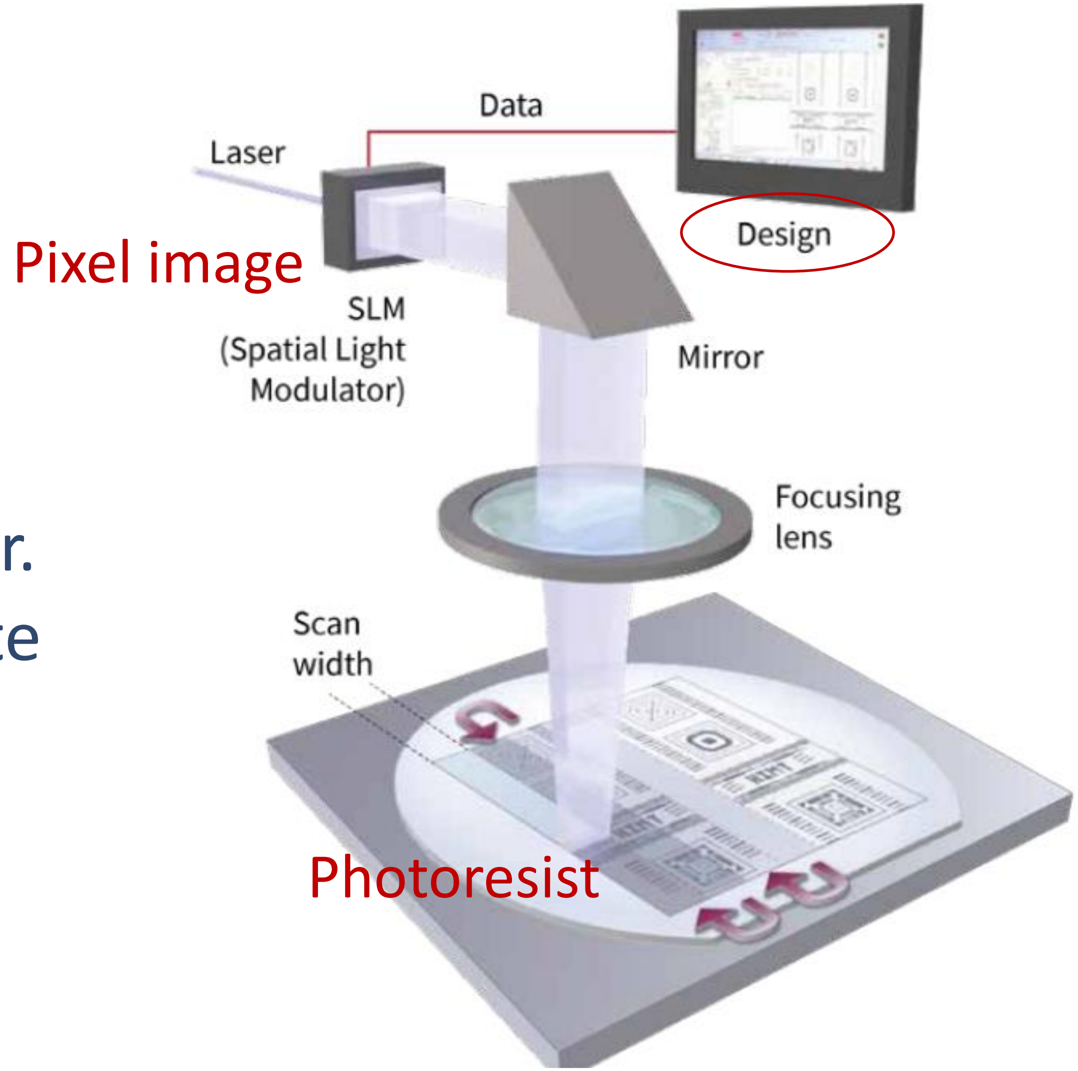
Mask Lithography

Conventional mask lithography

- Creating and changing photomasks: less flexible and more expensive for prototyping
- The limited size of reticles may require stitching of the patterns, which can result in stich lines or mismatched overlap.
- Trade off between resolution and depth of focus (DoF)

LDI (Laser Direct Imaging)

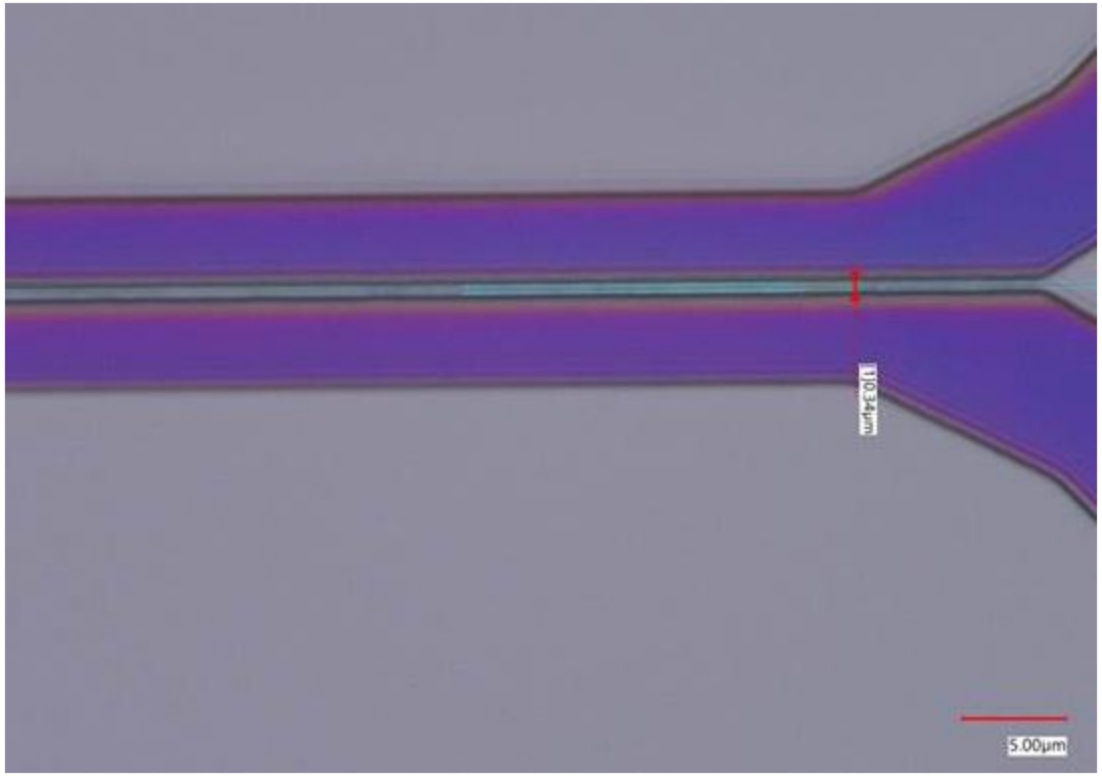
- With the elimination of photomasks, LDI allows for rapid prototyping and high flexibility.
- No reticle stitching is needed
- The DoF is improved by highly focused laser.
- Enabling adaptive patterning to compensate die shift.



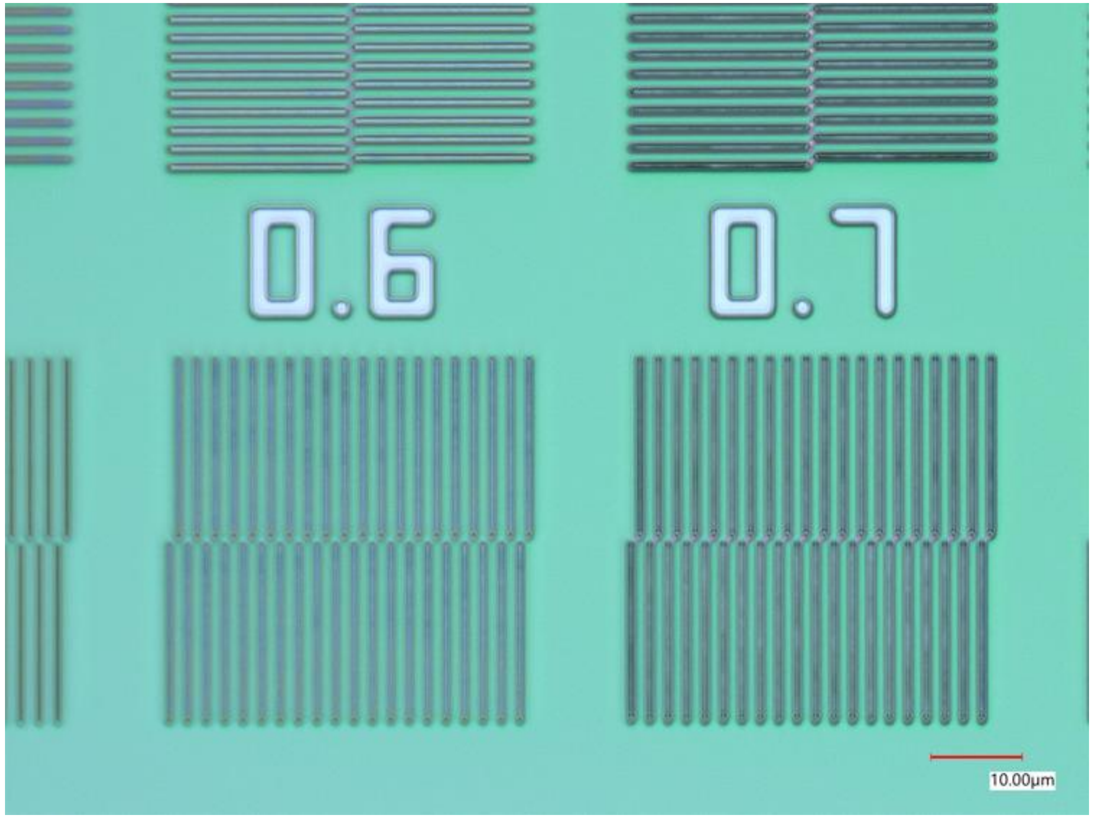
Writing strategy of MLA 150 maskless aligner

Source: Heidelberg Instruments

Fine Photoresist Pattern at MTW with MLA-300



300nm space design with photoresist AZ1505 at ~380nm thickness



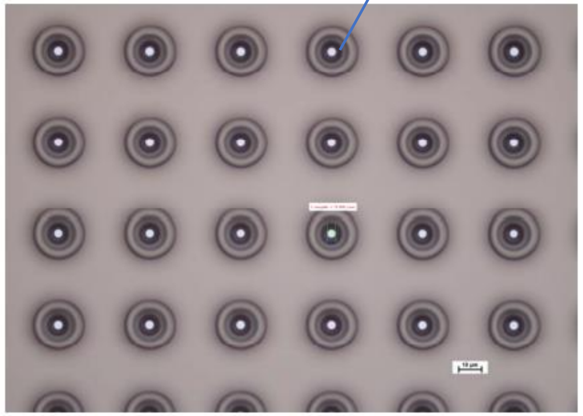
Sub-micron L/S photoresist pattern

Source: Advanced Electronics and Photonics core at MTW

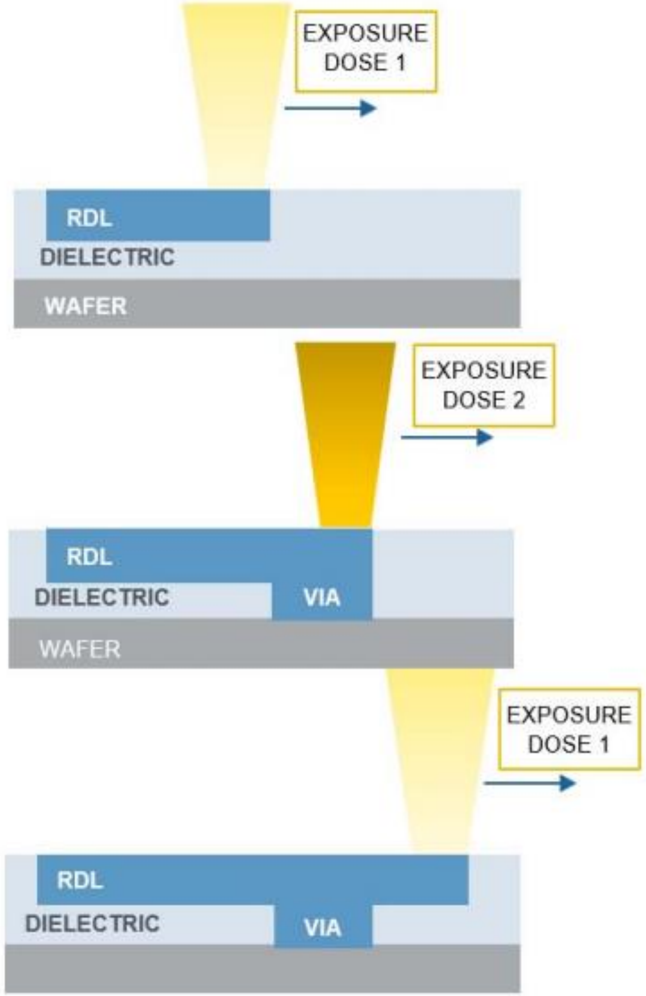
EVG's Work on Photosensitive PBO with LDI

- LDI on positive photo-imageable PBO HD8820 from HD Microsystem, with EVG's LITHOSCALE tool.
- Both RDL and deep via patterns were fabricated.
- 3.6 µm resolution was achieved.

3.6 µm inner via



HD8820 pattern with inner via = 3.6 µm



Dual-image exposure

Varga, Ksenija, et al. "Exploring Capabilities of Maskless Lithography for Dual—Image Exposure in FO WLP." 2023 IEEE 73rd Electronic Components and Technology Conference (ECTC). IEEE, 2023.

[17]

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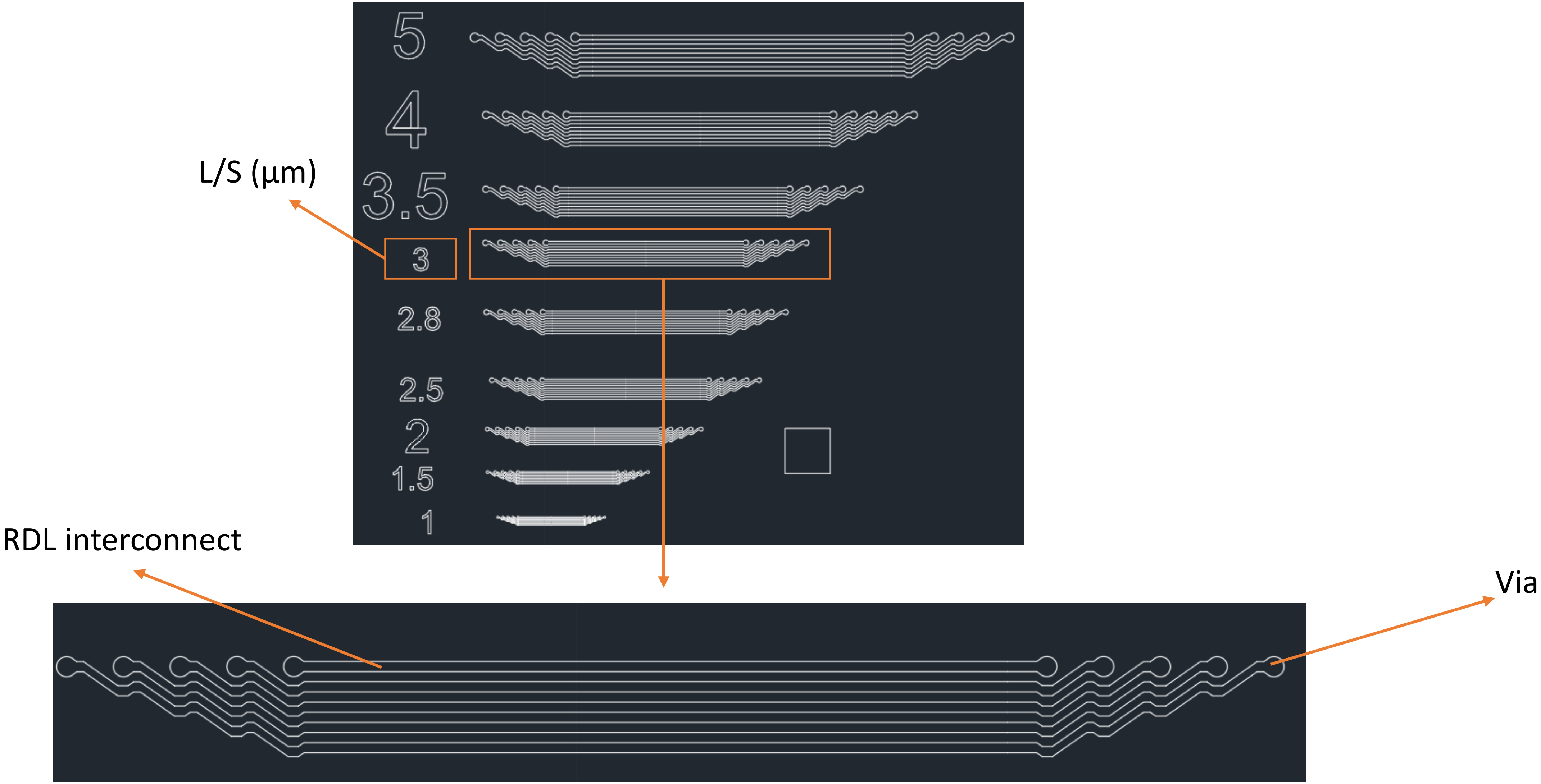
Pattern Design



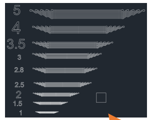
Fabrication Process

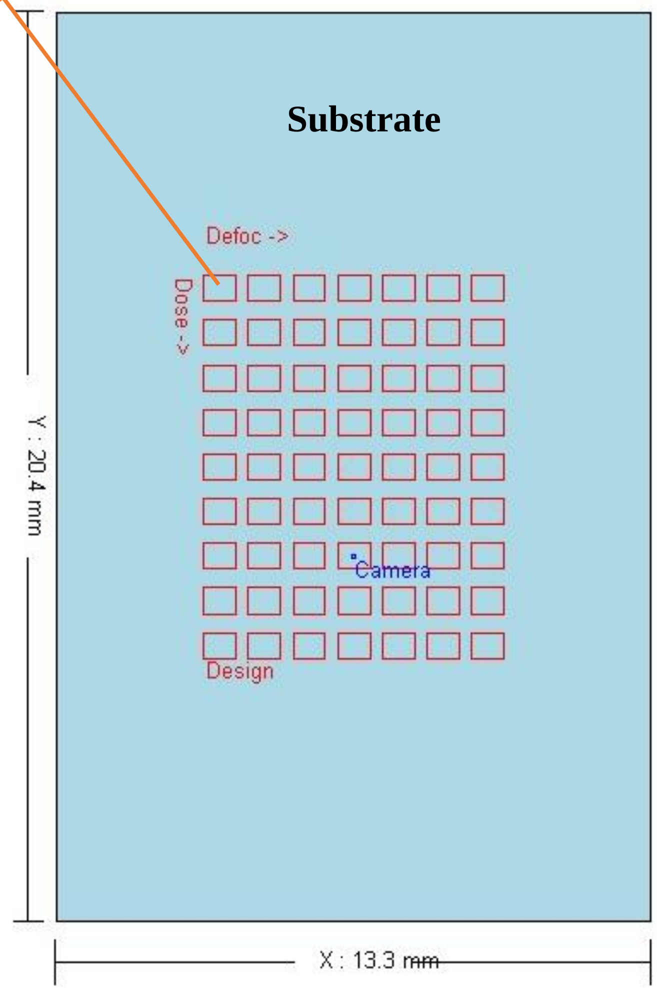
- Hexamethyldisilazane (HMDS) applied on the wafer to form a hydrophobic surface and improve the adhesion between PBO and the wafer
- 2.7 µm-thick (after development) PBO HD8820 spin coated
- Soft bake to drive out the solvent
- LDI patterning and development
  - Development time optimized for the specific thickness

Process	Parameters
PBO Spin Coating	9000rpm/60s
Soft Bake	120℃/180s
Exposure	405nm laser
Development	Aqueous Developer AZ 300 MIF/ 85s

Series Exposure

- Pattern exposed with different dose (mJ/cm^2) and defocus
- PBO top surface (defocus defined as 0) found with 670nm laser
- Positive defocus - focus moves down, into the PBO
  Negative defocus - focus moves up, away from the PBO
- Each box represents a particular combination of dose and defocus.





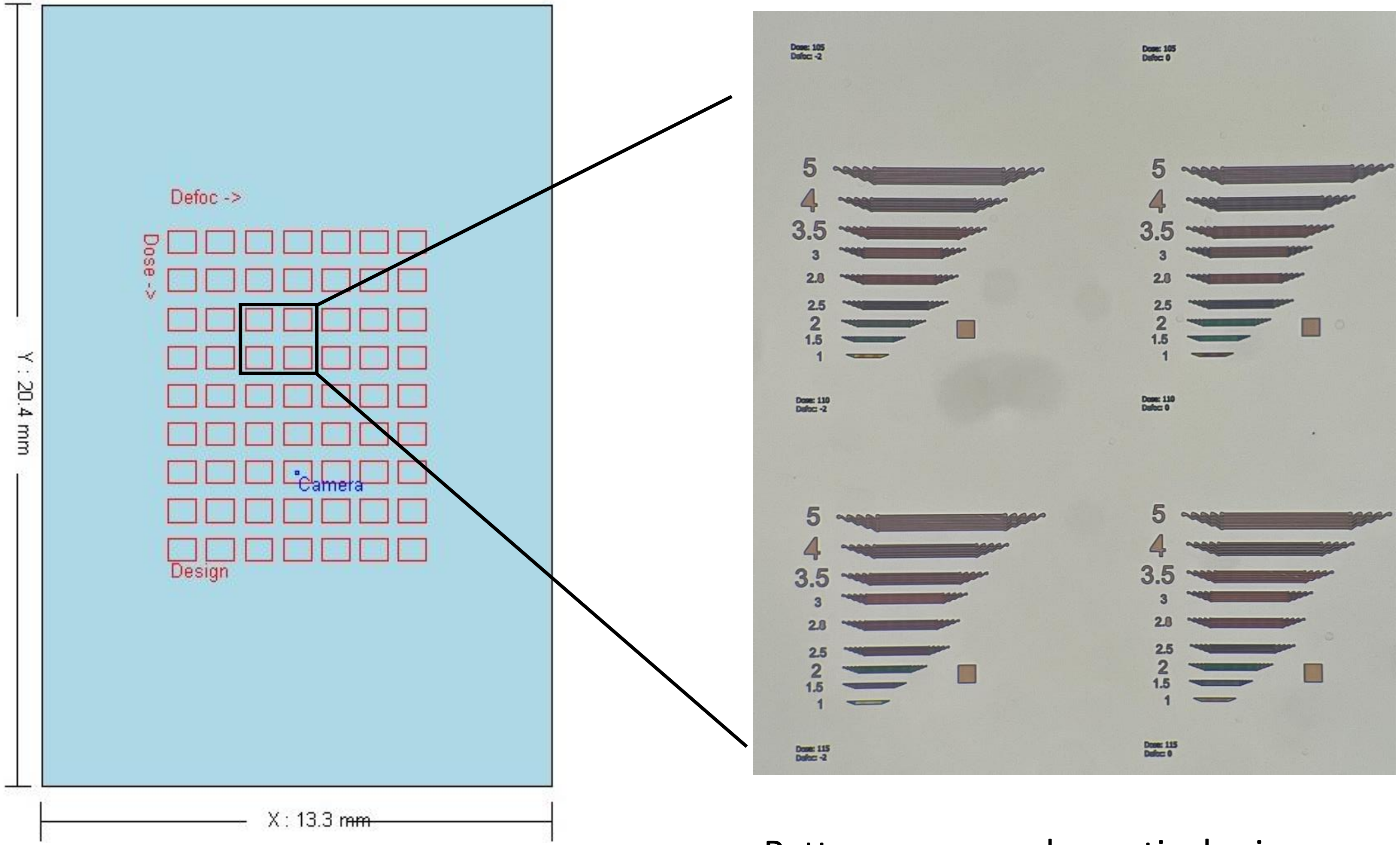
Series Info

Series Parameters

Name	Job5281_Series	
Step Size X / Y [mm]	1.0	1.0
	Dose	Defoc
Number of Fields	9	7
Start Value	100	-6
Step Size	5	2
End Value	140	6

An example of series exposure setup (screenshot)

Series Exposure Array



Pattern array under optical microscope

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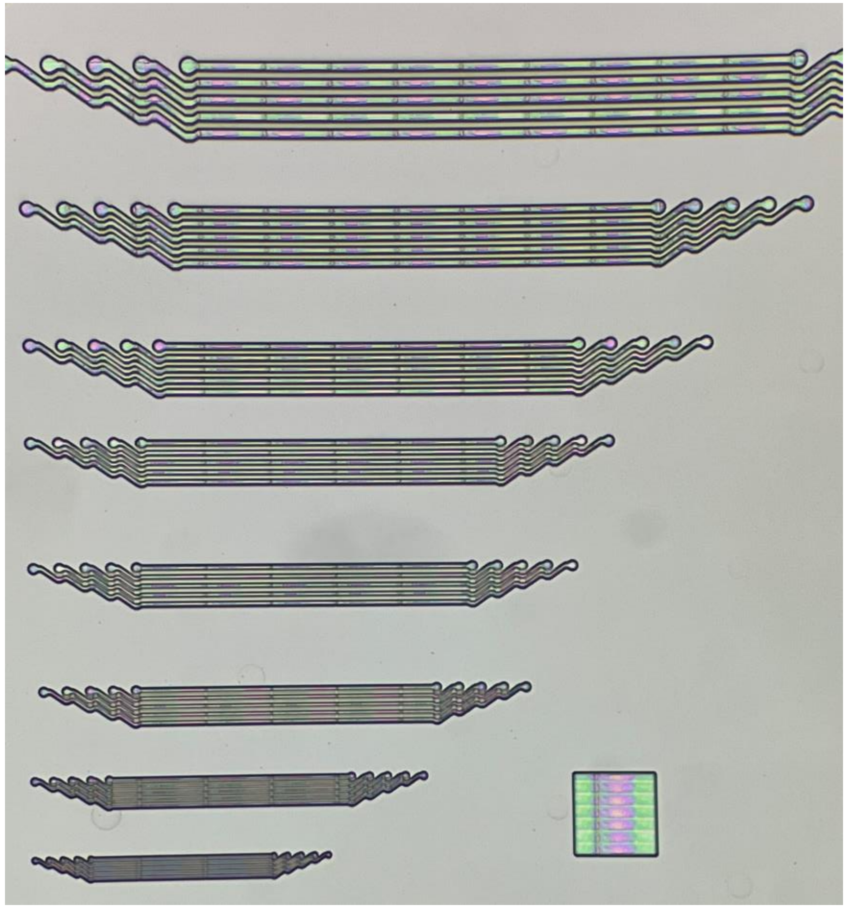
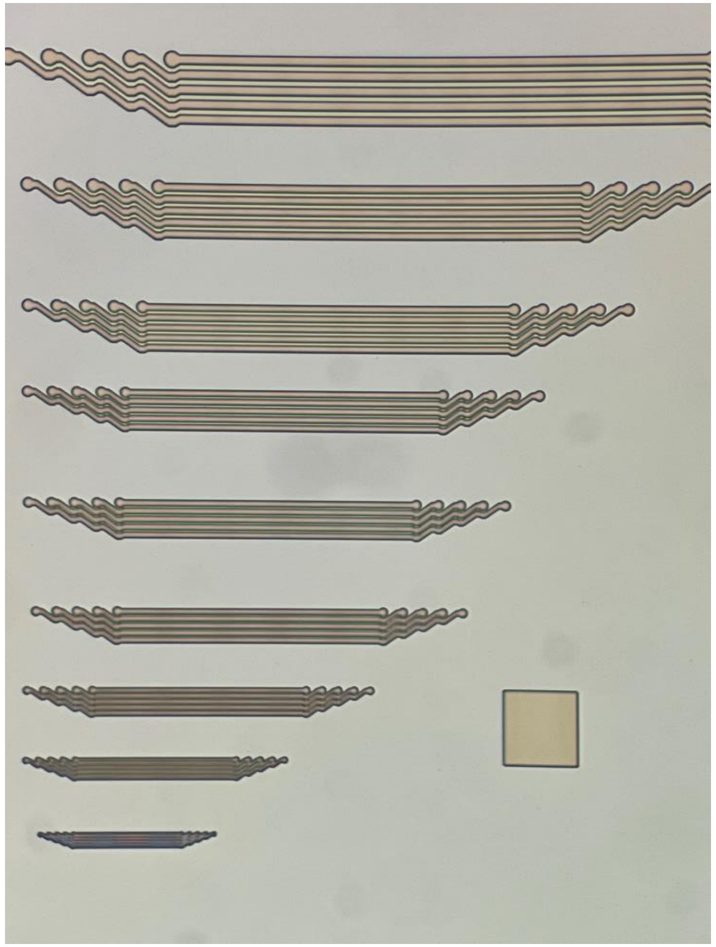
Patterns Under Optical Microscope

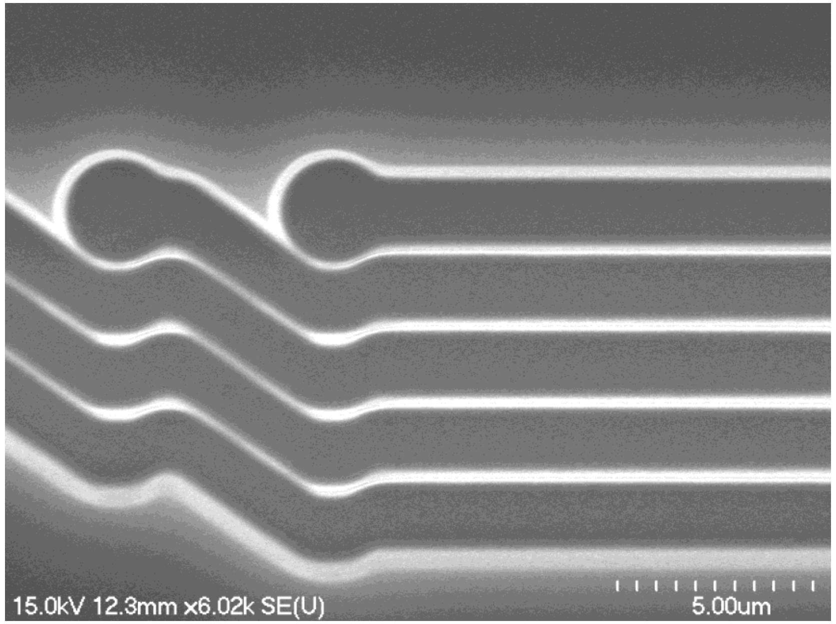


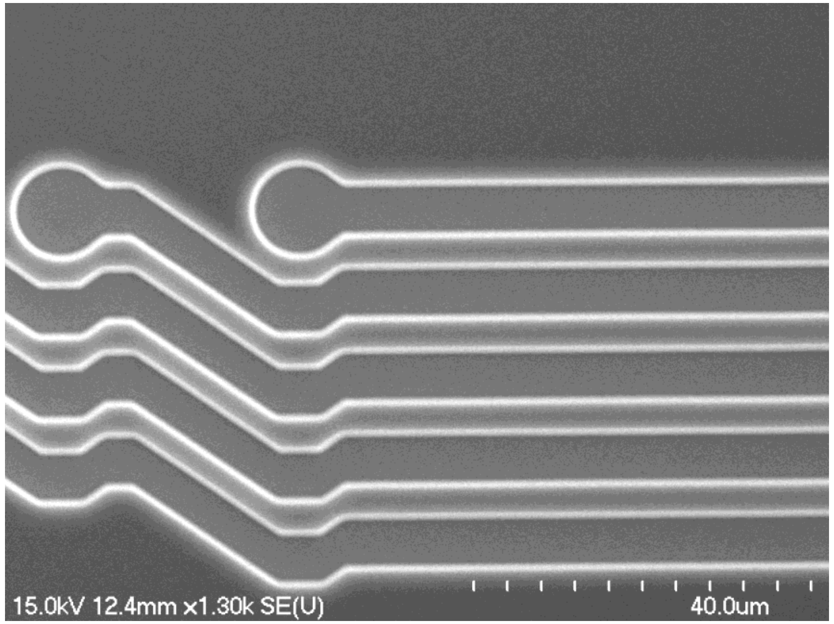
Underexposed or underdeveloped pattern



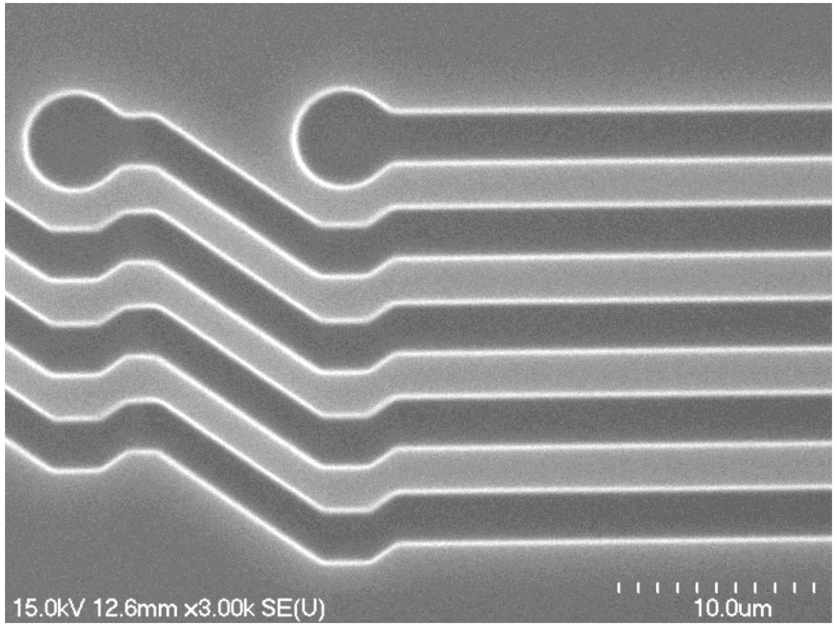
Properly exposed and developed pattern

SEM Metrology



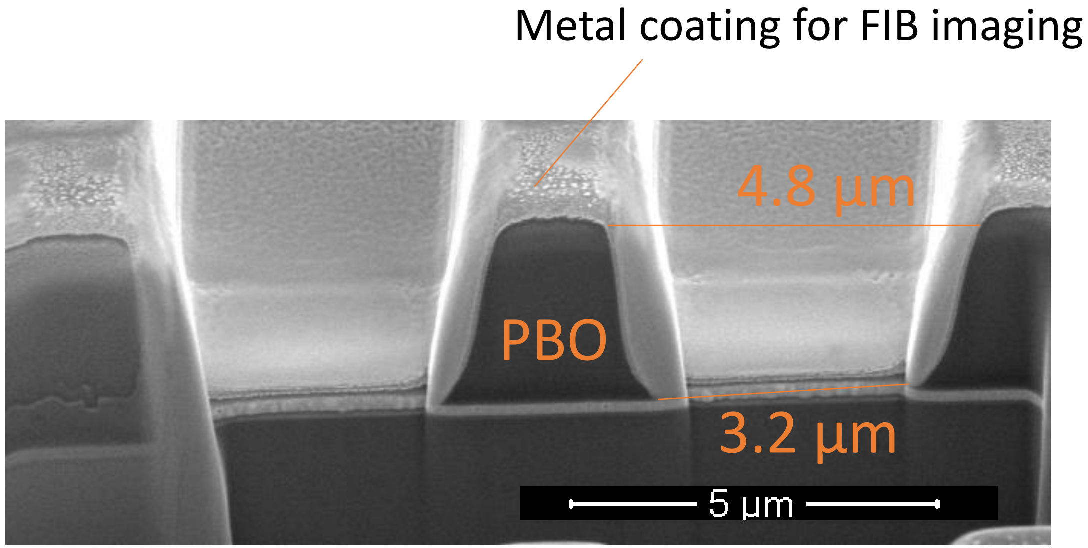


Overexposed pattens



Optimally exposed and developed patten

Cross Section of Overdeveloped PBO - 3 µm L/S



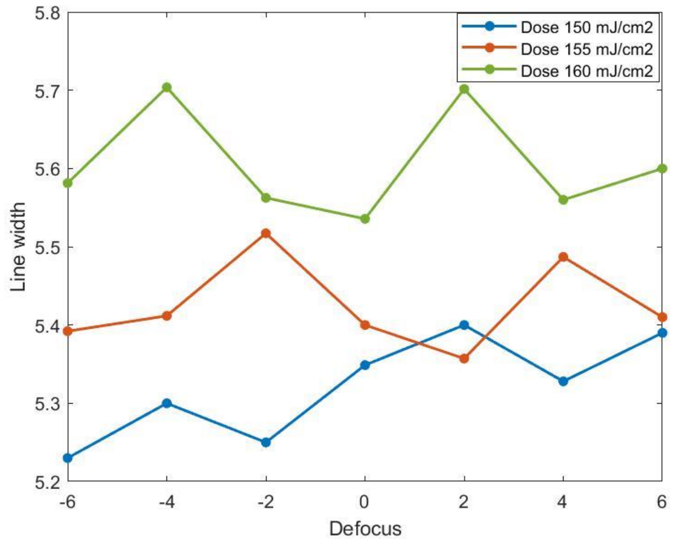
Cross section of overdeveloped PBO by FIB

- Top width - 4.8 µm, Bottom width - 3.2 µm
- The overcut profile (top width > bottom width) could be due to overdevelopment.

Line Width VS Dose and Defocus

Exploring the effect of exposure conditions on line-width

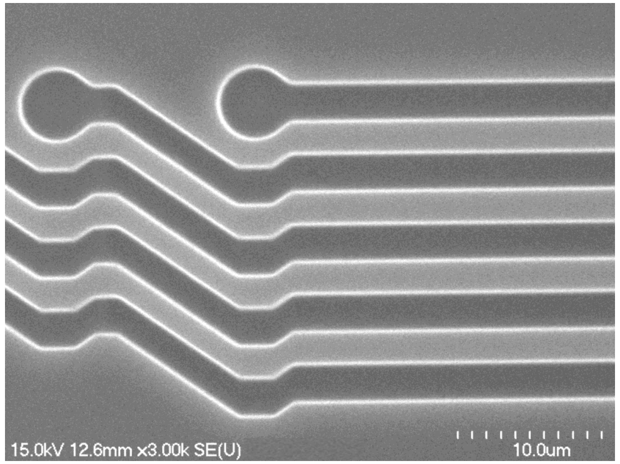
- Test Sample: 5µm L/S design
- Exposure dose - major factor affecting the line width.
- Defocus - Variation of <5% in line width



Line width for 5µm L/S design as a function of defocus

Optimal dose and defocus parameters for 2.5 µm L/S pattern:

- Dose: 125 mJ/cm^2
- Defocus: 2



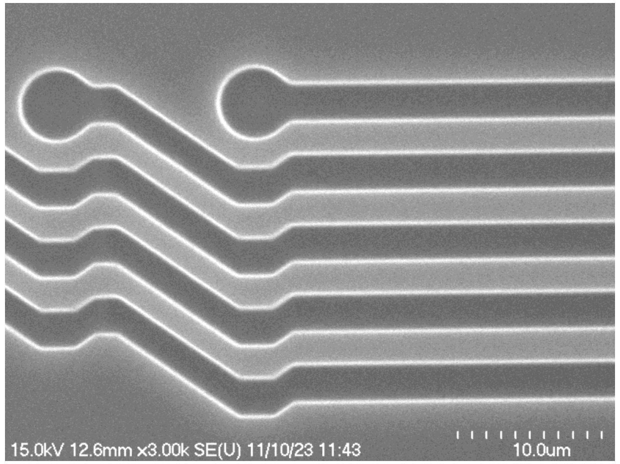
L/S: 2.5µm

Future work

- Developing fine pitch L/S patterns using PBO materials with higher resolution and lower curing temperature.
- Seed layer deposition and Cu plating on fine pitch PBO pattern
- Multiple layer RDL design and fabrication

Conclusion

- Fine pitch L/S patterns were designed and fabricated using photosensitive PBO and LDI.
- A minimum L/S of 2.5µm was achieved.
- The effect of exposure dose and defocus on line-width was explored.



L/S: 2.5µm

Thank you!