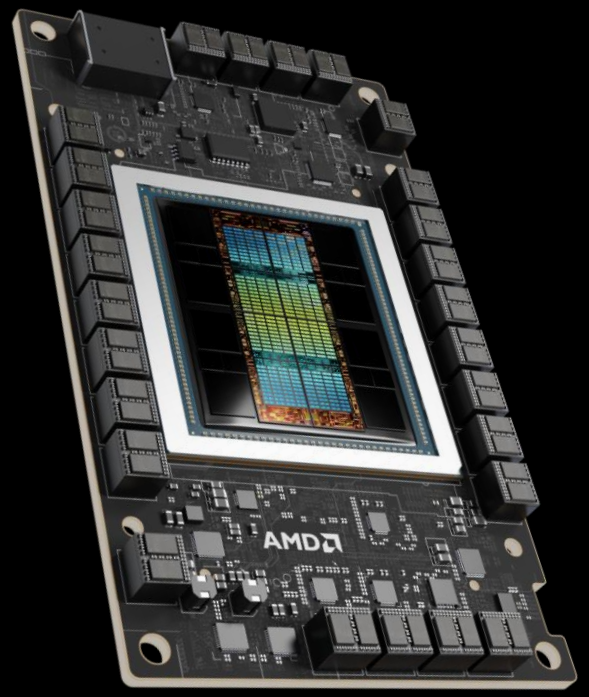
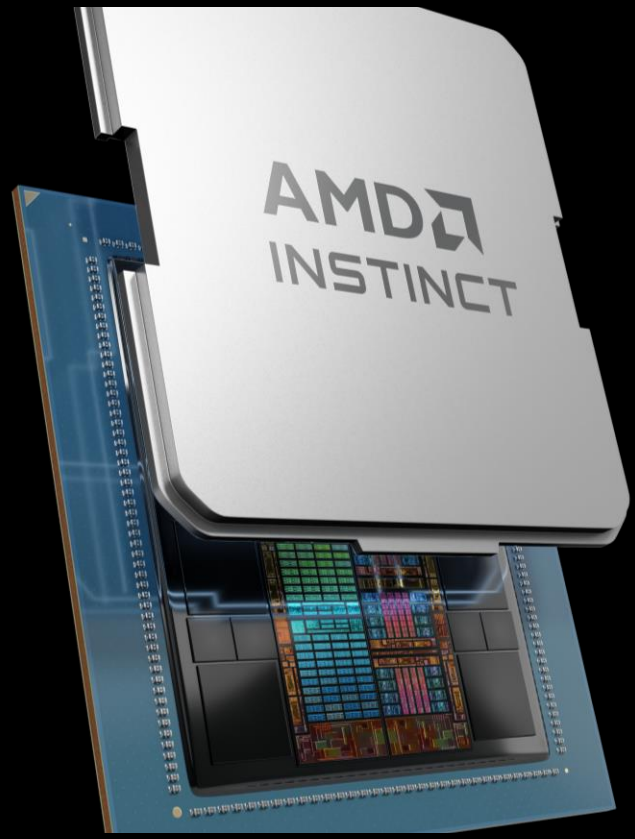
3.5D PACKAGING FOR HETEROGENEOUS INTEGRATION





CHINTAN BUCH

MEMBER OF TECHNICAL STAFF

ADVANCED PACKAGING

AMD SANTA CLARA

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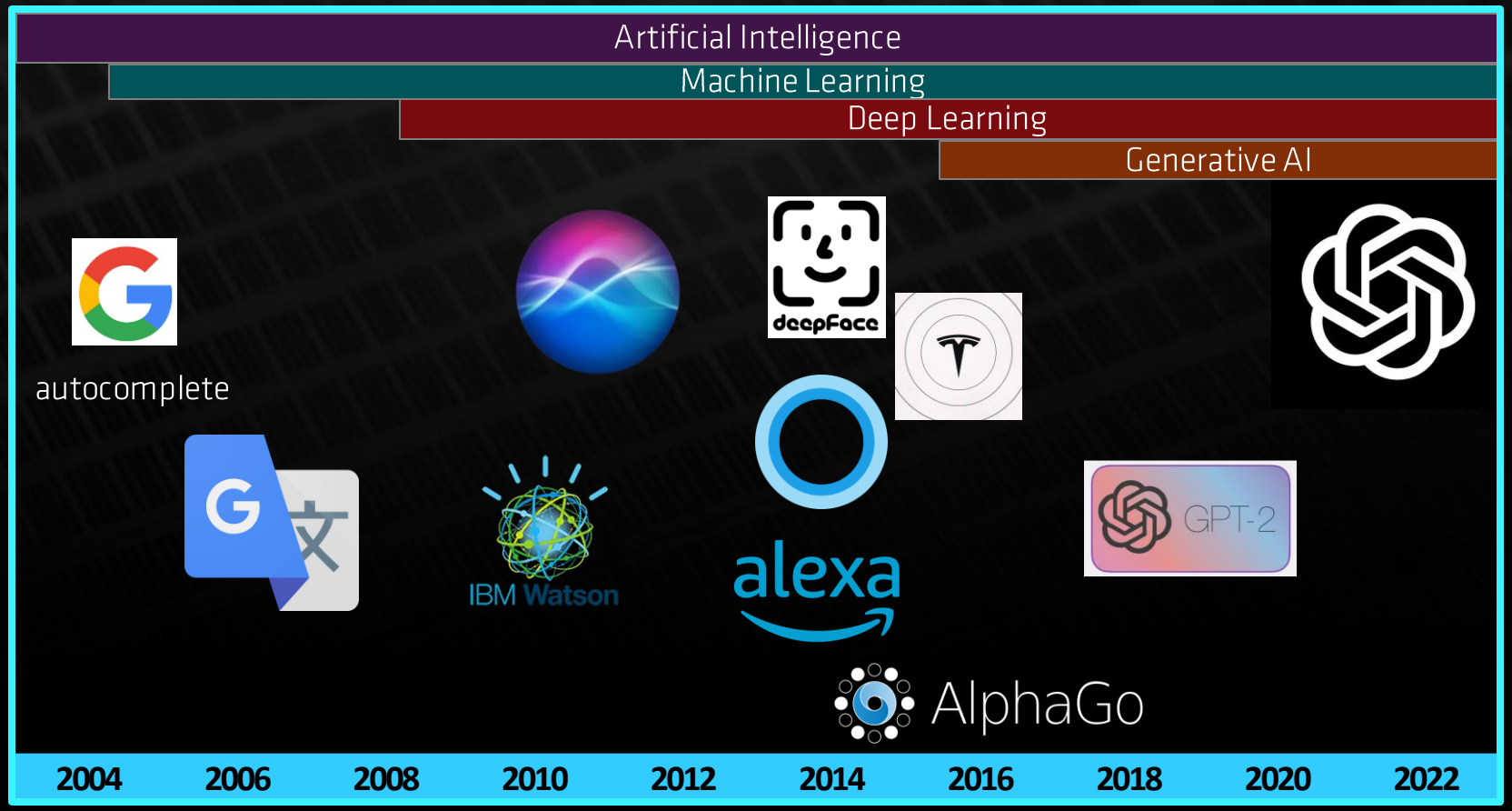
AGENDA

- AI evolution and compute needs
- AI hardware considerations and challenges
- 3.5D packaging motivation
- 3.5D packaging on AMDs INSTINCT™ MI300A/X
  - 3D hybrid Cu-Cu bonding
  - 2.5D integration of heterogeneous chiplets
  - Thermal management

Artificial Intelligence Evolution



- AI has been around for over 2 decades
- Big data, neural network application and hardware enabled rapid growth in the last 5-6 years
- Evolution of AI has increased the need for higher compute performance

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Hardware Considerations

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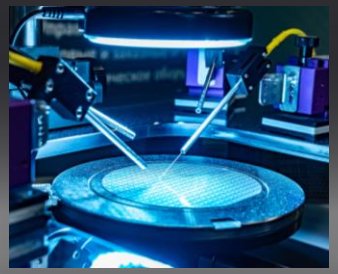
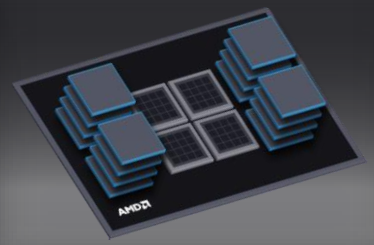
Hardware Challenges



Silicon

Increased density
High Perf/watt

Scaling/yield challenges



Memory

High Capacity/BW
Low latency

Near ASIC integration

High Speed Signaling

Effective signal delivery

Signal Integrity related issues

Power Delivery

High power requirements

High current delivery related issues

Thermals

Effective Heat removal

Thermal management and related performance

- Silicon, memory and HSIO requirements continue to challenge hardware
- Advanced packaging innovations can help address these challenges

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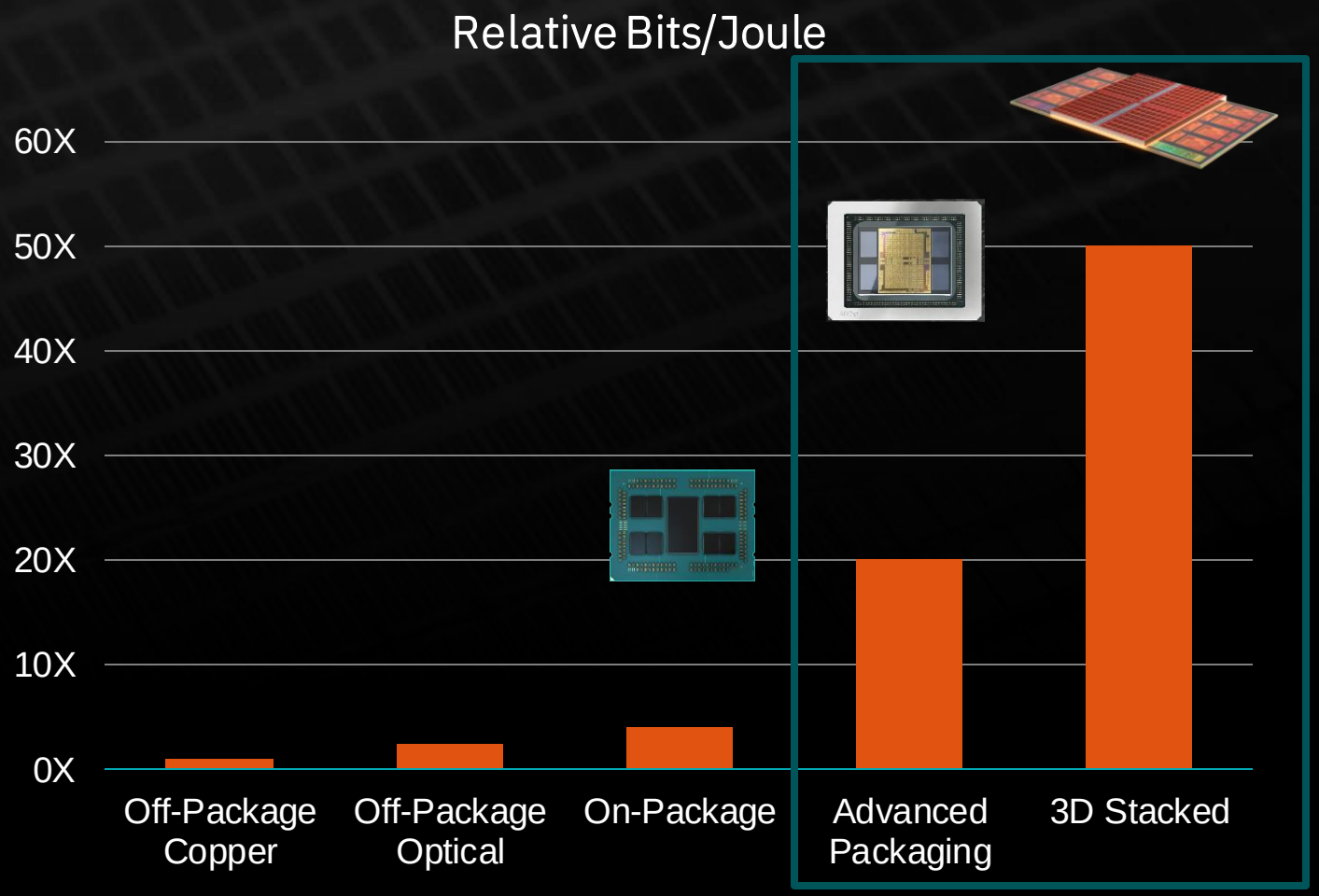
3.5D Packaging Motivation

- The key to power-efficient performance is tight integration
- Advanced 3D Hybrid bonding provides by orders of magnitude the densest, most power efficient chiplet interconnect
- Advanced 2.5D enables more compute and HBM in a package
- Increased system-level efficiency



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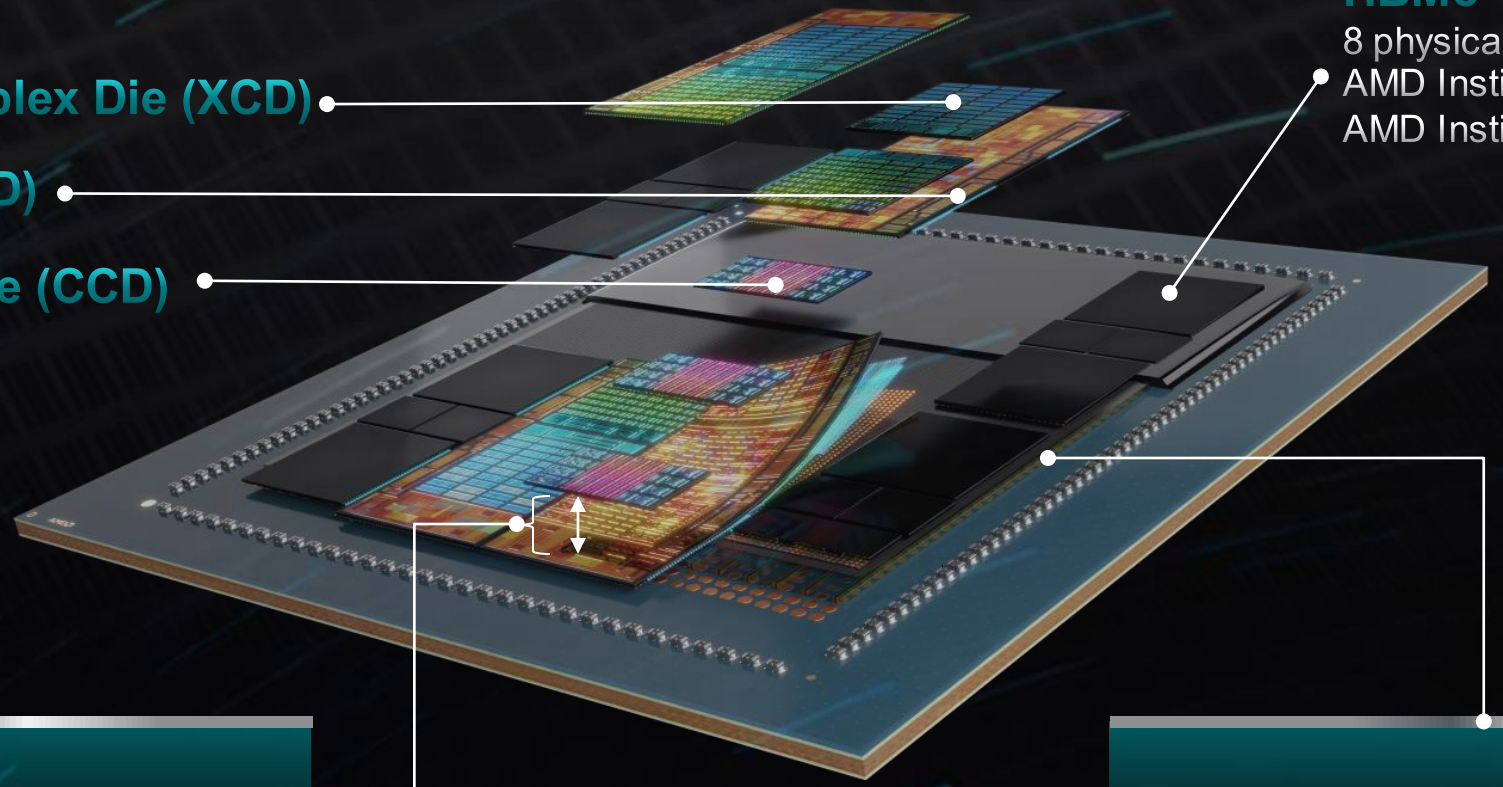
AMD Instinct™ MI300 3.5D Modular Chiplet Package



Accelerator Complex Die (XCD)

I/O Die (IOD)

CPU Complex Die (CCD)

HBM3
8 physical stacks
AMD Instinct™ MI300A: 128 GB (8H)
AMD Instinct™ MI300X: 192 GB (12H)

Advanced 3D Cu-Cu Hybrid Bonding

2.5D Interposer for Memory Integration

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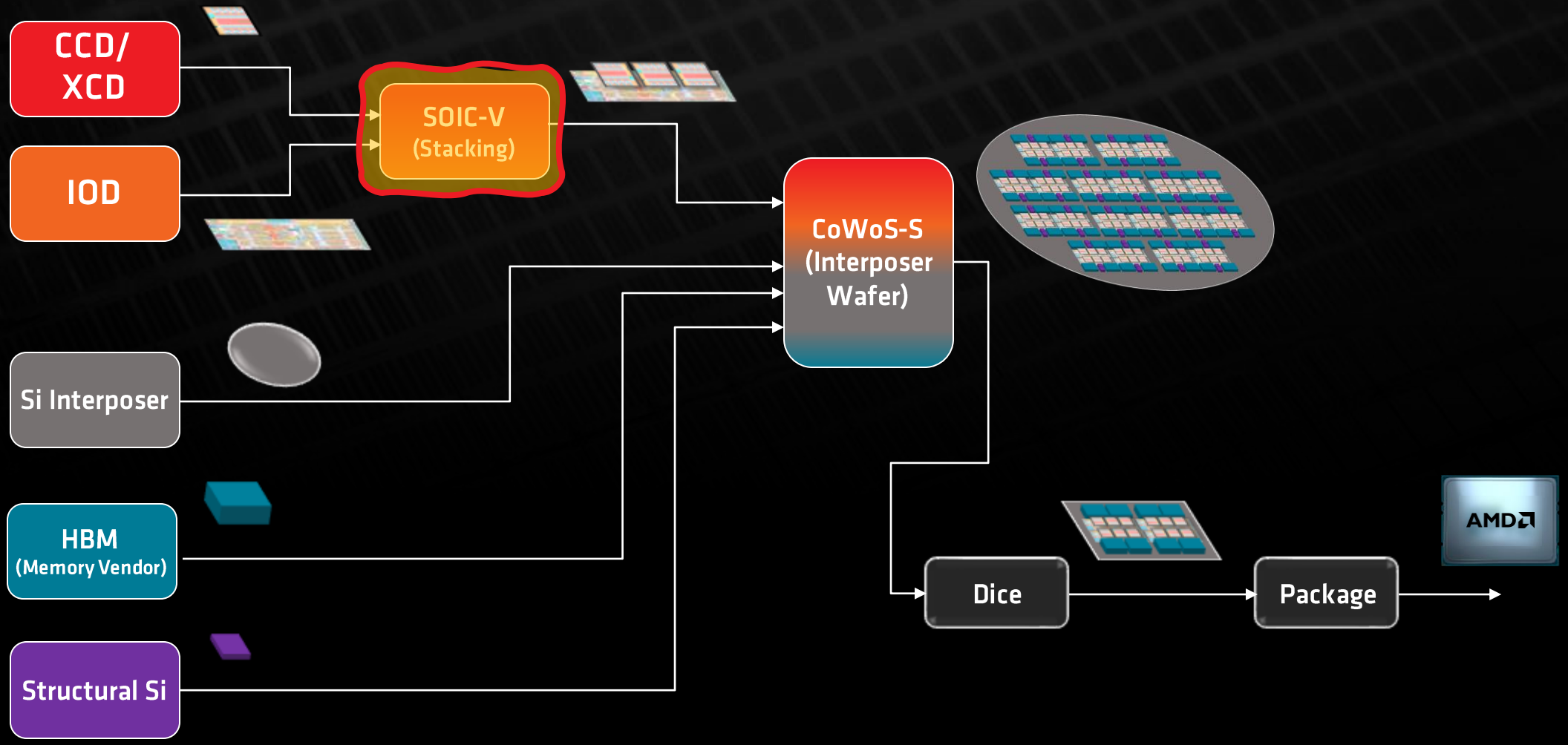
MI300 Advanced Packaging Flow

Multiple silicon components, multiple integration, and packaging technologies



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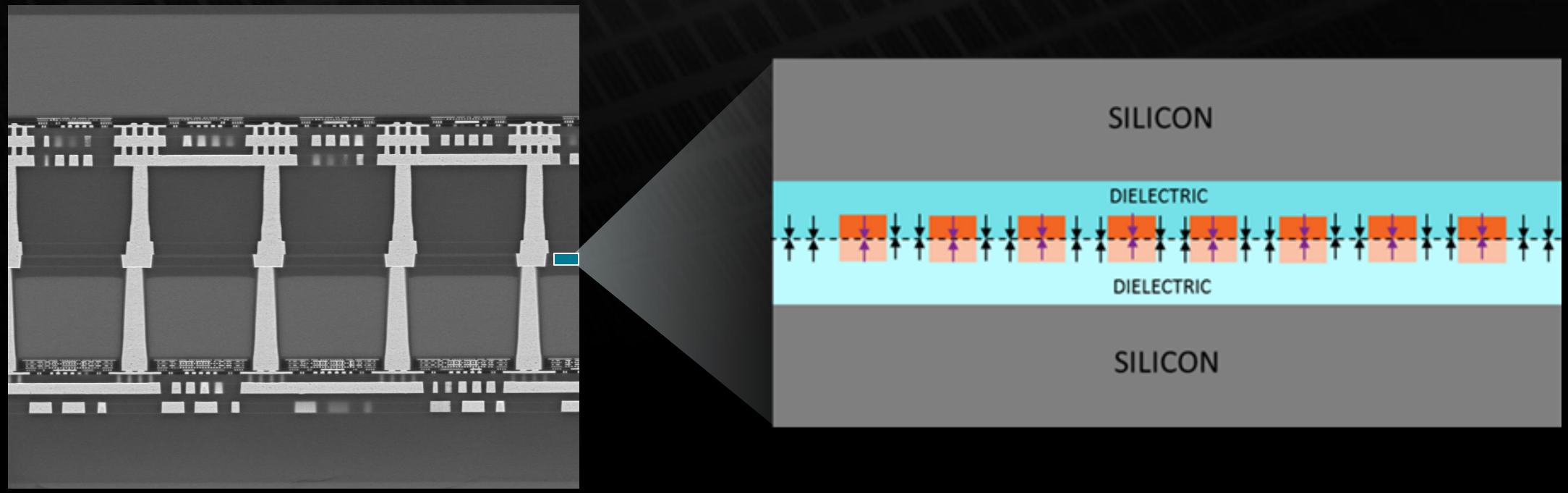
3D Cu-Cu Hybrid Bonding

3D Stacking Technology

Hydrophilic dielectric-dielectric + Cu-Cu bonding

- MI300A/X uses "hybrid bonding" 3D stacking technology for vertical 3D-stacking of XCDs & CCDs on IOD
- Dense through-silicon via (TSV) interface is used for connection to IOD data fabric (NoC)
- 9um TSV pitch enables 10000s of connections/mm2 between XCD/CCD and IOD



Enables >3X interconnect energy efficiency, >15X interconnect density and better signal and power performance (as compared to micro bumps*)

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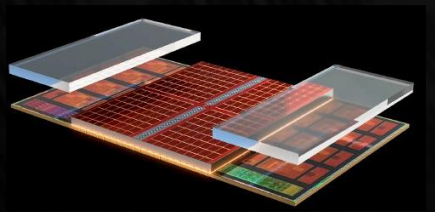
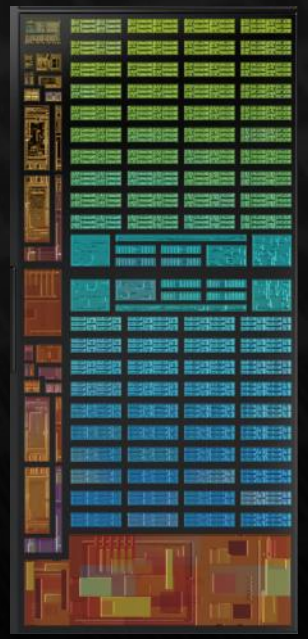
3D Stacking Technology Evolution

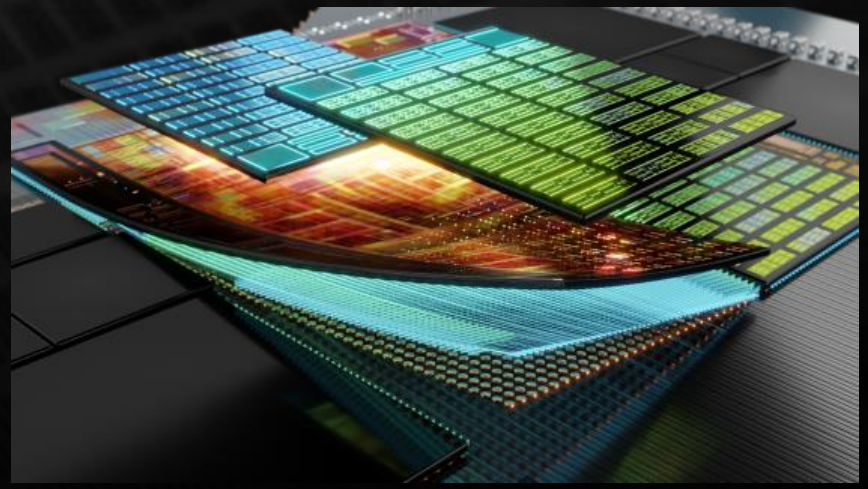
AMD 3D V-Cache™ Technology





- Hybrid Bonding size: ~7 x10 mm
- Logic die as base
- N7 (X3D) on N5 base (CCD) die
- Significant performance gains for desktop gaming and servers
- Up to 2.5TB/s vertical bandwidth

AMD Instinct™ MI300 Accelerator



- Leverage integration and manufacturing learnings from V-cache
- Hybrid Bonding size: ~13 x 29 mm (0.45x reticle)
- Logic die on top enables improved thermals
- N5 XCD/CCD stacked on N6 base die (IOD)
- Same 9µ TSV pitch
- Up to 17TB/s vertical bandwidth

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Future of 3D Stacking

TSV Pitch

FULL DIE-TO-DIE	IP ON IP	MACRO IN MACRO	IP FOLDING/SPLITTING	CIRCUIT SLICING

ADVANCED PACKAGING CAN ENABLE INTEGRATION SCHEMES NOT POSSIBLE WITH MONOLITHIC DESIGNS

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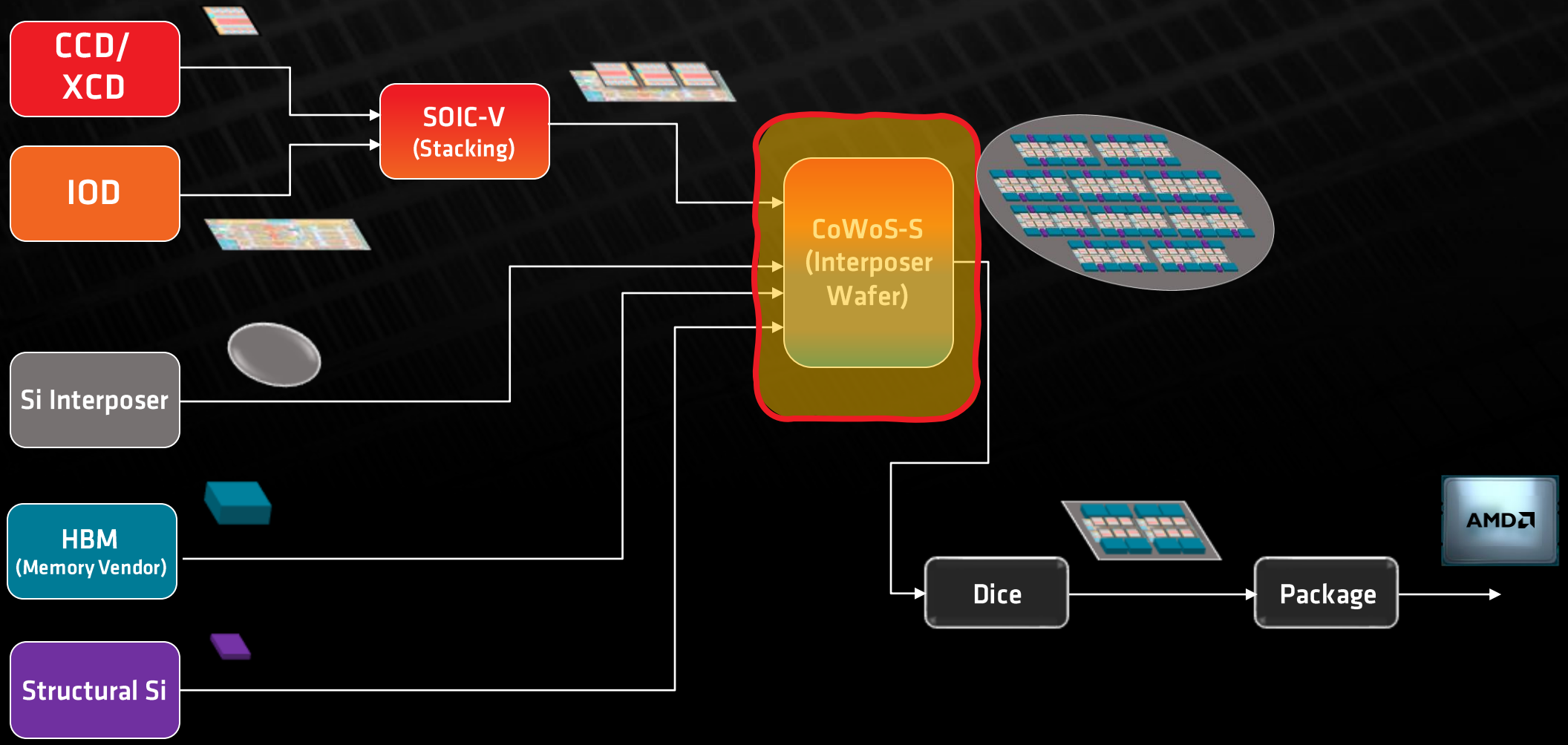
MI300 Advanced Packaging Flow

Multiple silicon components, multiple integration, and packaging technologies



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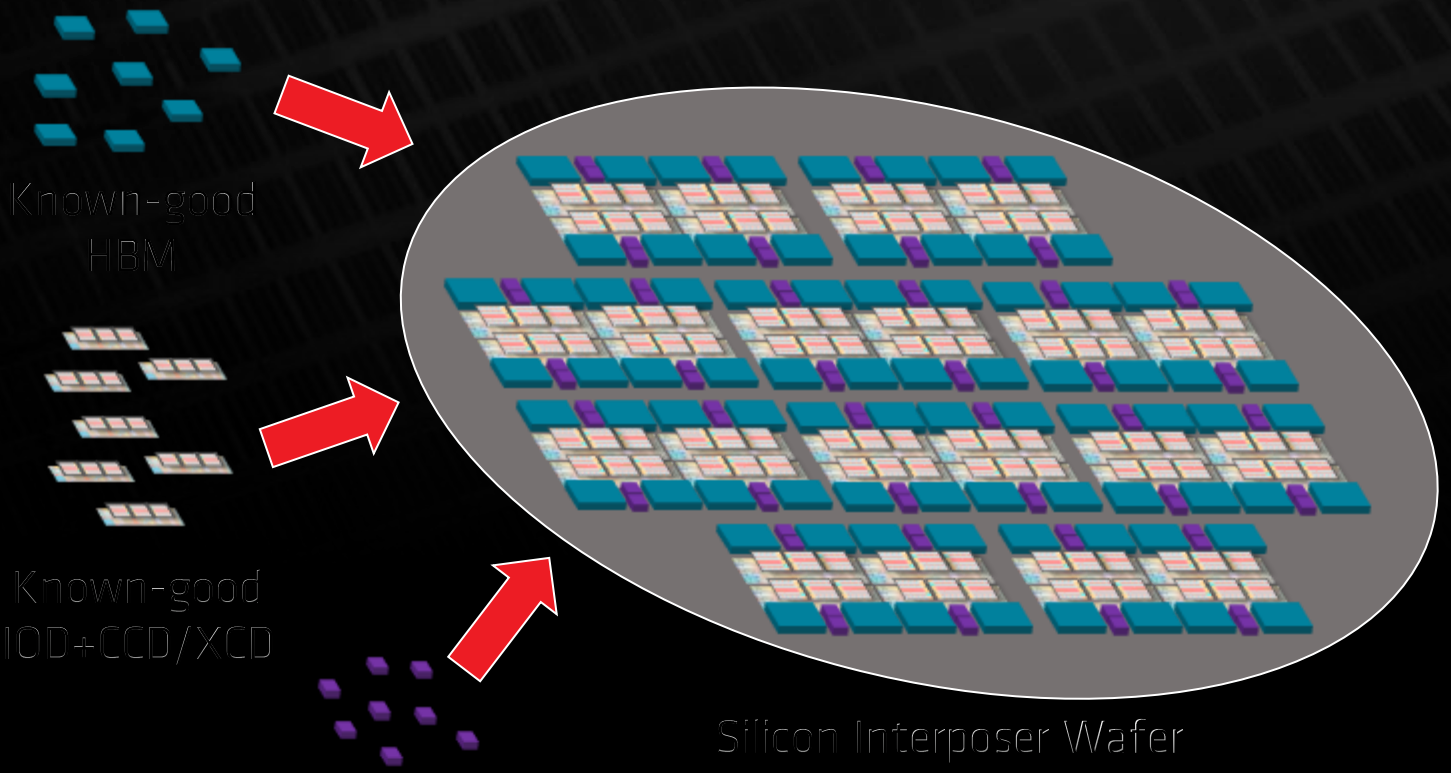
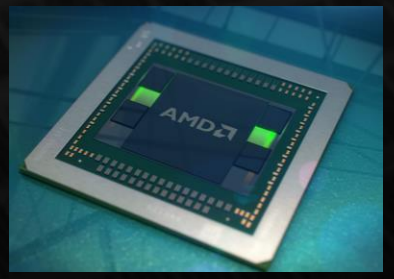
2.5D Integration of SoC and High Bandwidth Memory

CoWoS-S: 2.5D Heterogeneous Integration Technology

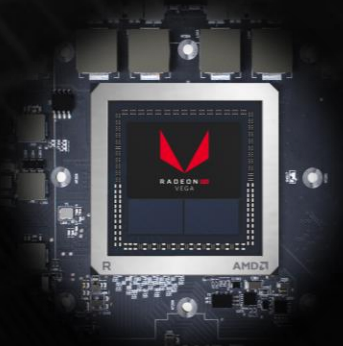
3D SoIC (IOD+XCD/CCD) modules, HBMs, and structural Si die are picked-and-placed on interposer



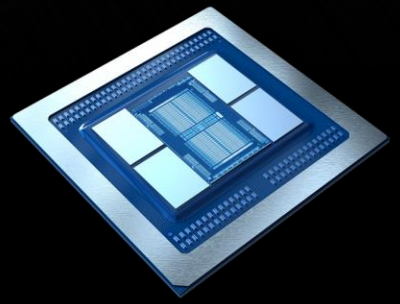
Standard technology with years of experience for GPUs, HBM



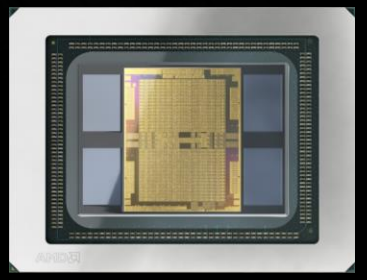
AMD Radeon™ R9 Fury GPU (2015)



AMD Radeon™ RX Vega64 GPU (2017)



AMD Instinct™ MI60 Accelerator (2018)



AMD Instinct™ MI100 Accelerator (2020)

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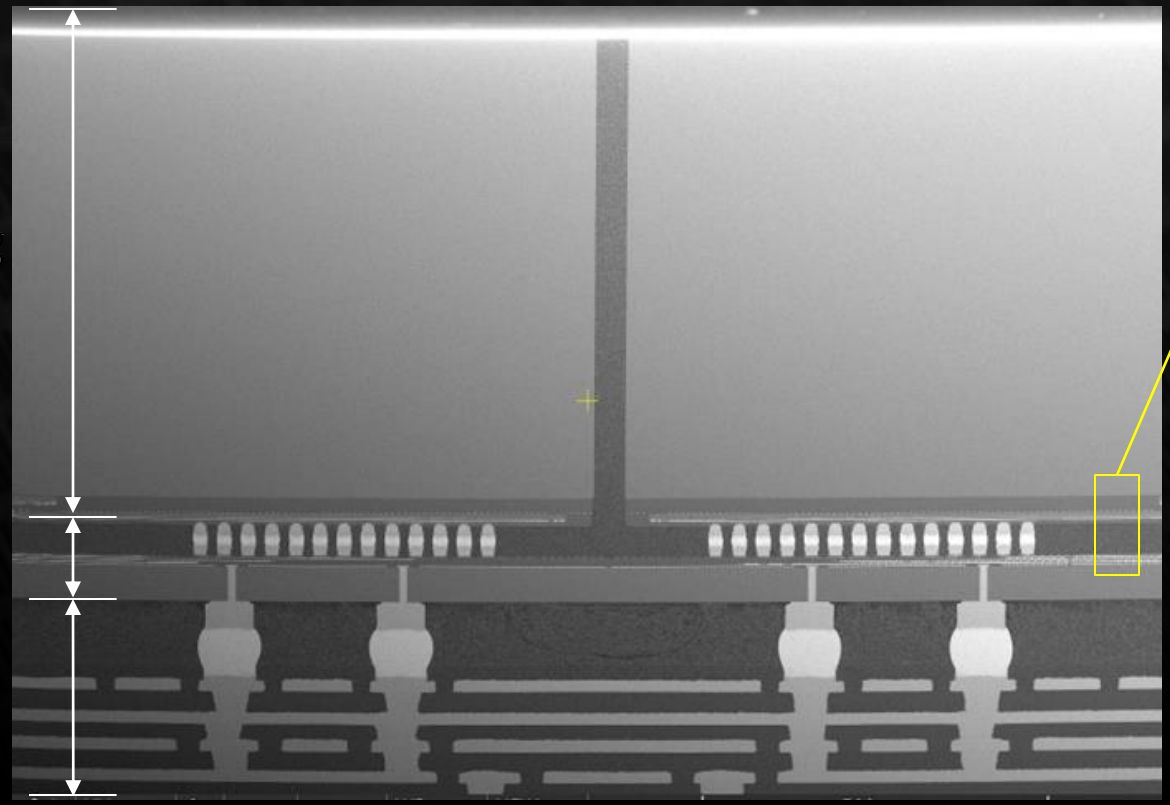
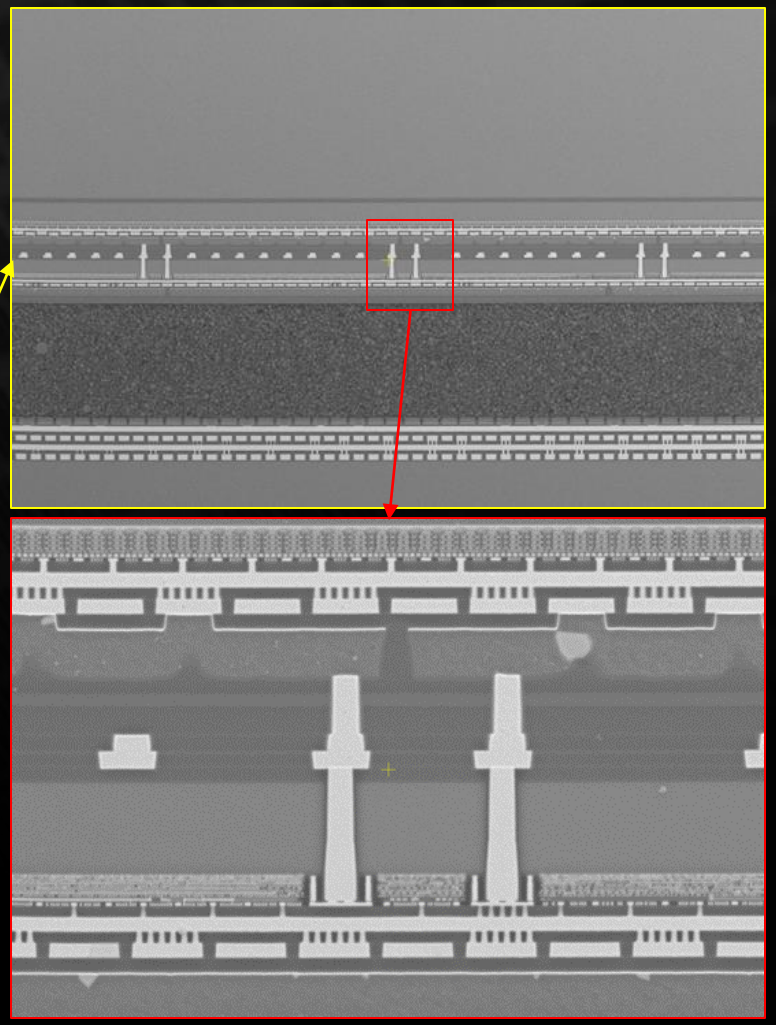
CoWoS-S: What's New?





- 2.5D and 3D heterogeneous integration of CCD + XCD + IOD + HBM + structural Si on larger, thinner Si interposer
- First implementation of novel metallization scheme for improved signal integrity at peak memory bandwidths
- Assembly at fine pitch of 35um to enable ultra-short-reach (USR) interconnects

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Fundamentals of Thermal Management

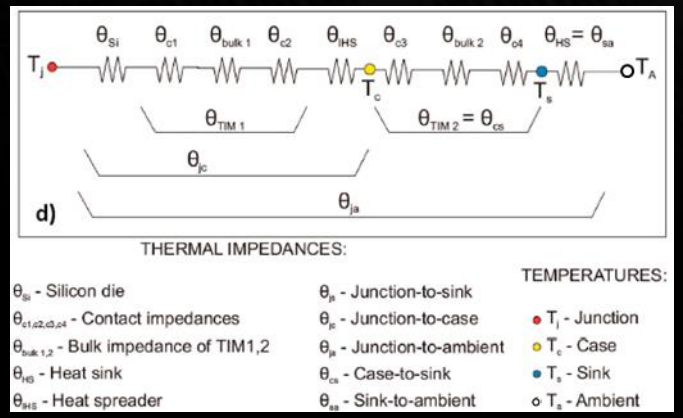
- Heat transfer out of MI300A/X package and Integrated Heat Sink (IHS) occurs in multiple stages

Requirements for low package-level thermal resistance:

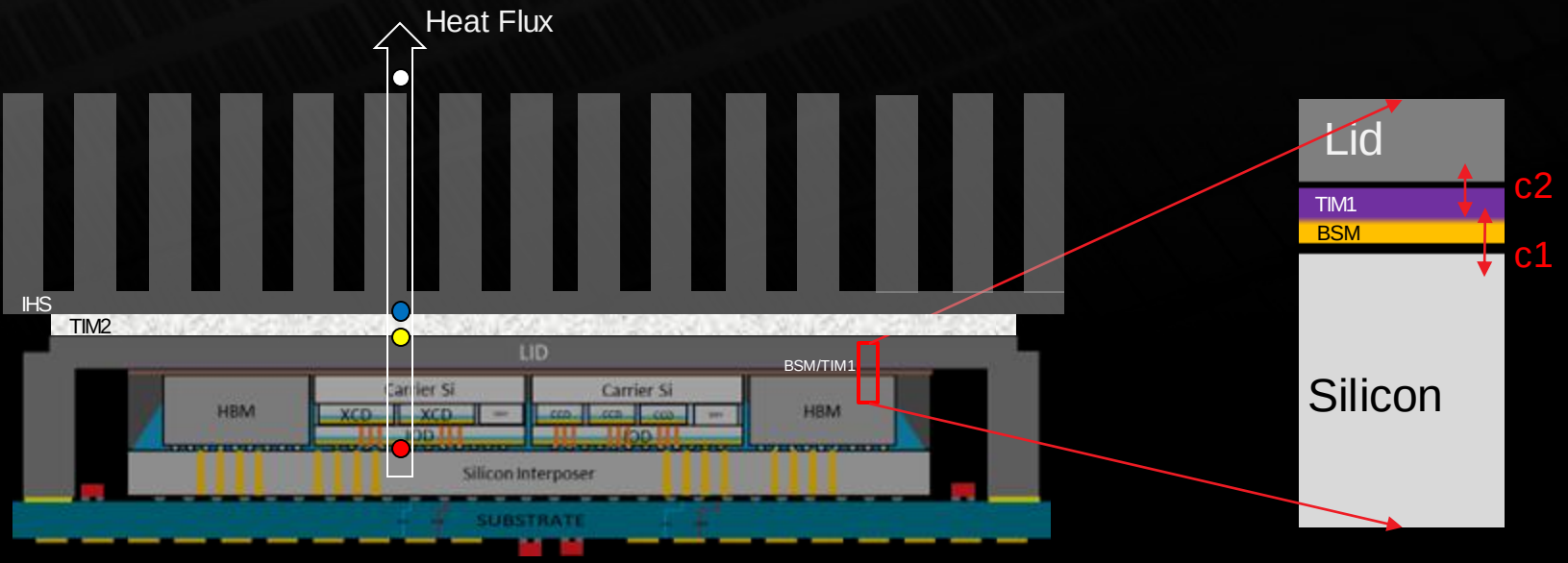
- High thermal conductivity and low Bond Line Thickness (BLT) of TIM1 material
- Low contact impedance at interfaces c1 and c2

$$\theta_{TIM} = \frac{BLT}{k_{TIM}} + \theta_{c_1} + \theta_{c2}$$

θ_{TIM1} = Total Thermal Resistance
BLT = Bond Line Thickness of Thermal Interface Material (TIM)
K_{TIM} = Bulk Thermal Conductivity of TIM
θ_{c_1} = Contact Impedance at C1 interface
θ_{c2} = Contact Impedance at C2 interface

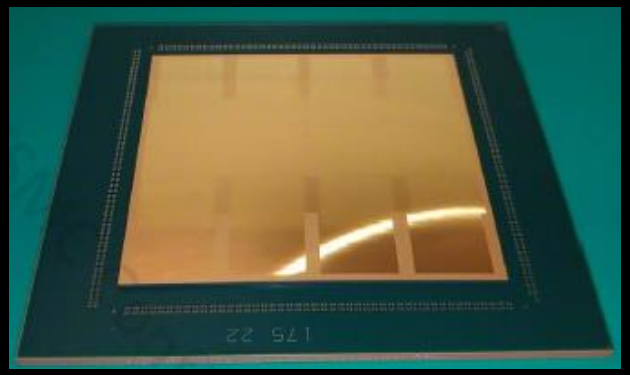


Multi-stage heat transfer through package and IHS



Back Side Metal (BSM) and Indium TIM Technology

- MI300A is a large-footprint, high-power >550W device with 8 HBM die + 4 IOD chiplets + 6 XCD chiplets and 3 CCD chiplets
  - Thermal coupling needs to be enhanced over large footprint (3.6x reticle interposer)
- Back Side Metallization on a molded CoWoS-S module enables low θ_{c_1}
- Nickel-plated copper lid design enables low θ_{c2}, enhances heat spreading effect and package warpage management
- Indium TIM solution is not a fundamentally new technology, but co-development with OSATs enabled implementation on the large molded module
  - Indium has high kTIM1 (bulk thermal conductivity) for low thermal resistance and efficient heat flux
  - Low melting temperature and good flow stress enables manufacturability



MI300 Package with BSM

Back Side Metal adhesion testing meets standards on Si as well as mold

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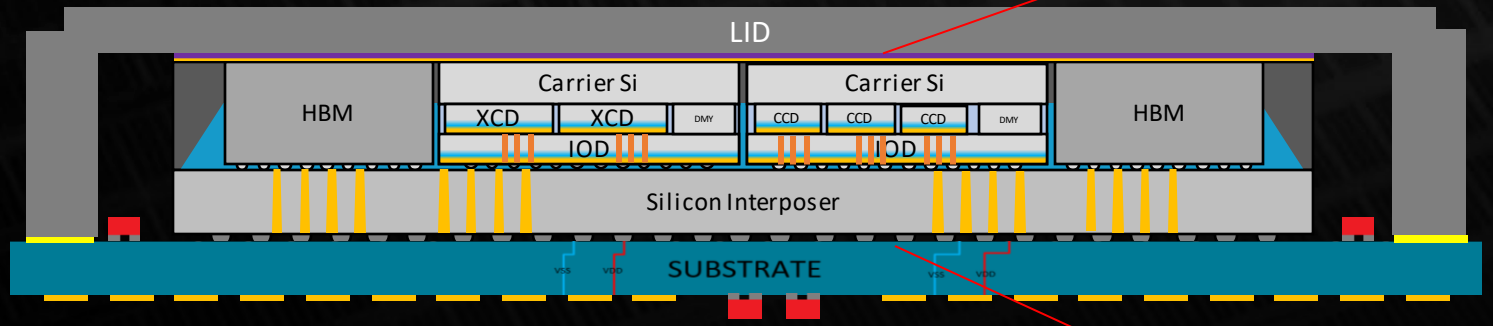
MI300A: Enabled by Advanced Packaging

Unique Thermal Architecture to support >550W TDP



3D Hybrid Bonded Architecture for XCD-IOD Perf/W benefits

2.5D Architecture for IOD-IOD and HBM integration

Large module on substrate

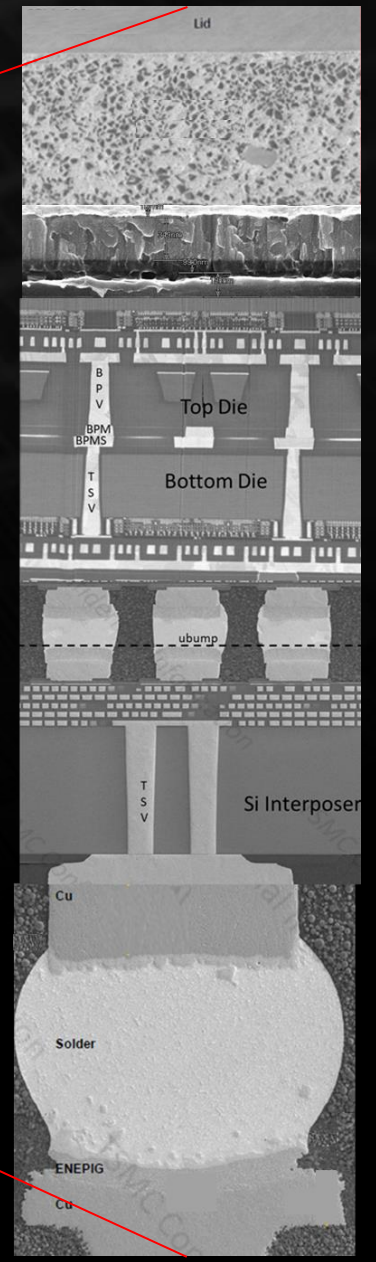


ILLUSTRATION PURPOSE ONLY

Questions?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