Overlay analysis and optimization for high-accuracy hybrid D2W bonding

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Besi

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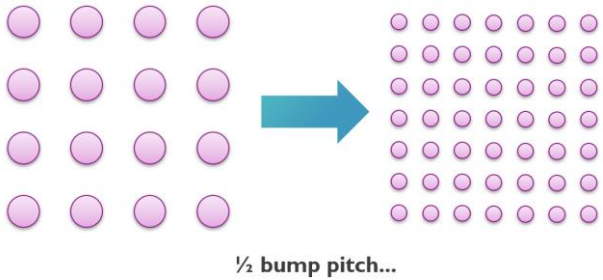
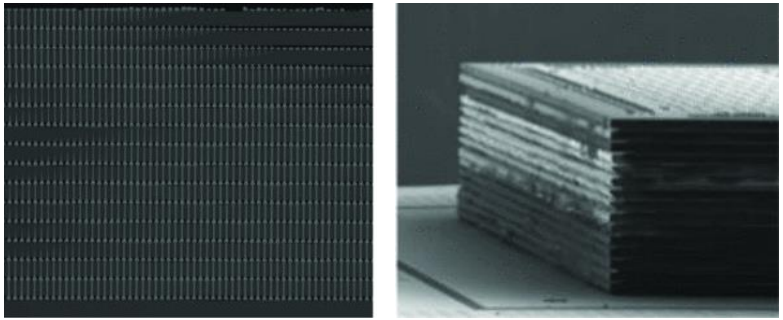
Outline

- Introduction
- Machine Baseline Alignment Capability
- Die-To-Wafer bonding overlay
- Intra-die overlay analysis

Introduction – small pitch D2W bonding

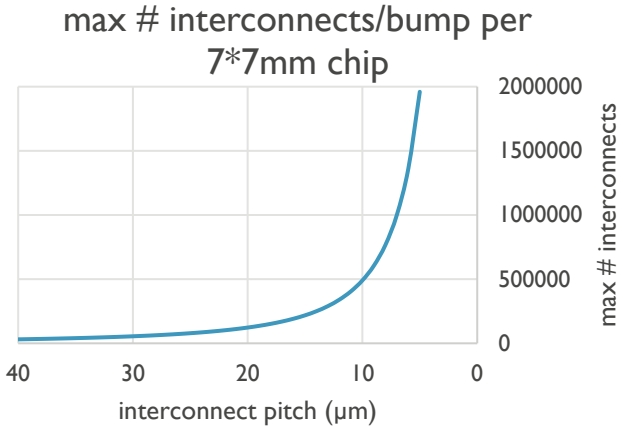


- **Chip-to chip interconnect scaling**
  - → Higher bandwidth/performance: AI, GPU, HPC
  - → Lower power consumption
- Traditional technology for small pitch D2W: **Thermal compression bonding** (TCB)
  - Traditional TCB with electroplated µ-bumps scalable to ~ 20µm bump pitch
  - New concepts (embedded, damascene landing pads), improved equipment → ~10µm bump pitch



16-layer die stack – 20 µm bump pitch TCB

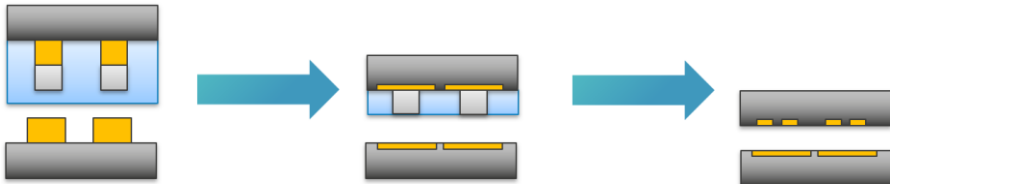
C. Gerets et al., "Process development and characterization of 3D multi-die stacking," 2020 IEEE 8th Electronics System-Integration Technology Conference (ESTC), Tønsberg, Norway, 2020, pp. 1-6, doi: 10.1109/ESTC48849.2020.9229814.

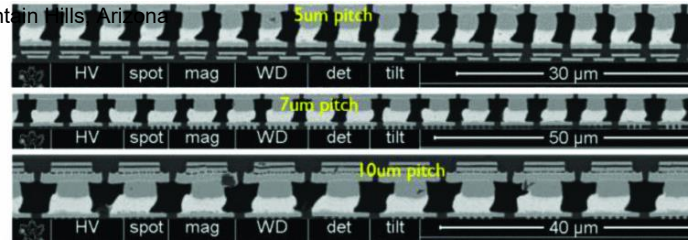


Introduction – small pitch D2W bonding

- **Below 10µm bump pitch → TCB increasingly difficult**
  - Heated process, elevated force → accuracy?
  - Solder bridging, high aspect ratio bumps (fragile)

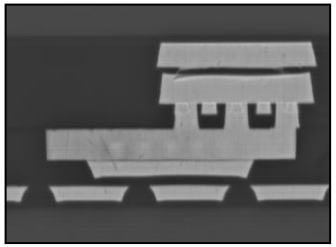
- **Sub- 10µm interconnect pitch scaling: hybrid D2W bonding?**
  - Cu pads embedded in bonding dielectric – easier to scale (damascene process)
  - Room temperature direct bonding mechanism
  - High accuracy bonding equipment available on the market (i.e. BESI Chameo*ultra plus*)



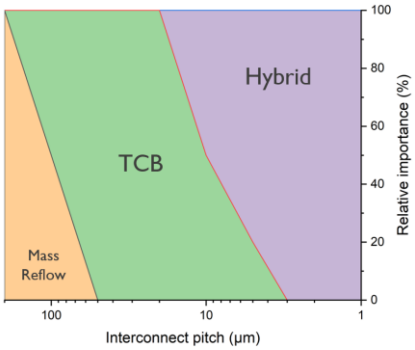


<10 µm bump pitch TCB (embedded bump)

J. Derakhshandeh et al., "10 and 7 µm Pitch Thermo-compression Solder Joint, Using A Novel Solder Pillar And Metal Spacer Process," 2020 IEEE 70th Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2020, pp. 617-622, doi: 10.1109/ECTC32862.2020.00102..



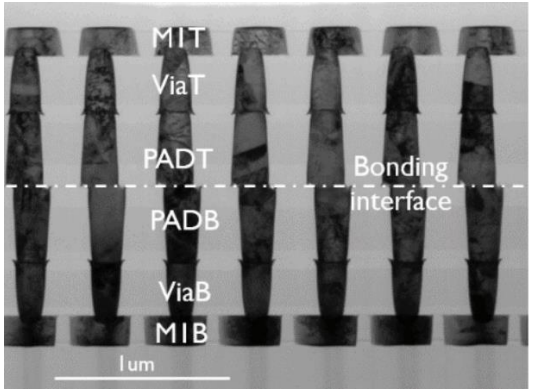
Cu/dielectric bonding interface



Estimated relative importance of different D2W bonding technologies

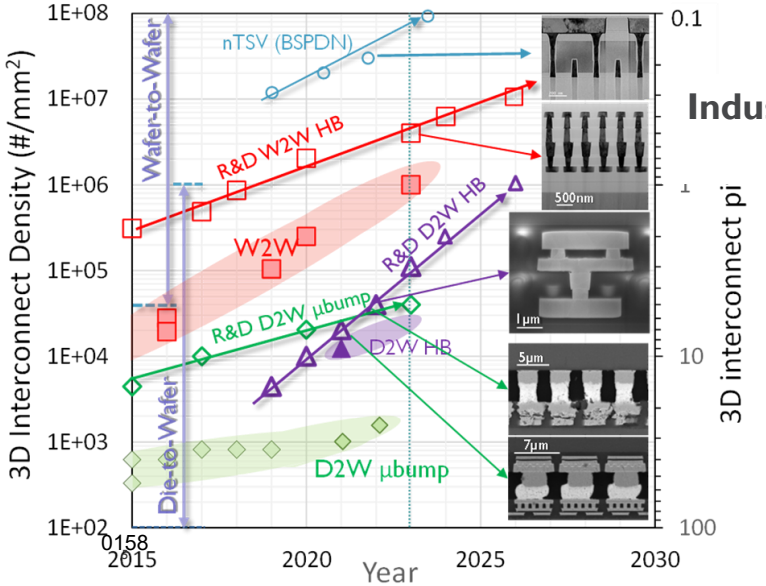
Introduction - D2W bonding overlay

- **D2W hybrid bonding is bridging the interconnect pitch gap** between TCB and W2W hybrid bonding
- Ever increasing need for higher bandwidths & speed, lower power consumption continues to drive interconnect pitch scaling
- Similar to W2W, **further scaling of D2W hybrid bonding pitch expected**



400nm pad pitch W2W bonding

S. -A. Chew et al., "The Challenges and Solutions of Cu/SiCN Wafer-to-Wafer Hybrid Bonding Scaling Down to 400nm Pitch," 2023 International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2023, pp. 1-4, doi: 10.1109/IEDM45741.2023.10413829



Industry & Imec R&D roadmap

- W2W HB - imec R&D
- W2W HB - industry
- D2W HB - imec R&D
- D2W HB - industry
- D2W µBump - imec R&D
- D2W µBump - industry

D2W= Die-to-wafer bonding
W2W= Wafer-to-Wafer bonding
HB= Hybrid bonding

imec

Introduction - D2W overlay

- Overlay requirements do not only depend on interconnect pitch, but also pad design
  - For imec 2µm pitch hybrid bonding test vehicle, <250nm overlay required for 100% pad contact

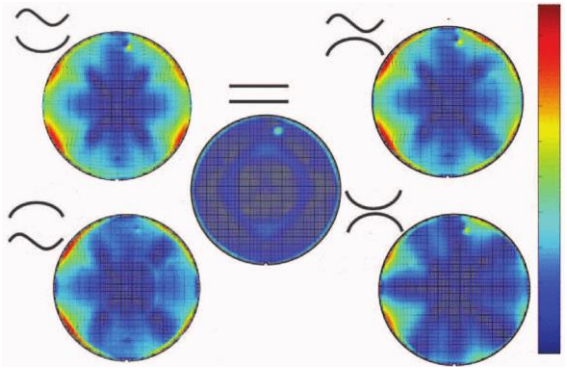
- 250 nm overlay is in line with state-of-the-art hybrid D2W bonding equipment alignment capability, **but….**
  - **Alignment capability ≠ post bond overlay**

- **Strong influence of process and material on overlay expected** (similar to W2W bonding)

TABLE I DESIGNS OF BOND PADS

Design	Pitch	Bond Pad Shape (yellow: top; blue: bottom)	Top Pad Size	Bottom Pad Size	Overlay Tolerance (full contact)	Overlay Tolerance (open)
A	2 µm		0.50 µm x 0.50 µm	1.00 µm x 1.00 µm	0.250 µm	0.750 µm
B	3 µm		0.75 µm x 0.75 µm	1.50 µm x 1.50 µm	0.375 µm	1.125 µm
C	3 µm		1.00 µm x 1.00 µm	1.50 µm x 1.50 µm	0.250 µm	1.250 µm
D	3 µm		2.14 µm x 0.50 µm	2.14 µm x 0.50 µm	0.820 µm	1.320 µm

Imec D2W test vehicle pad geometry designs

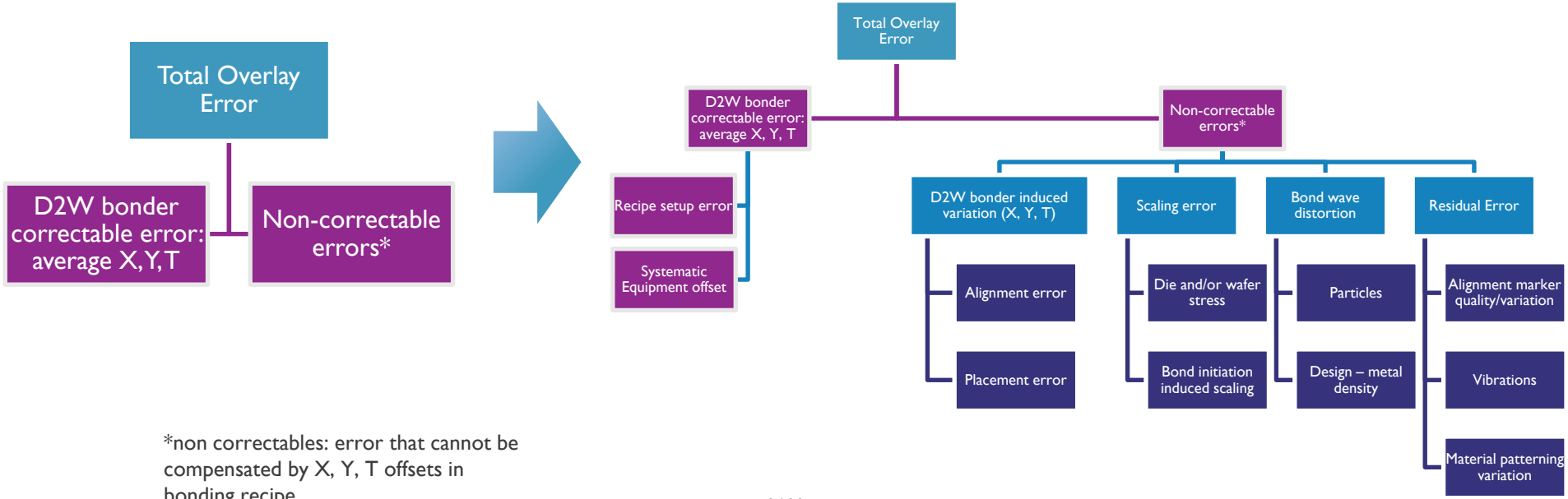


Overlay residual maps for W2W bonding with various wafer shape combinations

S. Iacovo et al., "A Study of SiCN Wafer-to-Wafer Bonding and Impact of Wafer Warpage," 2023 IEEE 73rd Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2023, pp. 1410-1417, doi: 10.1109/ECTC51909.2023.00241.

Introduction - D2W overlay

- To achieve best possible post-bond overlay error, **deeper understanding of the overlay error contributors** is required

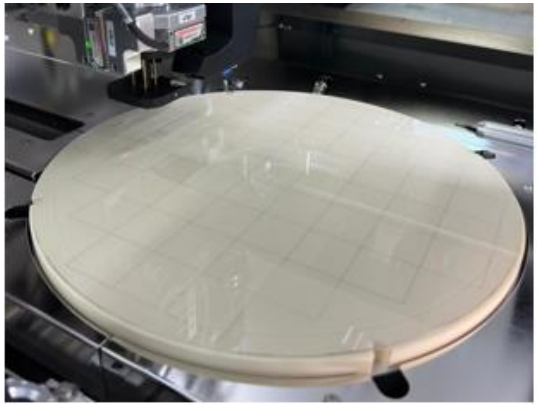


*non correctables: error that cannot be compensated by X, Y, T offsets in bonding recipe

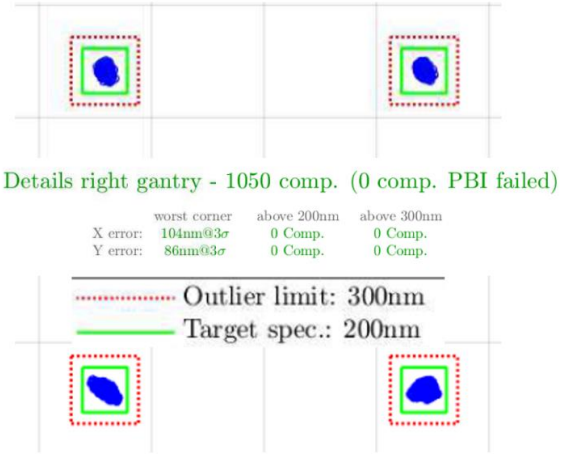
Machine Baseline Alignment Capability

- Hybrid bonding equipment: BESI Chameo*ultra plus*
- Glass-on-glass alignment test to assess **machine capability** (≠ process capability)
  - =Matrix Baseline Machine Capability test (MBMC)
  - No impact of material variations & process included
- → **Alignment capability well below 200nm @ 3s**

BESI Chameo*ultra plus*

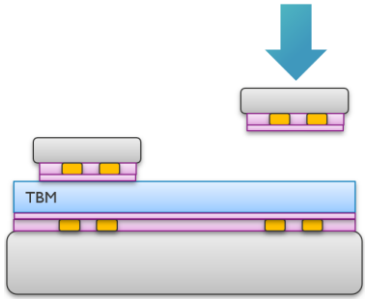


Glass substrate on wafer chuck during MBMC test

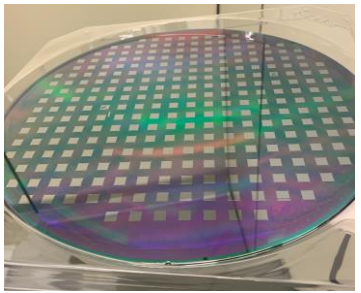


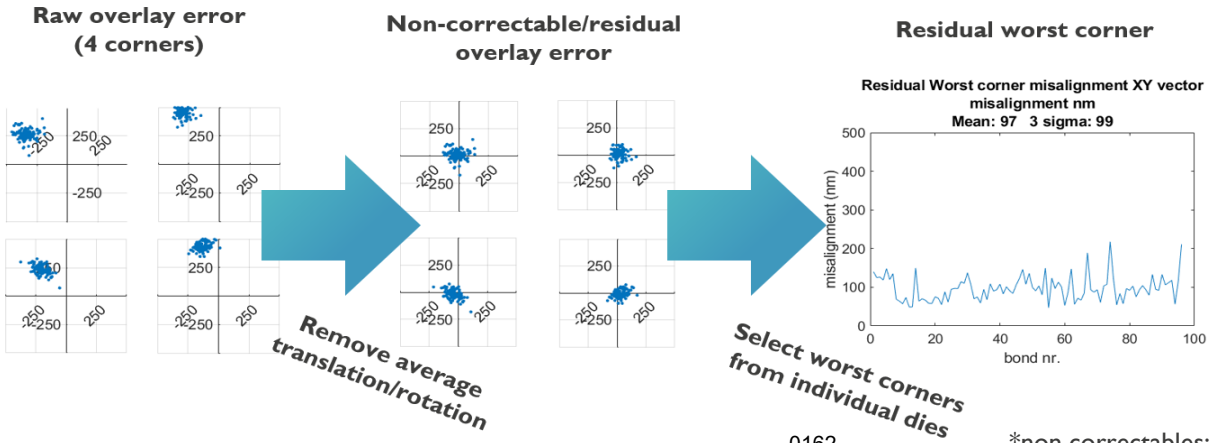
Example MBMC results of Chameo^{UltraPlus} in imec

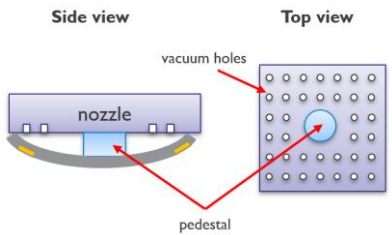
D2W bonding – adhesive coated wafers



- **Bonding on Temporary Bonding Material (TBM) coated wafer**
  - **→ avoid impact of particles/dielectric/hybrid bonding process**
- Overlay test vehicle
  - 7.2*7.2 mm, 50µm thin top dies
- D2W bonding in BESI Chameo*ultra plus*
- No overlay optimization, focus on residual errors!
- IR overlay measurements → **Good overlay results achieved (<200nm residual worst corner error)**



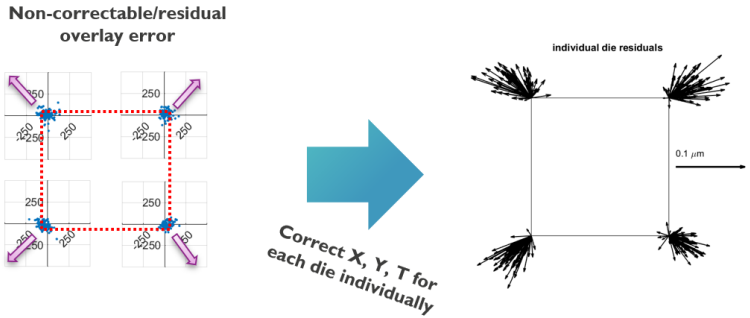


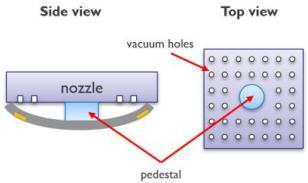


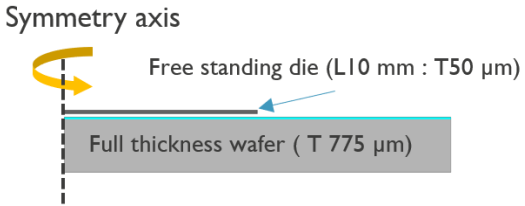
*non correctables: error that cannot be compensated by X, Y, T offsets in bonding recipe

D2W bonding – adhesive coated wafers

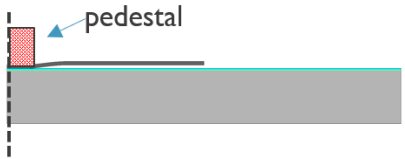
- **Scaling error of ~80nm in die corners** observed
  - Significant contributor to worst corner error!
- **FEM modeling** to explain observed scaling error







Step 1: Apply residual stress on dielectric layer



Step 2: Apply load with a pedestal in the center of the die

Step 3: Release vacuum - final bonding

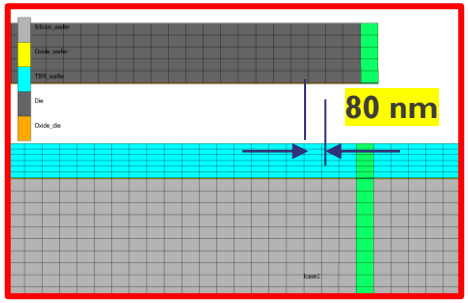
Modeling – TBM vs dielectric/hybrid bonding

- Before bonding, already 80nm scaling error top die versus landing wafer!
- Pedestal bending the die → **Tensile strain → additional scaling error**

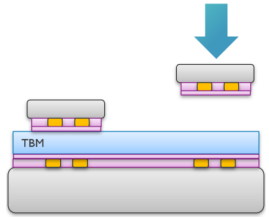
- **Adhesive/TBM bonding**
  - After release of vacuum, the soft TBM does not "hold" the deformation → die comes back to original stress/strain state
  - Final misalignment is only due to the dielectric layer in combination with difference in die and substrate thickness (~80 nm)

- **Dielectric/hybrid bonding**
  - After release of vacuum, the **strong SiCN/SiCN dielectric bond prevents the release of strains**
  - **Final misalignment is the SUM of dielectric + thickness induced differences and extra bending strain due to die deformation** (total error expected ~110 nm)

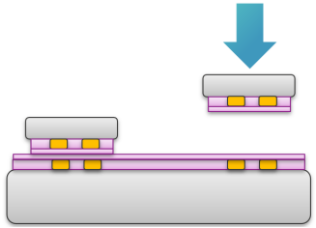
- **→ Initial modeling shows impact of dielectric stress and bonding nozzle on scaling error**
  - → Further work to be done to finetune model



Misalignment due to dielectric layer in combination with differences in Si thickness



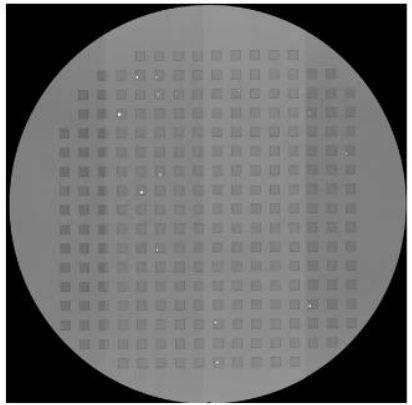
TBM/adhesive based bonding

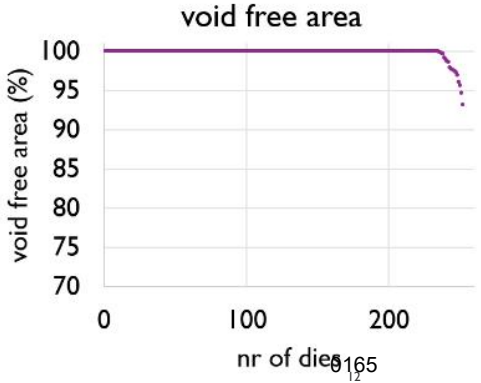


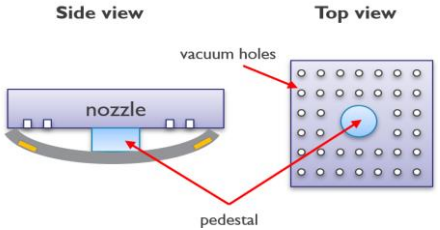
Dielectric/hybrid bonding

D2W dielectric bonding experiments

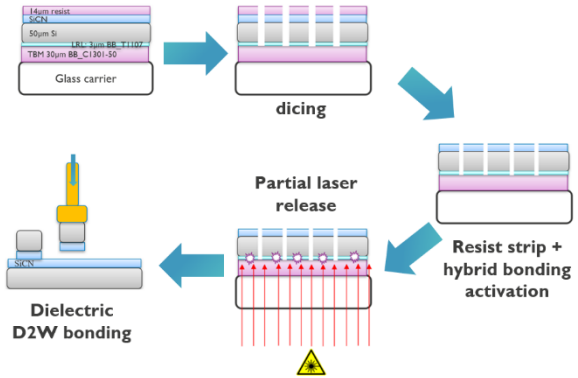
- **SiCN** based dielectric bonding
  - No Cu exposed, avoid influence of Cu patterning on bonding performance
- D2W bonding in **BESI Chameo**$^{ultra\ plus}$
  - No "global" overlay optimization performed
  - → **focus on residual errors & repeatability**
- **Pedestal nozzle** – ensure die center bond initiation
- SAM: good voiding yield







Pedestal nozzle tooling



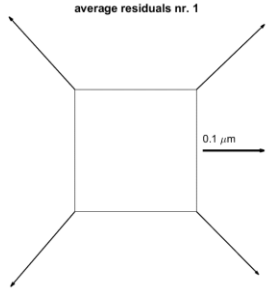
Imec dielectric/hybrid D2W process flow

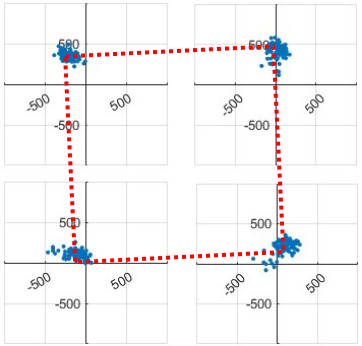
P. Bex, A. Phommahaxay, K. Kennes, S. Suhard, S. Brems and E. Beyne, "Optimized Die Preparation and Handling for High Yield Hybrid Die to Wafer Bonding," in *IMAPS Symposium*, San Diego, 2023

D2W dielectric bonding: overlay results

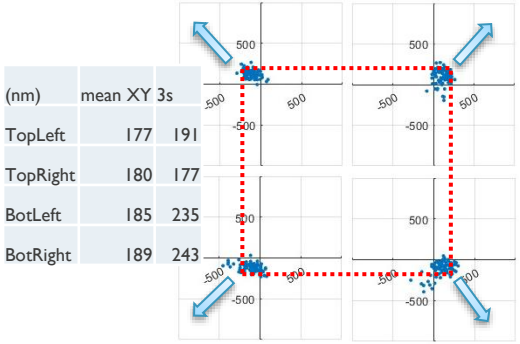
- 4 corner IR overlay measurements
  - **Good die-center placement precision**
- Clear scaling-like error visible
  - ~150 nm error vector in die corners
  - Strong contributor to worst corner error!
- **Scaling error has a significant impact on overlay in die corners!**
  - → to assess equipment performance, focus on die center X, Y, Theta, not worst corner accuracy!

Average scaling error

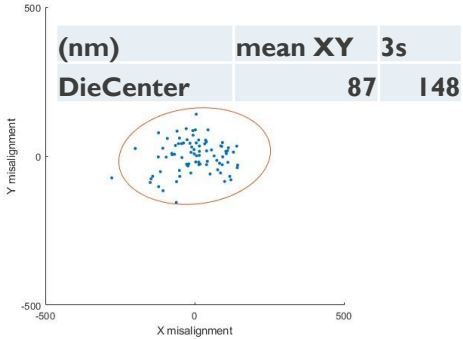




Raw overlay data – 4 corners



Residual data → correctables* removed



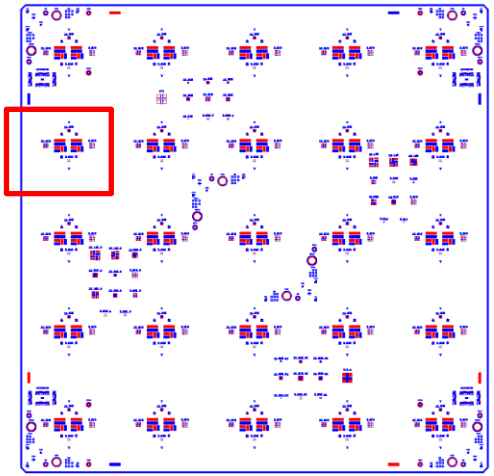
4 corner average: placement precision

* We here consider correctables as wafer average X, Y and rotation error

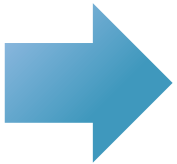
D2W dielectric bonding: intra-die overlay analysis

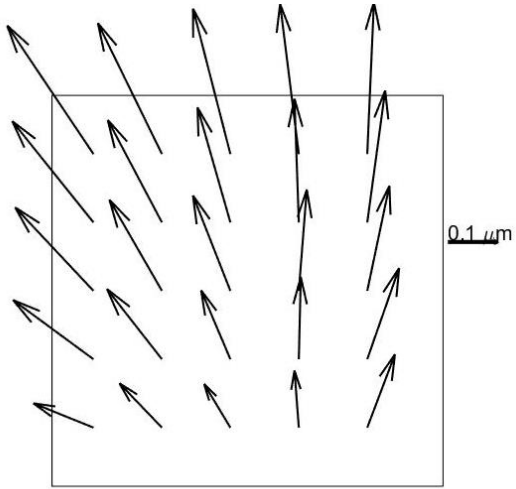
- To further investigate the scaling error, **more measurement points are required**
- imec overlay test vehicle contains **25 overlay marker cells per die**
- Measure all cells in all dies to allow more accurate, high resolution within-die overlay analysis

Standard cell



Overlay test vehicle layout

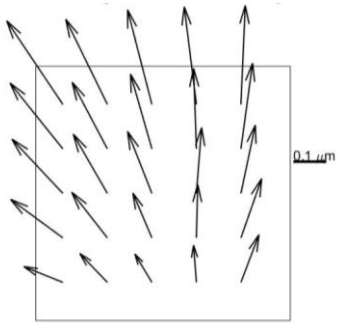




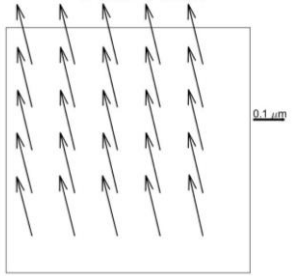
Intra-die overlay analysis

$$d_x = T_x - R_{xy}Y + S_{xy}X + res_x$$
$$d_y = T_y + R_{xy}X + S_{xy}Y + res_y$$

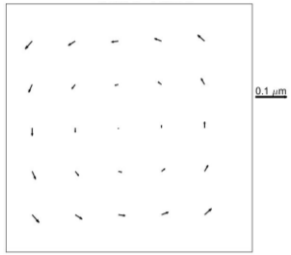
- Overlay analysis per die with **4 parameter overlay model**
  - simplified version of classic 6-parameter lithography overlay model
  - → misalignment is sum of Translation (X & Y), Rotation, Scaling and residual error
- After removing the D2W bonder correctable parameters (translation and rotation): **scaling** pattern confirmed



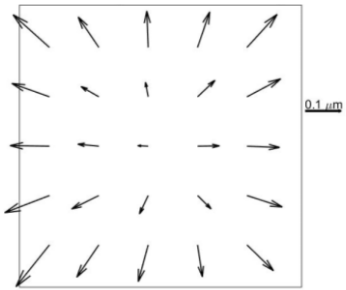
Raw overlay data (d)



- Translation error (T)



- Rotation error (R)

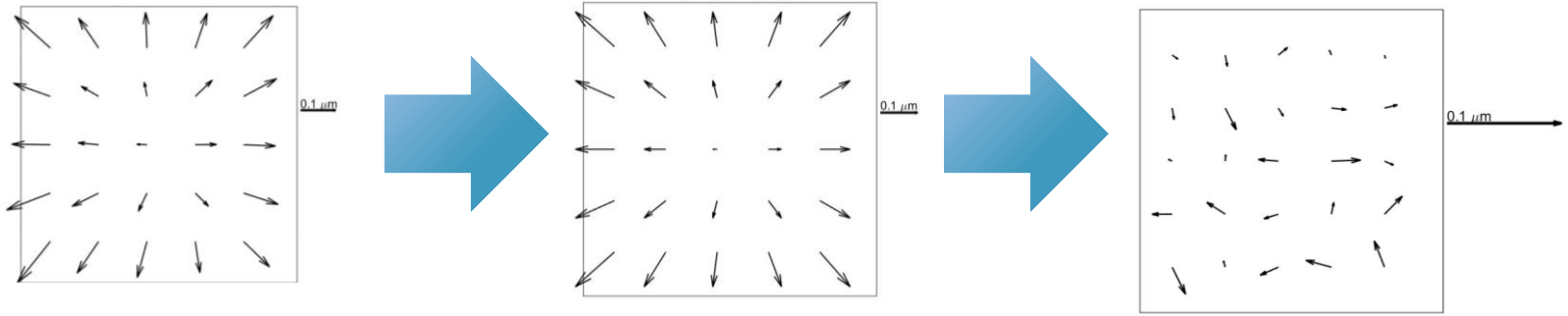


Linear scaling + residual error (S + res)

$$d_x = \cancel{T_x} - \cancel{R_{xy}}Y + S_{xy}X + res_x$$
$$d_y = \cancel{T_y} + \cancel{R_{xy}}X + S_{xy}Y + res_y$$

Intra-die overlay analysis

- After removing **linear** scaling component (~34 ppm) – very small residual error observed
  - Metrology, distortion,…
- **Linear scaling error reduction → significant impact on D2W overlay expected**
  - Die stress compensation
  - **Alternative bonding nozzle(s)**



Linear scaling + residual error (S+ res)

- Linear scaling error (S)

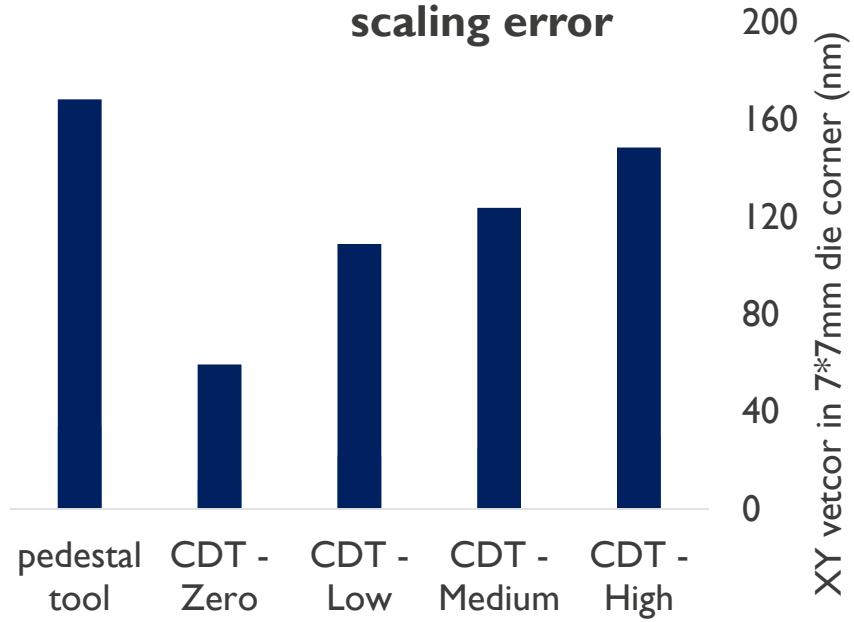
Residual error (res)

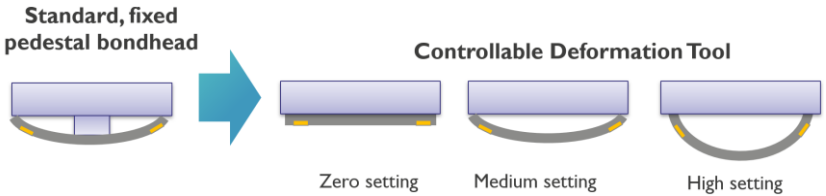
$$d_x = T_x - R_{xy}Y + S_{xy}X + res_x$$
$$d_y = T_y + R_{xy}X + S_{xy}Y + res_y$$

Alternative bonding nozzle

- New bonding nozzle: **controllable die deformation tool nozzle (CDT)**
- CDT nozzle decreases the scaling error…

$$d_x = T_x - R_{xy}Y + \boldsymbol{S_{xy}X} + res_x$$
$$d_y = T_y + R_{xy}X + \boldsymbol{S_{xy}Y} + res_y$$

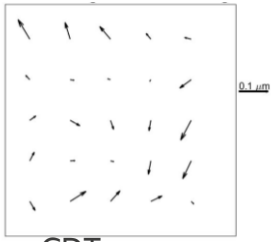




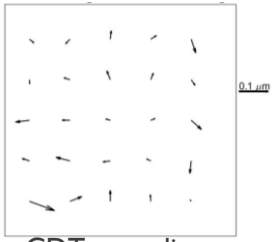
Alternative bonding nozzle

$$d_x = T_x - R_{xy}Y + S_{xy}X + \boldsymbol{res_x}$$
$$d_y = T_y + R_{xy}X + S_{xy}Y + \boldsymbol{res_y}$$

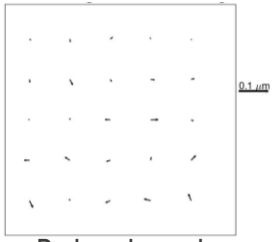
- But: **strong increase in residual error**
  - **Less control of bond wave propagation?**
  - Zero setting CDT (=flat tool)
    - chip touchdown in corner → rotation over die corner
    - Non-central bond wave initiation
- Outlook: reduce scaling error with:
  - **alternative/lower pedestal tool**
  - **stress compensation layers**



CDT - zero

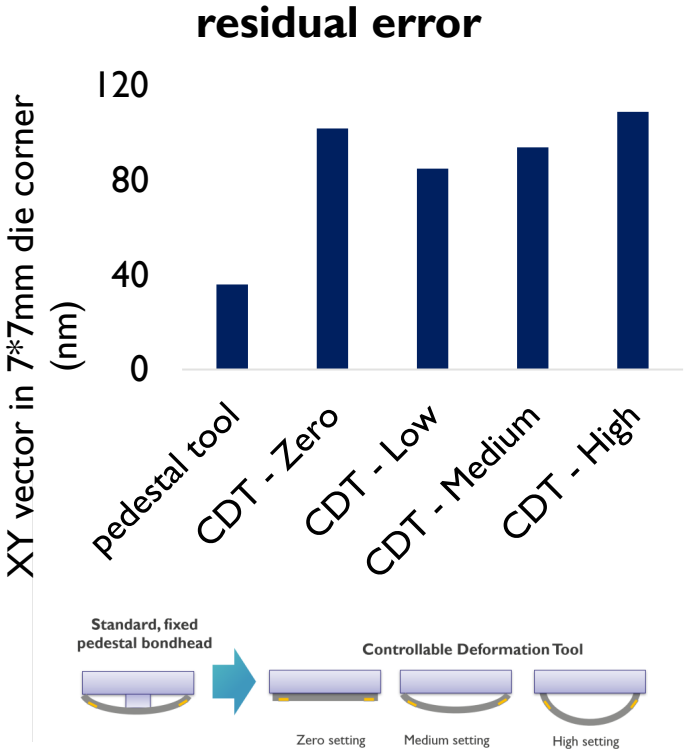


CDT - medium



Pedestal nozzle

residual error (res)



Conclusion & outlook

- **Conclusions**
  - Direct Dielectric D2W bonding
    - Good bonding yield, little voids
    - Good placement precision achieved
  - Large (linear) scaling error observed → strong contributor to worst corner error
  - Demonstration of high-resolution IR overlay measurements to analyze intra-die overlay
  - Die scaling overlay error mitigation options identified:
    - Alternative bonding nozzles
    - Compensating thin die stress

- **Outlook**
  - Alternative bonding nozzle exploration
  - Die stress compensation

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