The Mid-Atlantic Semiconductor Hub (MASH):
a distributed network of resources and talent to reassert U.S. leadership in semiconductor manufacturing

Daniel Lopez

Liang Professor of EE
Director Nanofabrication Lab
Materials Research Institute
Penn State University
dlopez@psu.edu

iNEMI: 5G/6G MAESTRO – Project Completed

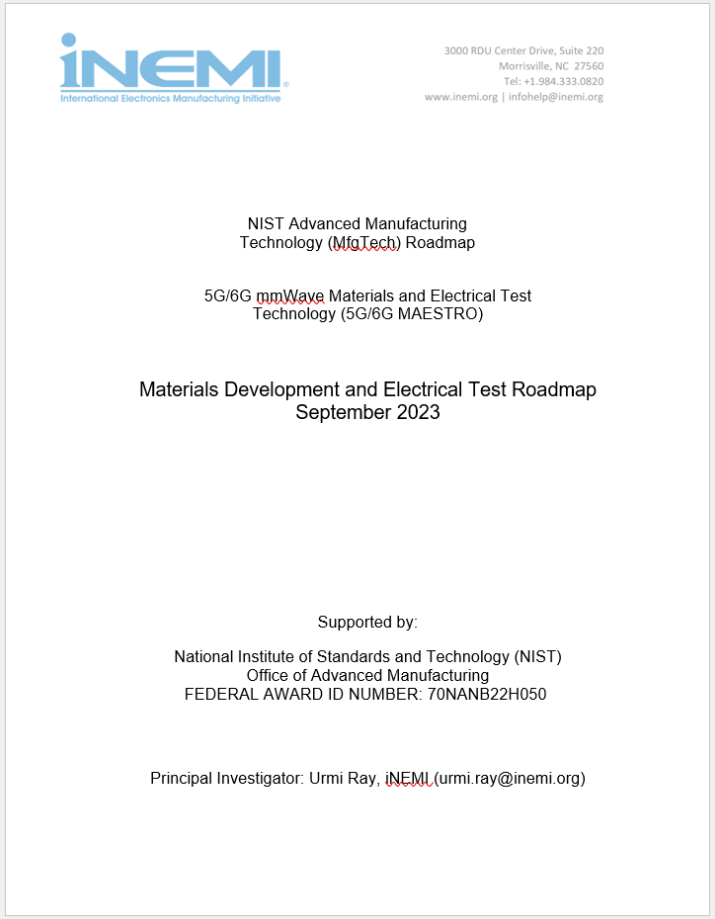
Project Duration: 1 May 2022 – 30 Sep 2023 (18 months)
Project Objective

Create a technology roadmap

- Develop a comprehensive **10-year hardware roadmap** for mmWave materials development & electrical characterization and testing.

Develop a U.S.-focused implementation strategy

- Recommend a U.S.-centric, cross-supply-chain consortium to execute the vision of the roadmap, the foundations for a **strong U.S. manufacturing ecosystem in RF materials and testing**.
- Promote the growth of a **strong and diverse U.S. workforce** in RF communication technologies, by proposing a plan of university curricula development and training.



iNEMI
International Electronics Manufacturing Initiative

3000 RDU Center Drive, Suite 220
Morrisville, NC 27560
Tel: +1.984.333.0820
www.inemi.org | infohelp@inemi.org

NIST Advanced Manufacturing
Technology (MfgTech) Roadmap

5G/6G mmWave Materials and Electrical Test
Technology (5G/6G MAESTRO)

Materials Development and Electrical Test Roadmap
September 2023

Supported by:

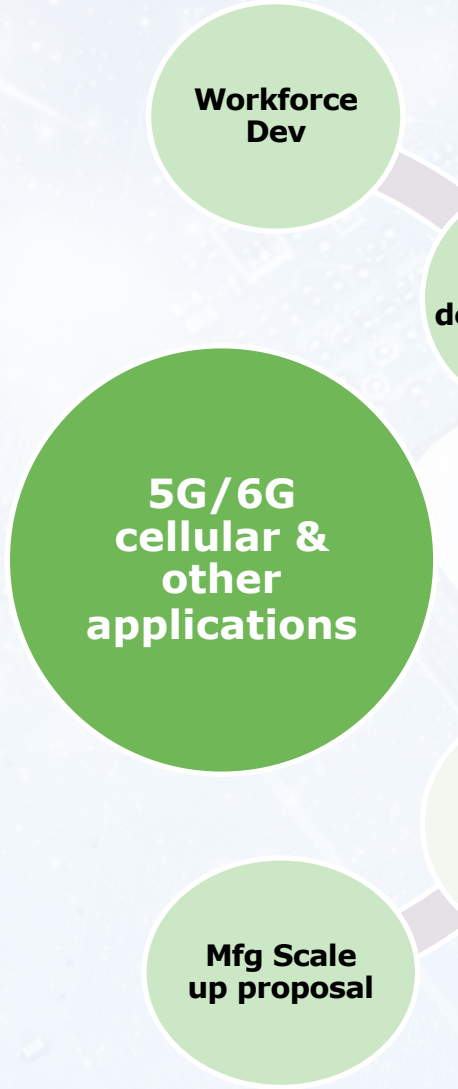
National Institute of Standards and Technology (NIST)
Office of Advanced Manufacturing
FEDERAL AWARD ID NUMBER: 70NANB22H050

Principal Investigator: Urmi Ray, iNEMI (urmi.ray@inemi.org)

5G/6G MAESTRO - iNEMI

https://www.inemi.org/maestro

5G/6G MAESTRO: Technology Scope



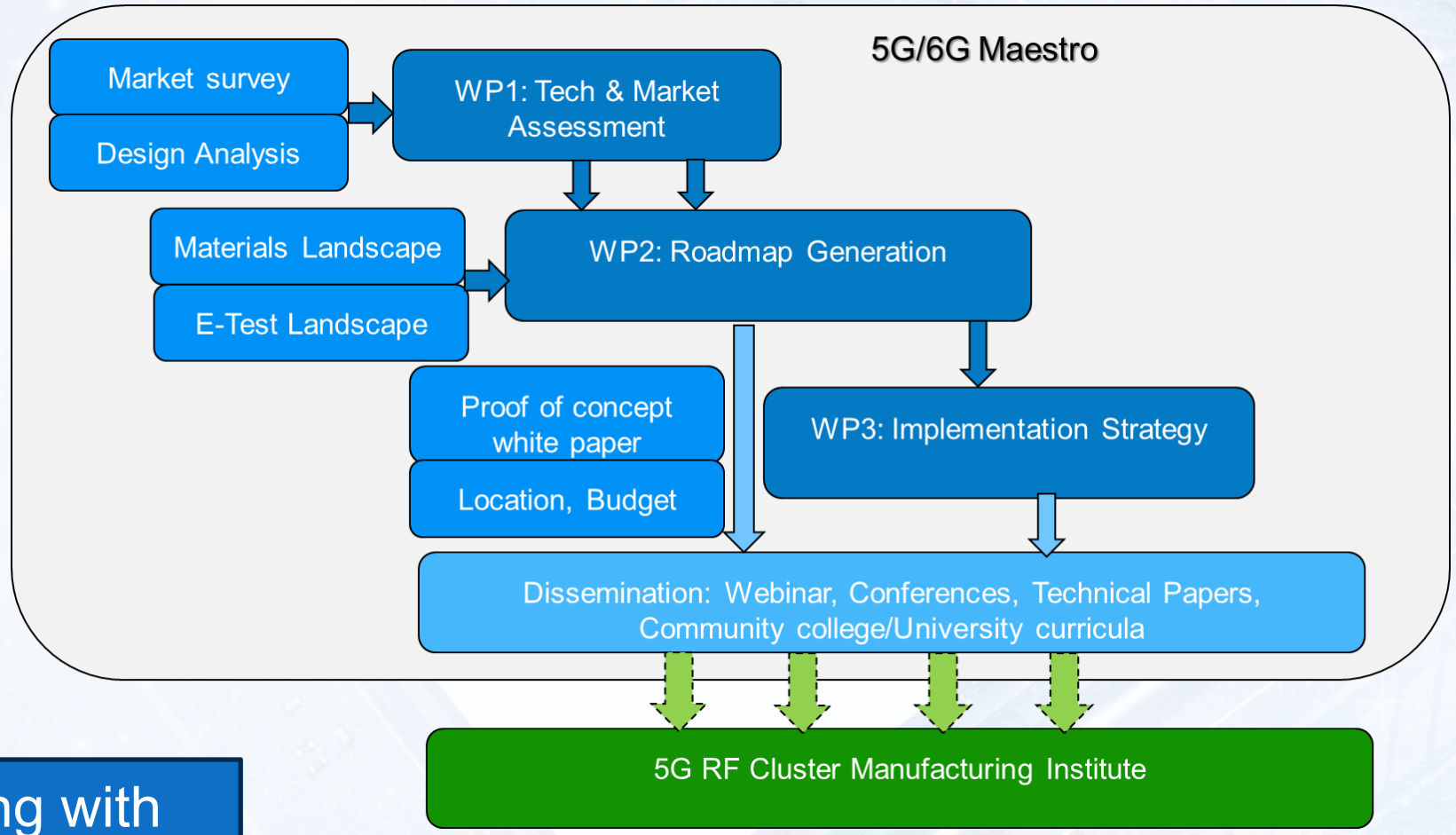
- mmWave frequency bands
- Roadmap materials to meet functional requirements on the loss tangent and dielectric constant
- Mechanical and thermal properties in scope
- Constraint: right cost-point & manufacturability at scale

- Identify techniques for repeatable fast low-loss material characterization
- Address lack of standard reference materials (SRM)
- Propose cross-industry approaches, enabling cross-supplier comparisons

- Transition from contact testing to over-the-air testing, particularly with pervasive use of massive MIMO at mmWave frequencies
- Consider changes in RF front-end packaging, including emergence of antenna-in-package technology
- Scaling up from lab-level testing to high-volume manufacturing environments

5G/6G MAESTRO - iNEMI

iNEMI 5G/6G MAESTRO: Project Flow



Partnering with MASH

https://mash-semiconductors.org/

Mid-Atlantic Semiconductor Hub genesis

Coalition of top universities and industries that will **combine resources and expertise** to meet the need of semiconductor industry in the US by strengthening and aligning **R&D, manufacturing, and workforce development**.

Our region is rich in many components of the manufacturing supply chain

- Digital twins for advancing semiconductor processes
- Materials and materials integration
- Semiconductor equipment manufacture
- Power components and module power delivery
- Precision instruments for fabrication and metrology
- Hardware and software security
- Packaging and Prototyping equipment
- Reliability and Systems
- Workforce development across the USA

Distributed network of resources and expertise

MASH distributed network of resources & expertise

Founding Universities

Enabling Universities

ASU

STEVENS INSTITUTE OF TECHNOLOGY 1870

Drexel

CUNY THE CITY UNIVERSITY OF NEW YORK

LEHIGH UNIVERSITY

WVU

CORNELL UNIVERSITY FOUNDED A.D. 1865

More than 500 tools for nanofabrication and characterization

↓

- **Redundancy**
- **Accessibility**

Access to many industrial facilities and advanced prototyping equipment

Industry-led workshops

How our combined research, educational activities and resources would be helpful to support and enhance the future of US semiconductor research and manufacturing?

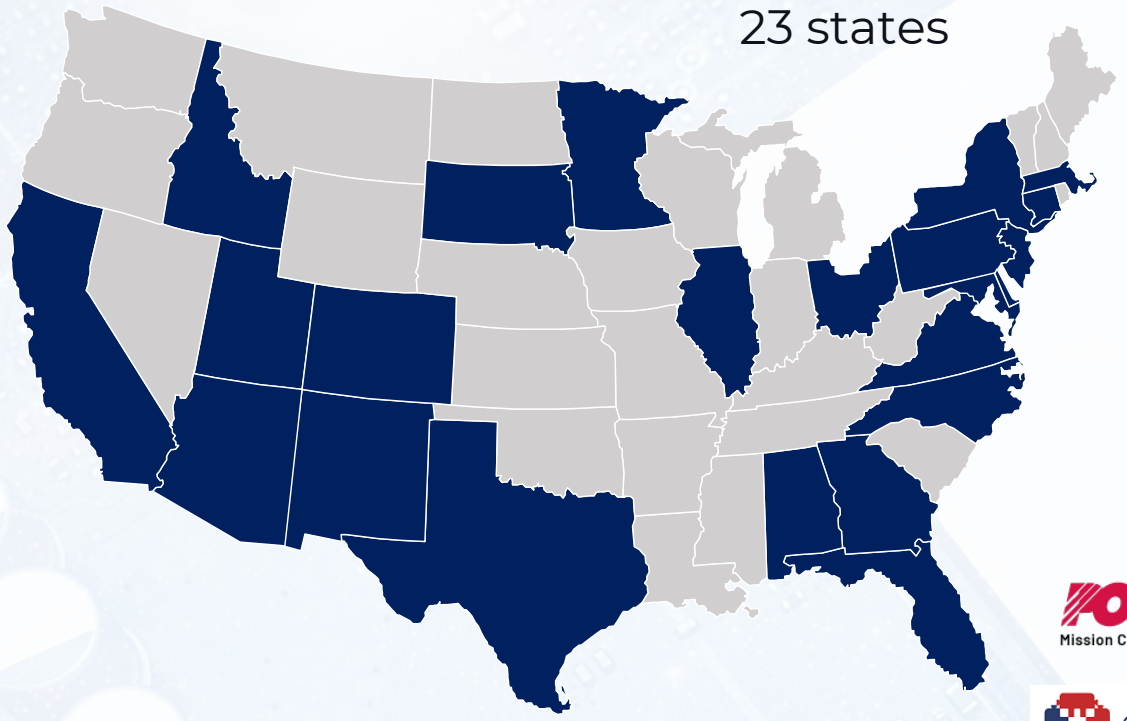
MASH Winter 2023 workshop
Philadelphia
January 11, 2023

MASH Spring 2023 workshop
State College
May 22-23, 2023

MASH Winter 2024workshop
State College
January 16-17, 2024

Industrial Engagement

- Engaged more than 160 companies to work with MASH.
- Created an ***Industrial Working Group*** to identify their technical and WFD needs.
- **Request for Information** survey to the industry to collect feedback on technical and WFD needs.



SCHOTT glass made of ideas
3D GS A New Dimension for Electronics
LASER THERMAL
BROADCOM
BOEING
Infinera
Kurt J. Lesker Company
DREAM PHOTONICS
Goeppert accelerating science
HORIBA
DISCO
SUNRAY SCIENTIFIC
NOKIA Bell Labs
ClassOne TECHNOLOGY
MOXTEK
MOSAIC microsystems
Texas Instruments
Morgan Advanced Materials
SIEMENS
ANSYS
Greene Tweed
BRUKER
euclid TECHLABS
Kulicke & Soffa
POWEREX Mission Critical Power Electronics
muRata INNOVATOR IN ELECTRONICS
Plasma-Therm
Lam RESEARCH
CORNING
FREE FORM FIBERS
NORTHROP GRUMMAN
Raytheon Technologies
IBM
menlomicro
imec
onsemi
KEYSIGHT TECHNOLOGIES

MASH Mid-Atlantic SEMICONDUCTOR HUB
PennState Penn Carnegie Mellon University University of Maryland NYU University of the District of Columbia University of Delaware Princeton University Boston University Columbia

Industry-led workshops

The **MASH "distributed" network of facilities and cloud of expertise** will support technology transition to manufacturing and offer redundancy of resources. MASH will give access to one of the world's largest nanofabrication, packaging, and characterization facility by linking and enhancing the facilities in the hub.

MASH will focus on helping the semiconductor industry to transition **Materials into Systems:** advanced communications, non-volatile memory, More than Moore devices, IIoT , Artificial Intelligence, edge computing, wireless communications, quantum devices, environmental sustainability, and materials and substrates.

MASH activities will center around three cross-cutting areas:

- **Si-adjacent technologies,**
- **Advanced packaging,**
- **Digital Twins & AI for semiconductor processes**.

MASH will develop skills-based **educational and workforce development** plans to attract people to the field, provide companies with an agile system to meet staffing requirements, and at the same time, enhance racial and socioeconomic diversity.

What problems might MASH solve

Si-adjacent materials

- **SiC foundry**

→ Josh Robinson (PSU)
Adri Van Duin (PSU)
Suzanne Mohney (PSU)

- **Ferroelectric and Piezoelectric manufacturing capabilities** → Susan Trolier-McKinstry (PSU)
Gianluca Piazza (CMU)
Troy Olsson (UPenn)

- **Diamond manufacturing capabilities** → Nathalie de Leon (Princeton)
Alastair Stacey (PPPL)
David Graves (PPPL)
Josh Robinson (PSU)

What problems might MASH solve

Si-adjacent materials

- **SiC foundry**

→ Josh Robinson (PSU)
Adri Van Duin (PSU)
Suzanne Mohney (PSU)

- **Ferroelectric and Piezoelectric manufacturing capabilities** → Susan Trolier-McKinstry (PSU)
Gianluca Piazza (CMU)
Troy Olsson (UPenn)

- **Diamond manufacturing capabilities** → Nathalie de Leon (Princeton)
Alastair Stacey (PPPL)
David Graves (PPPL)
Josh Robinson (PSU)

Advanced Packaging

- **Glass Core substrates** → John Mauro (PSU)
Mike Lanagan (PSU)
Madhavan Swaminathan (PSU)
- **High-throughput glass structuring** → Colin Schmucker (SCHOTT)
- **Scaling of TGV** → Andrew Ketterson (Qorvo)
- **Low loss materials for ultra high-performance photonics** → Michal Lipson (CU)
Keren Bergman (CU)
Alexander Gaeta (CU)
- **Substrates for low loss RF & photonic signal routing; packaging for mmWave structures** → Jeff Fitzgerald (BAE Systems)
- **Quantum packaging** → J. Herbsommer (TI)
Huascar Ascarrunz (Freq Elect)
Daniel Lopez (PSU)

What problems might MASH solve

Si-adjacent materials

- **SiC foundry**

→ Josh Robinson (PSU)
Adri Van Duin (PSU)
Suzanne Mohney (PSU)

- **Ferroelectric and Piezoelectric manufacturing capabilities** → Susan Trolier-McKinstry (PSU)
Gianluca Piazza (CMU)
Troy Olsson (UPenn)

- **Diamond manufacturing capabilities** → Nathalie de Leon (Princeton)
Alastair Stacey (PPPL)
David Graves (PPPL)
Josh Robinson (PSU)

Advanced Packaging

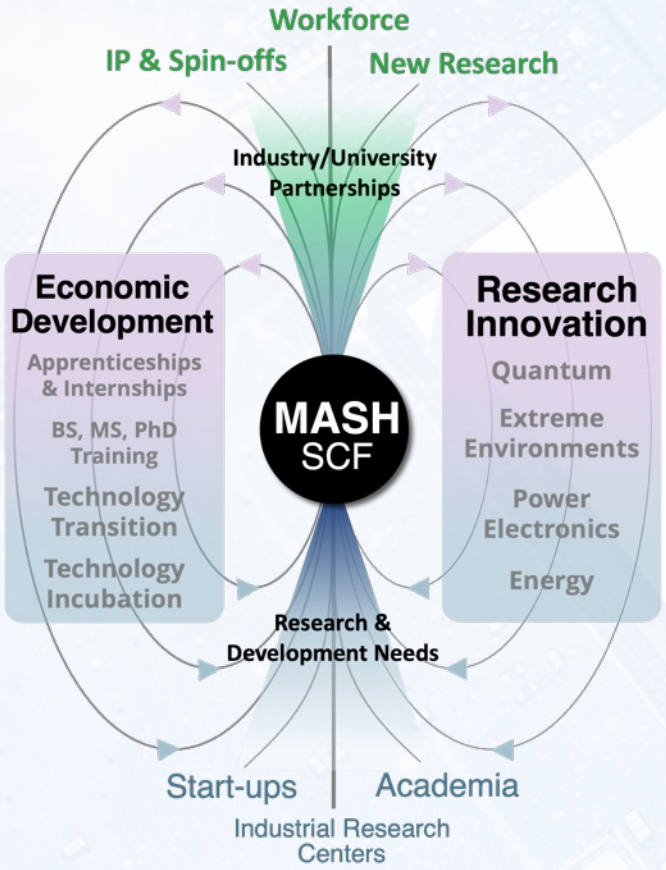
- **Glass Core substrates** → John Mauro (PSU)
Mike Lanagan (PSU)
Madhavan Swaminathan (PSU)
- **High-throughput glass structuring** → Colin Schmucker (SCHOTT)
- **Scaling of TGV** → Andrew Ketterson (Qorvo)
- **Low loss materials for ultra high-performance photonics** → Michal Lipson (CU)
Keren Bergman (CU)
Alexander Gaeta (CU)
- **Substrates for low loss RF & photonic signal routing; packaging for mmWave structures** → Jeff Fitzgerald (BAE Systems)
- **Quantum packaging** → J. Herbsommer (TI)
Huascar Ascarrunz (Freq Elect)
Daniel Lopez (PSU)

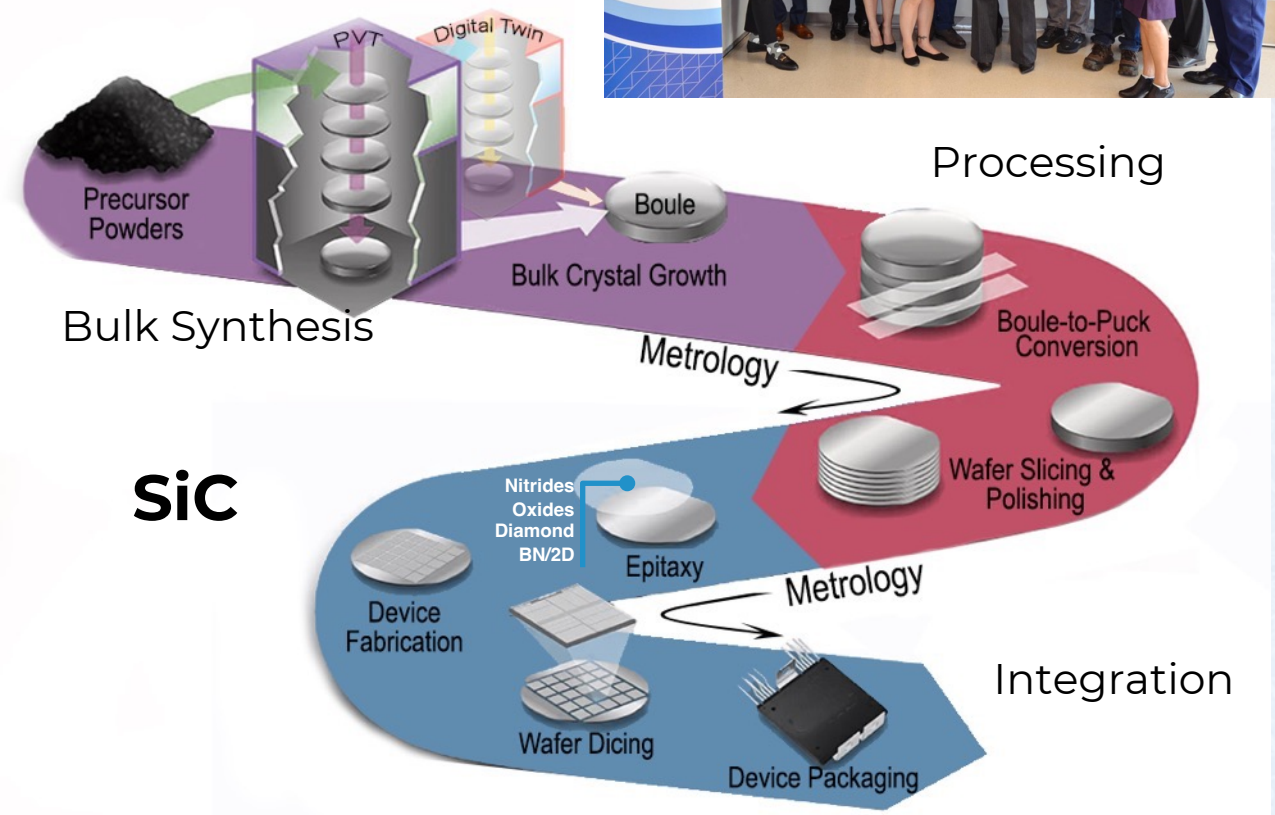
Digital Twins & AI for semiconductor processes

- How products perform in the field?
- Large scale simulation of manufacturing processes
- Large scale simulations of materials synthesis
- How to collect large metrology data and perform software analysis?
- **Digital twins for packaging?**
- Accelerate the engineering of new materials.
- Multi-physics tools for thermal budget
- **PDK for packaging**
- Hardware security

Semiconductor Crystal Foundry

Lead University: PSU (Josh Robinson, Susan Trolier-McKinstry)
Partner Universities: UPenn, CMU, Princeton, Columbia, U Delaware

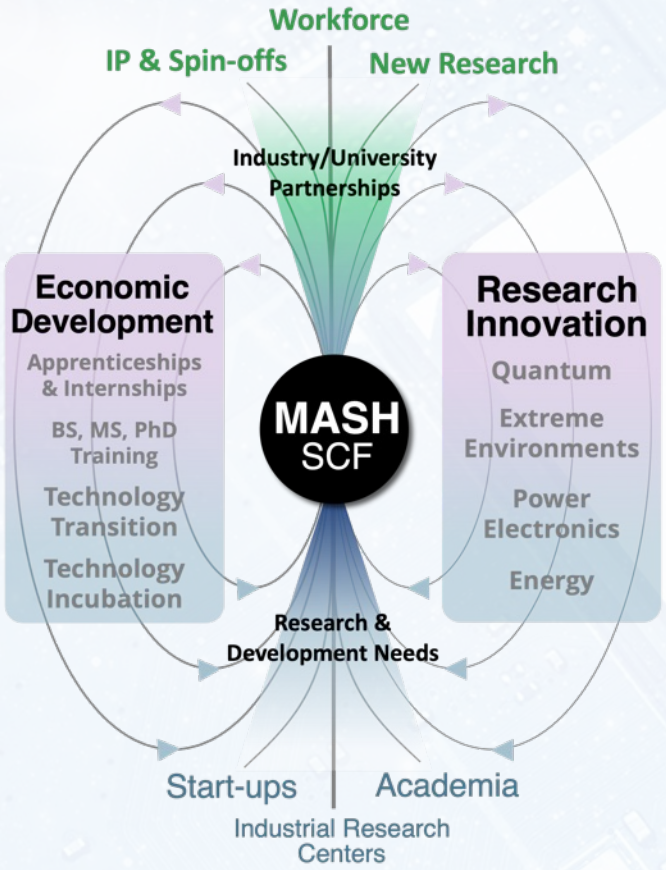




Onsemi, Coherent, Qorvo, PowerEx,...

Semiconductor Crystal Foundry

Lead University: PSU (Josh Robinson, Susan Trolier-McKinstry)
Partner Universities: UPenn, CMU, Princeton, Columbia, U Delaware



Ferroelectric and Piezoelectric manufacturing capabilities

- FRAM
- Fe-CAP
- MEMS

Diamond manufacturing capabilities

- Power electronics
- Quantum sensors
- Extreme environments

Digital Twins and AI for manufacturing

Lead University: CMU (Gary Fedder)
Partner Universities: BU, Columbia, NYU, UPenn, PSU

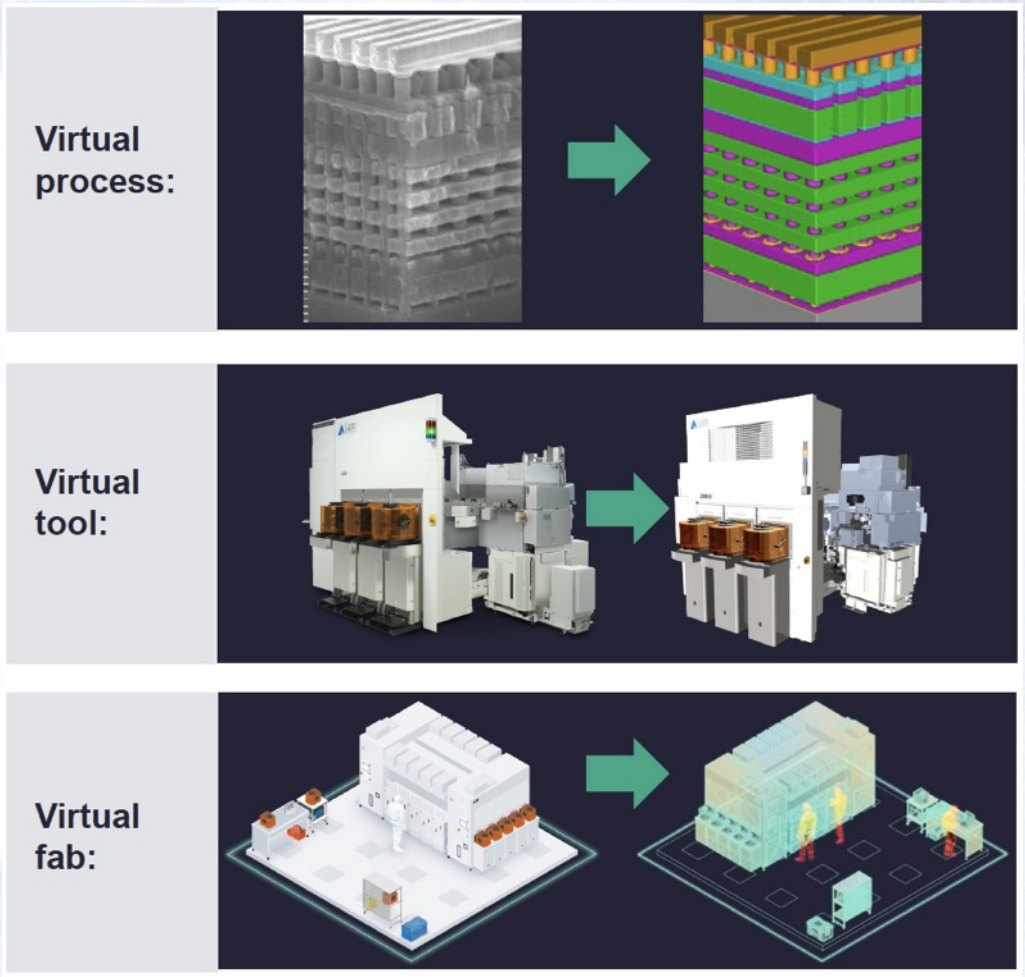
Carnegie Mellon University

NYU

PennState

BOSTON UNIVERSITY

Penn
University of Pennsylvania



Courtesy of Rick Gottscho & David Fried (Lam Research)

Engineering

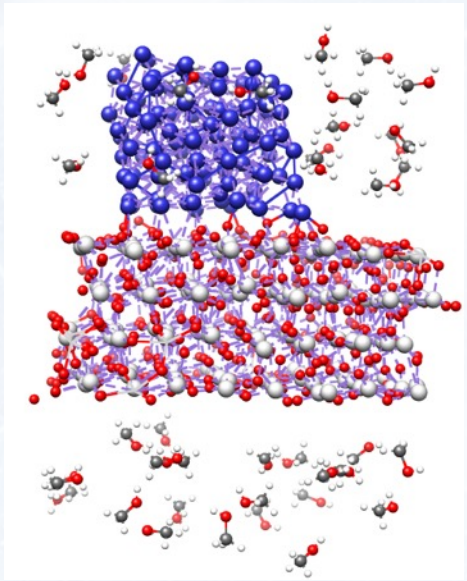
Human–AI team halves cost of chip-design step

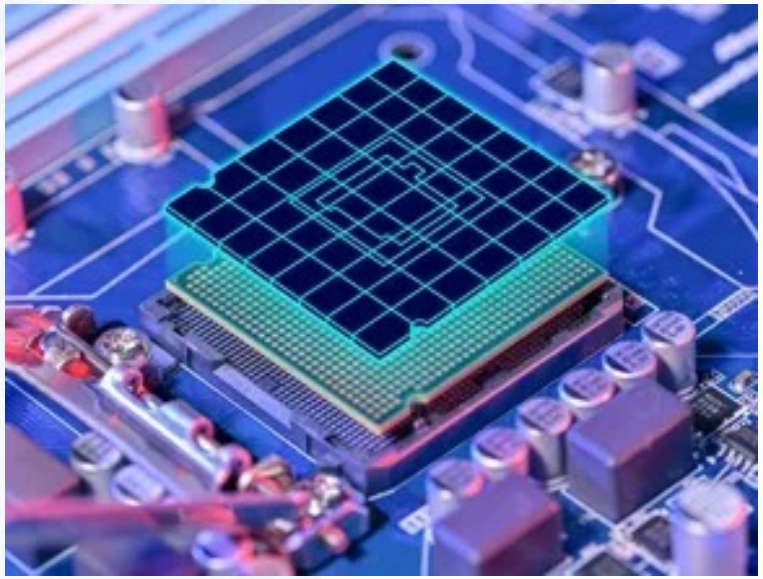
Ying-Lang Wang & Mao-Chih Huang

Engineers and algorithms have competed in a virtual test to design a step in the process of manufacturing computer chips. Pairing human expertise with computational efficiency proves most cost-effective, but only when the timing is right. **See p.707**

Digital Twins and AI for manufacturing

Lead University: CMU (Gary Fedder)
Partner Universities: BU, Columbia, NYU, UPenn, PSU





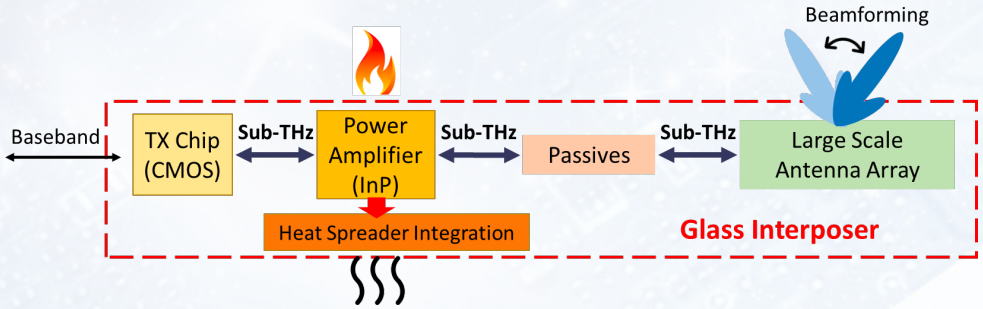
Materials growth
SiC & GaN
Ferro and Piezo
Diamond

Devices
CMOS
Photonics
MEMS

Facilities & equipment
Cleanrooms
Manufacturing equipment
Packaging tools

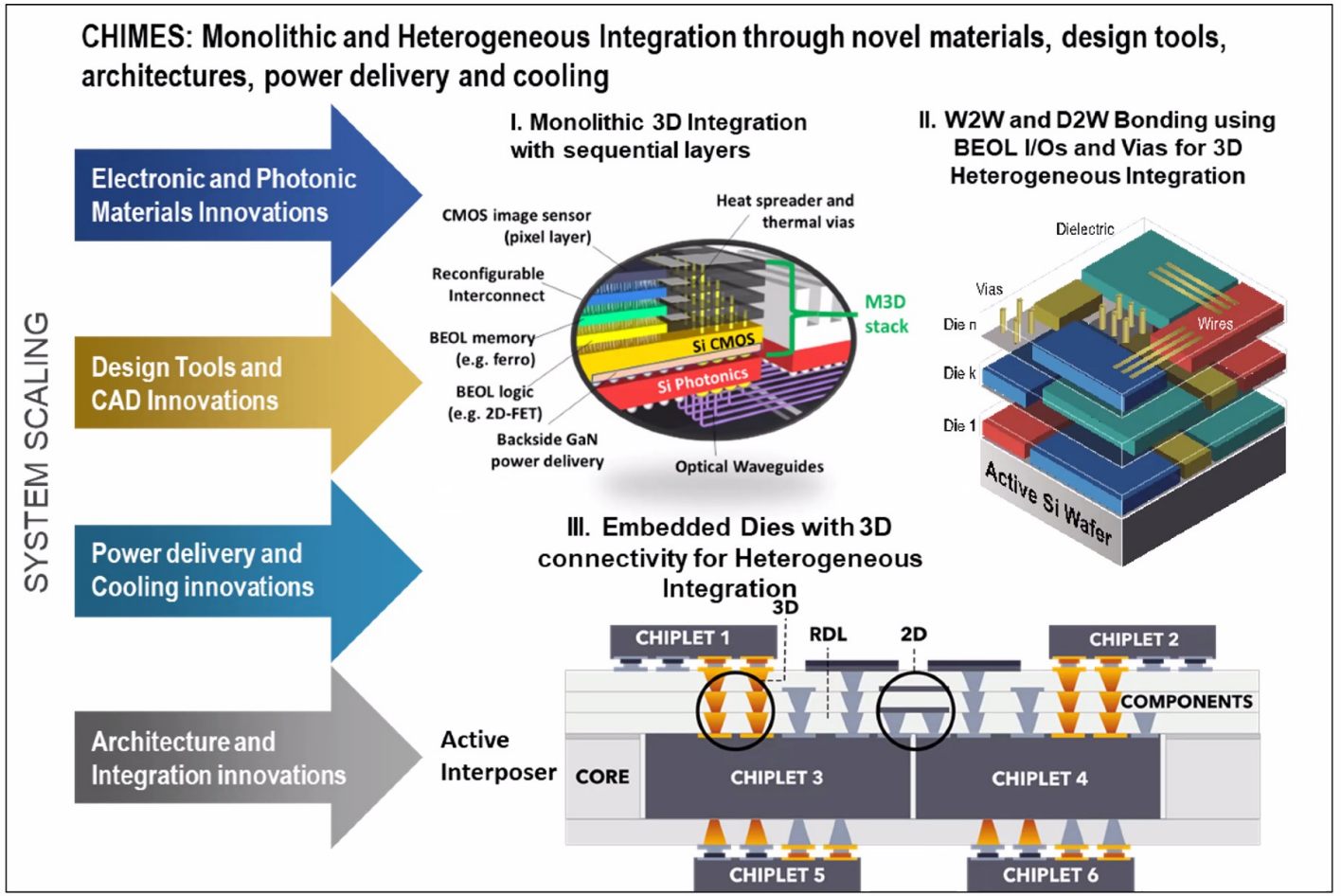
Workforce development

Advanced Packaging



Prof. Madhavan Swaminathan

CHIMES – VISION



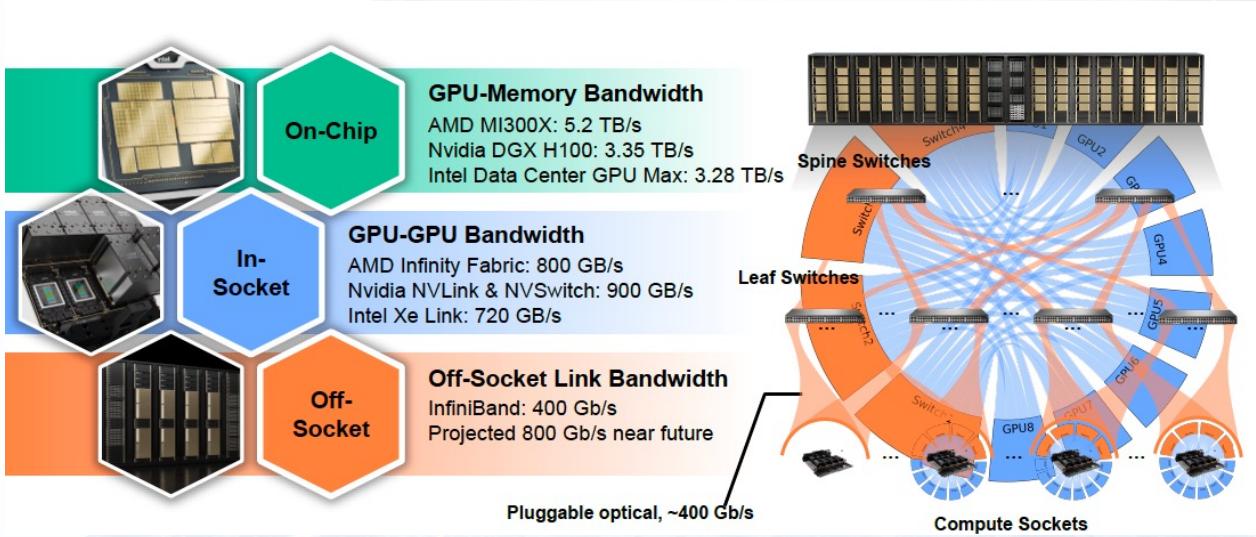
Center for Heterogeneous Integration of Micro Electronic Systems

Advanced Packaging

Lead University: PSU (Madhavan Swaminathan), Keren Bergman (Columbia)
Partner Universities: NYU, Columbia, Princeton, U Maryland

CUbiC
Center for Ubiquitous Connectivity

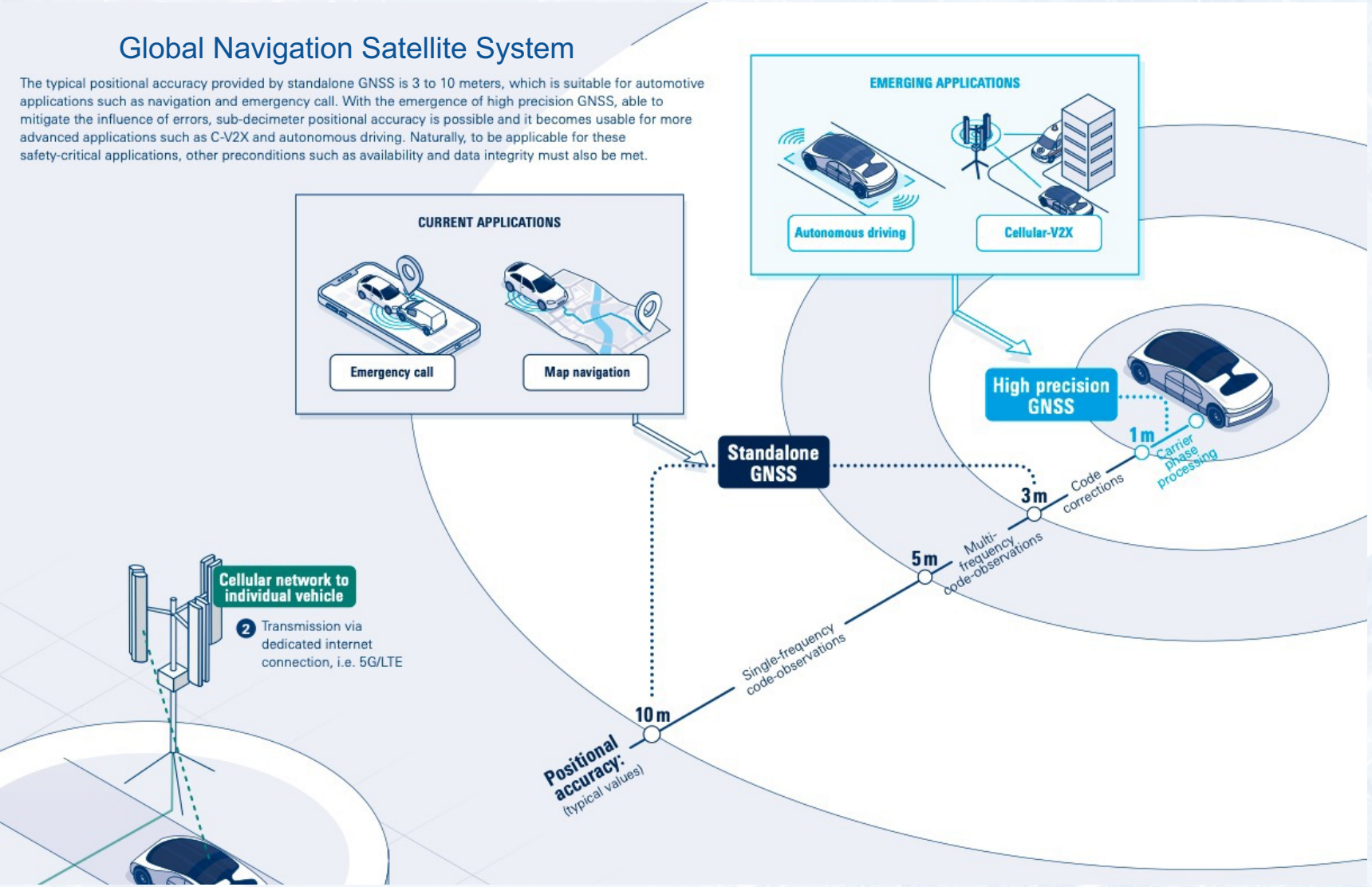
Keren Bergman
Charles Batchelor Professor of Electrical Engineering;
Dept of Electrical Engineering, Columbia University



Advanced Packaging

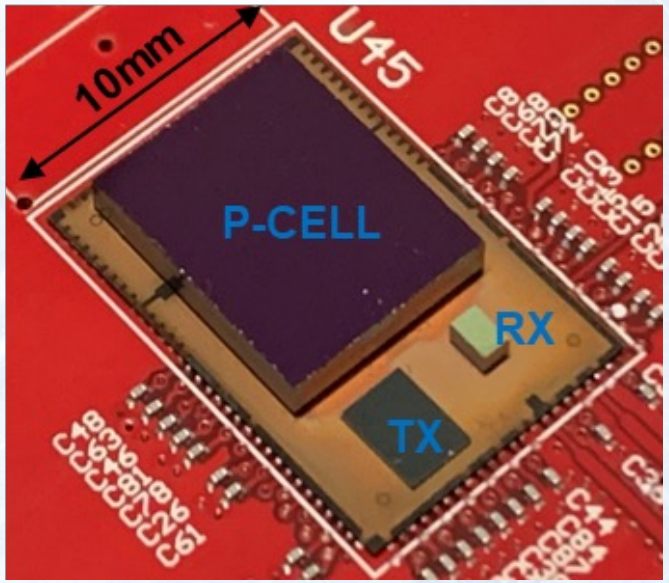
Global Navigation Satellite System

The typical positional accuracy provided by standalone GNSS is 3 to 10 meters, which is suitable for automotive applications such as navigation and emergency call. With the emergence of high precision GNSS, able to mitigate the influence of errors, sub-decimeter positional accuracy is possible and it becomes usable for more advanced applications such as C-V2X and autonomous driving. Naturally, to be applicable for these safety-critical applications, other preconditions such as availability and data integrity must also be met.



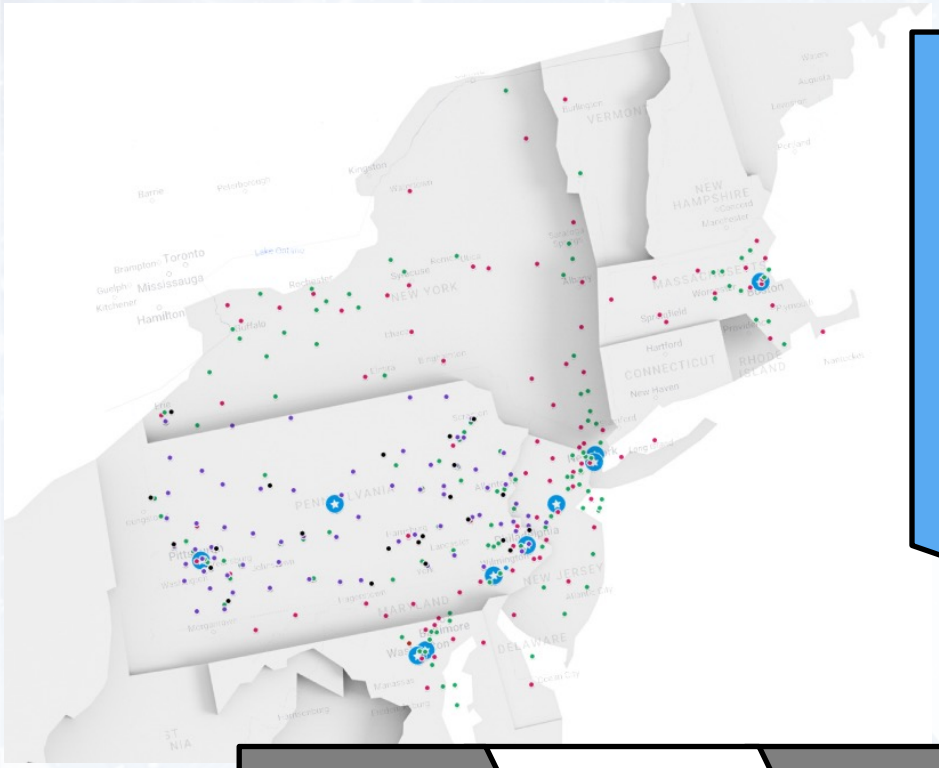
Texas Instruments

Sensitivity/stability augmentation through Integrated Quantum Sensors



From $5000 to $50?

Workforce Development



60M
residents

Workforce Development Corridor

- Digital twins for advancing semiconductor processes
- Materials and materials integration
- Semiconductor equipment manufacture
- Power components and module power delivery
- Precision instruments for fabrication and metrology
- Hardware and software security
- Packaging and Prototyping equipment
- Reliability and Systems
- Workforce development across the USA

12k K12 institutions

9M K12 students

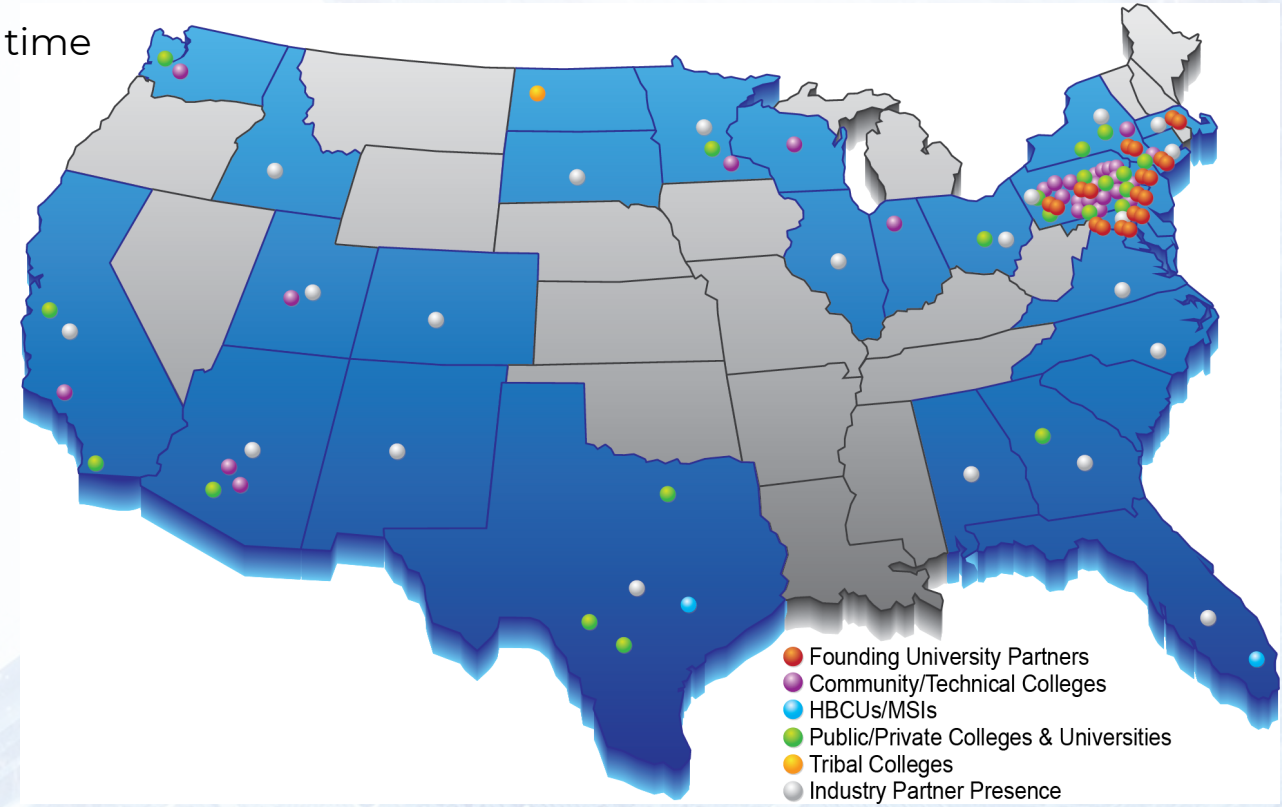
500 colleges & universities

2.4M undergraduates

Workforce Pipeline

Workforce Development across MASH

- Core group for WFD coordination across MASH:
  - community colleges, HBCUs, MSIs, unions, Veteran/Military organizations.
- **WFD asset mapping** conducted across MASH participating universities and partners.
  - training the currently available individuals in the workforce
  - establishing pipelines through k12 and higher Ed as a sustainable future
  - ensuring that the diversity of the work force grows over time
  - reskilling in the age of Artificial Intelligence



MASH and the CHIPS Act

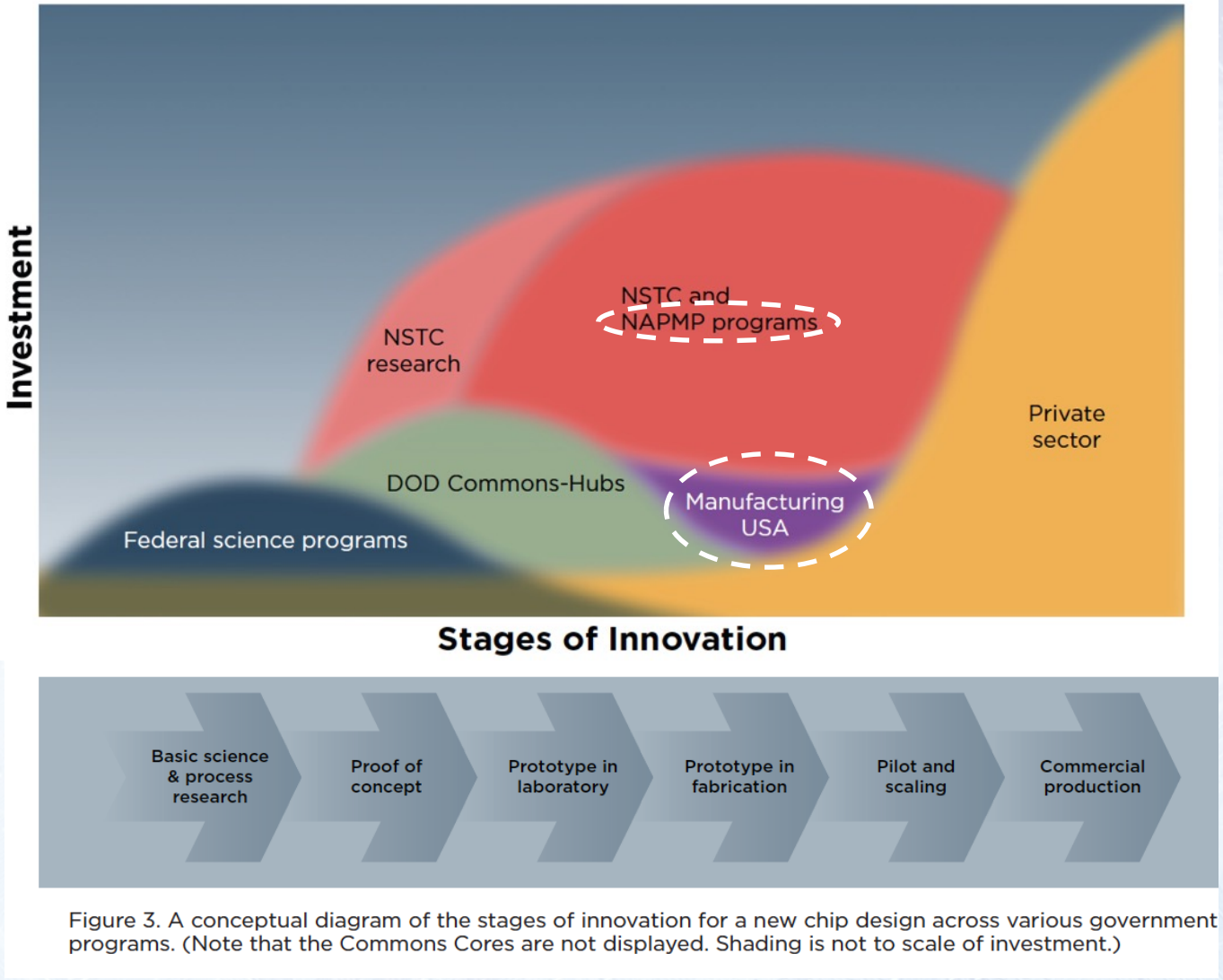
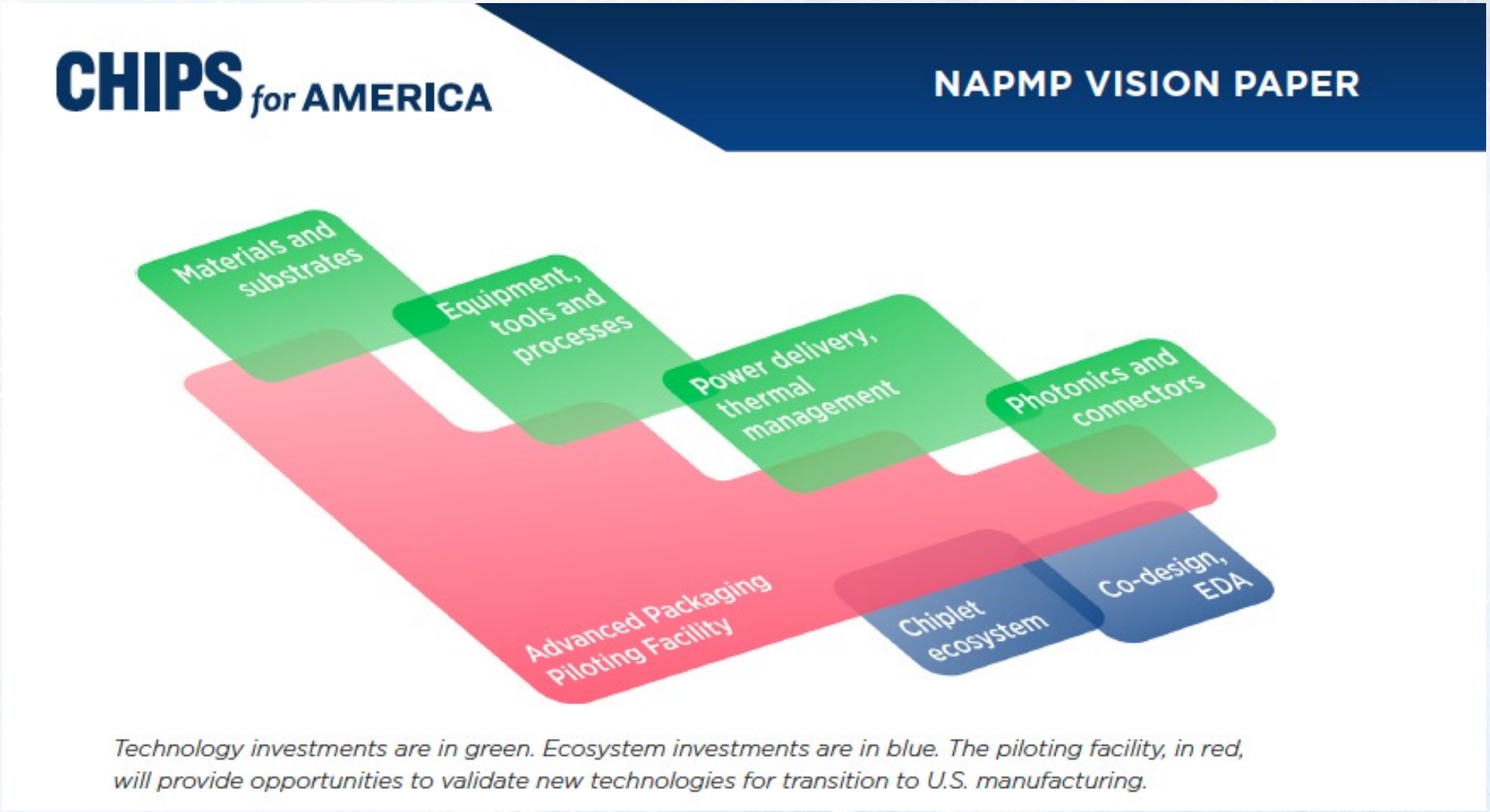


Figure 3. A conceptual diagram of the stages of innovation for a new chip design across various government programs. (Note that the Commons Cores are not displayed. Shading is not to scale of investment.)

National Advance Packaging Manufacturing Program



Technology investments are in green. Ecosystem investments are in blue. The piloting facility, in red, will provide opportunities to validate new technologies for transition to U.S. manufacturing.

National Advance Packaging Manufacturing Program

Advanced Packaging

NOTICE OF FUNDING OPPORTUNITY (NOFO)

National Advanced Packaging Manufacturing Program (NAPMP) Materials & Substrates

Executive Summary

Federal Agency Name: National Institute of Standards and Technology (NIST), United States Department of Commerce (DOC)

Funding Opportunity Title: FY2024 CHIPS R&D National Advanced Packaging Manufacturing Program (NAPMP) Materials & Substrates

Announcement Type: Initial

Funding Opportunity Number: 2024-NIST-CHIPS-NAPMP-01

Assistance Listing Number(s): 11.042 – CHIPS R&D

Funding Opportunity Description: This NOFO seeks applications for research and development activities that will establish and accelerate domestic capacity for advanced packaging substrates and substrate materials. Through this NOFO, the NAPMP program seeks to achieve the following objectives:

(1) Accelerate domestic R&D and innovation in advanced packaging materials and substrates;
(2) Translate domestic materials and substrate innovation into U.S. manufacturing, such that these technologies are available to U.S. manufacturers and customers, including to significantly benefit U.S. economic and national security;
(3) Support the establishment of a robust, sustainable, domestic capacity for advanced packaging materials and substrate R&D, prototyping, commercialization, and manufacturing; and
(4) Promote a skilled and diverse pipeline of workers for a sustainable domestic advanced packaging industry.

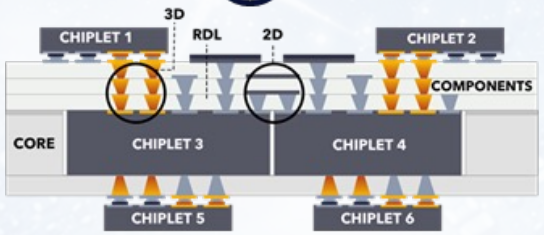
Table 1. Materials & Substrates NOFO Key Dates	
Webinar Information Session	March 1, 2024
Proposers Day	March 12, 2024
Concept Papers Due	April 12, 2024
Invited Full Applications Due	July 3, 2024

Table 2: CHIPS R&D-specified Technical Targets

Technical Target Category	CHIPS R&D-specified Technical Targets		
	TA 1 (Organic)	**TA 2 (Glass)**	**TA3 (Semiconductor-Based)**
1. Minimum Line Width, Spacing, and Pitch	1 µm line width, 1 µm line spacing, 2 µm pitch	0.5 µm line width, 0.5 µm line spacing, 1 µm pitch	0.25 µm line width, 0.25 µm line spacing, 0.5 µm pitch
2. Coplanarity at Die Attach (Bonding Area)	Below 0.5 µm over dielet area, where dielet area can vary between 1 mm x 1 mm to 10 mm x 10 mm	Below 0.5 µm over dielet area, where dielet area can vary between 1 mm x 1 mm to 10 mm x 10 mm	Below 0.5 µm over dielet area, where dielet area can vary between 1 mm x 1 mm to 10 mm x 10 mm
3. Interlevel via diameter	1 µm	0.5 µm	0.25 µm
4. Through substrate via diameter	Less than 100 µm	Less than 100 µm	Less than 100 µm
5. Max wire thickness	Equal to wiring pitch	Equal to wiring pitch	Equal to wiring pitch
6. Max number of Layers (hierarchical)	10+10 (side 1 + side 2), or 15 single sided for Fan Out wafer level packaging	10+10 (side 1 + side 2)	15+15 (side 1 + side 2)

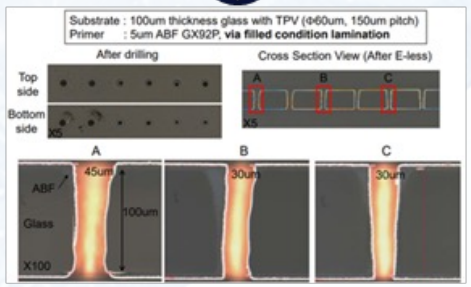
Glass substrate (MAESTRO Roadmap)

1



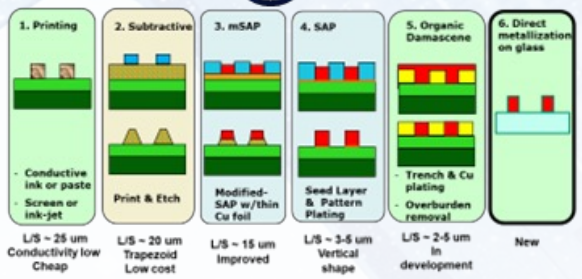
- Glass core substrates: Surface roughness, CTE, modulus, moisture absorption like Si but dielectric insulator and large area (500mm) to reduce cost.

2



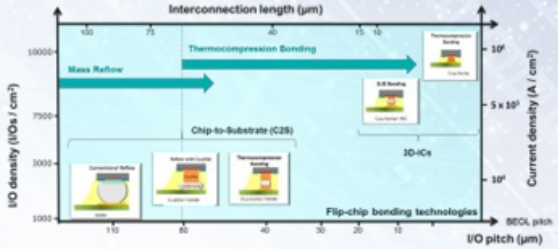
- 10um/20um pitch through core vias with 20:1 aspect ratio

3



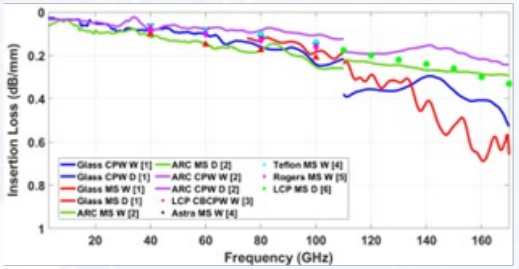
- 10um L/S (mmWave)
- 8+ Metal Layers
- 1um L/S with good adhesion (mixed signal)

4



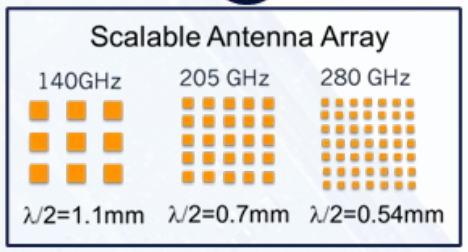
- 35um C2S (mmWave)
- <10um assembly pitch C2S (mixed signal)
- No cracking or delamination

5



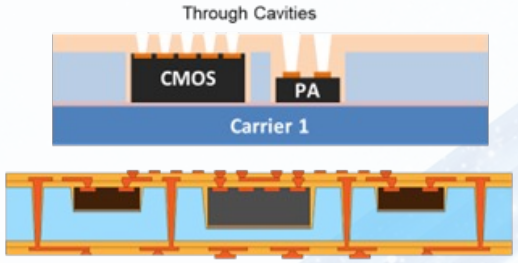
- Low Dk (3.0), Low Df (10^{-4}) dielectrics; 5-100 um thick
- Air Dielectrics

6



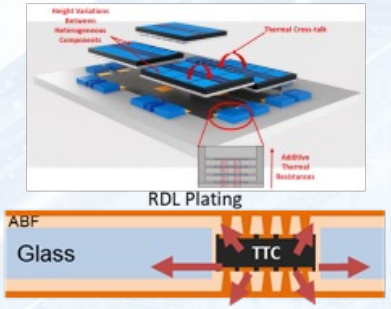
- Antenna in Package
- Patch/Slot antennas
- Base station / Handset

7



- Through & Blind Cavities
- CMOS/InP 75-150um die thickness
- <1dB loss

8



- Thermal Insulator (1W/mK)
- Thermal Mgmt (>400W/mK)

9

End User
EDA Optimization
Substrate
Assembly & Test
Equipment Manf.
Materials

- Supply Chain Eco-system needs to come together

Manufacturing USA Semiconductor Institute

Vision

Enable **seamless integration of digital twin models** into the U.S. semiconductor manufacturing, advanced packaging, and assembly industries, enabling rapid adoption of innovations and enhancing domestic competitiveness for decades.

Mission

Foster a **collaborative environment** within the domestic semiconductor industry, enabled by the world's first **shared** semiconductor Digital Twin process **validation facility**, industry-relevant research projects, and digital-twin supported workforce training.

Digital Twin Institute Approach

A physical facility and digital framework, integrated with industry-led research projects

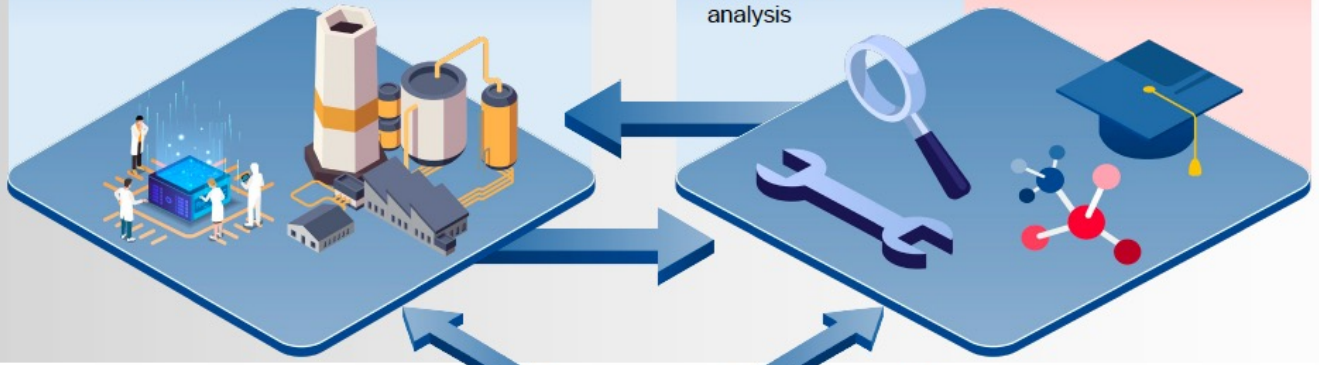
1 Establish a **shared physical facility**

Expected activities:
- Baseline facility testbed
- Digital emulation hardware
- Core technical & operations staff

2 Competitively fund **industry-led technical and workforce development projects**

Deliver technical solutions, de-risk new tools, and conduct data analysis

Develop and test education & workforce development tools enabled by digital twins



3 **Digital framework** for interoperable data and models

4 Create a **shared marketplace** of digital twin models

CHIPS for AMERICA

Manufacturing USA Semiconductor Institute

MASH Manufacturing Institute

Industries

Academia

Advanced tools for simulation, fabrication, test, assembly & packaging

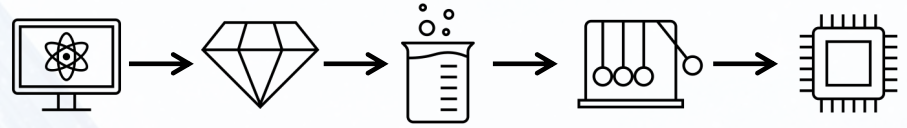
PennState · Penn · Carnegie Mellon University · University of Maryland · NYU · University of the District of Columbia · University of Delaware · Princeton University · Boston University · Columbia

Industrial facilities and resources for precompetitive collaborations

Foundry

Government Programs

Trained workforce



Advance Prototyping

Workforce Development

- **Manufacturing Institutes**
- **NSTC**
- **NAPMP projects**
- DoD NGMM & ME Commons
- WFD organizations
- Federal Science programs

MASH working groups

- Workforce development
- Silicon adjacent materials
  - Materials for Power Electronics
  - Materials for Optical Interconnects
  - Ferro and Piezoelectric materials
- Digital Twins and AI
- Advanced Packaging
  - MAPT
  - CHIPS
  - 5G/6G Maestro (iNEMI)

More than 450 participants from industry and academia

Contact:
Madhavan Swaminathan
Daniel Lopez
Urmi Ray

The people behind MASH

	NAME	TITLE
PennState	**Daniel Lopez**	Liang Professor of Electrical Engineering Director, Nanofabrication Lab, Materials Research Institute
	Osama Awaldelkarim	UNESCO Chair Professor Director, Center for Nanotechnology Education and Utilization
	Shannon Munro	Vice President for Workforce Development Pennsylvania College of Technology
	Mark Threeton	Professor of Education, Associate Director of PPDC
	Priya Baboo	Senior Director of Corporate and Industry Engagement, College of Engineering
Penn	**Mark Allen**	Scientific Director, Singh Center for Nanotechnology
	Gerald Lopez	Director, Business Development Singh Center for Nanotechnology
Carnegie Mellon University	**Gianluca Piazza**	Professor, Electrical and Computer Engineering
	Matthew Moneck	Executive Director, Nanofabrication Facility
NYU	**Nina Gray**	Assistant Vice Provost for Research
	Kurt Becker	Vice Dean for Research, Innovation and Entrepreneurship

	NAME	TITLE
University of Delaware	**Jamie Philips**	Chair, Department of Electrical and Computer Engineering
Princeton University	**Alex Norman**	Executive Director Princeton Materials Institute
	Barry Rand	Associate Professor of Electrical and Computer Engineering
	Richard Register	Director, Materials Institute
Boston University	**David Bishop**	Head of the Division of Materials Science & Engineering
	Alice White	Professor and Chair, Mechanical Engineering
Columbia University	**James Hone**	Chair, Department of Mechanical Engineering
	Samar Kaukab	Director of Strategic Research Development
University of Maryland	**Pamela Abshire**	Professor, Electrical and Computer Engineering
	Ankur Srivastava	Professor & Director Institute for Systems Research
University of the District of Columbia	**Pawan Tyagi**	Professor of Mechanical Engineering & Director of ME Graduate Program

Susan Trolier-McKinstry

Madhavan Swaminathan

Daniel Lopez

MASH summary

- Distributed network of academic, federal, and industrial resources and a cloud of talent in all the components of the manufacturing supply chain
- Regionally-centered programs with strong national connections and participation.
- Focused on transitioning materials into systems with strong emphasis on packaging and developing agile education and workforce opportunities.

MASH Partners:

- 160+ industry
- 300+ organizations
- 3 National Labs
- 18 academic institutions
- 500+ members
- Support from local states

Targeted opportunities:

- **NAPMP** (Madhavan Swaminathan)
- **Manufacturing Institute** (Daniel Lopez)

THANK YOU

Daniel Lopez

Liang Professor of EE
Director Nanofabrication Lab
Materials Research Institute
Penn State University

dlopez@psu.edu

Madhavan Swaminathan

Dept. Head Electrical Engineering
William E. Leonhard Endowed Chair
Director, CHIMES (an SRC JUMP 2.0 Center)
Penn State University

mvs7249@psu.edu

mash-semiconductors.org

MASH brochure

	NAME	TITLE
PennState	**Jennifer McCann**	Marketing Director, Materials Research Institute MASH Communications Manager
	Kimberly Brue	Assistant Vice President Research Communications
Penn	**Lee Ozier**	Program Coordinator Singh Center for Nanotechnology
Carnegie Mellon University	**Laura Snyder**	Senior Director of Research Communications
NYU	**Joseph Tirella**	Senior Director of Executive Communications
University of Delaware	**Tracey Bryant**	Senior Director for Research Communications
Princeton University	**Steven Schultz**	Director of Engineering Communications
Boston University	**Rachel Lapal Cavallario**	Associate VP, Public Relations
Columbia University	**Michele Hoos**	Executive Director of Communications, Engineering
University of Maryland	**Institute for Systems Research**	Resources for the Media
University of the District of Columbia	**Leeaan Hall**	Vice President for Marketing & Communications
	Andrea Williams	Assistant Vice President for Marketing & Communications

Available at https://mash-semiconductors.org/