A Novel Approach to Co-Design of Analog and RF Multi-Die Packages

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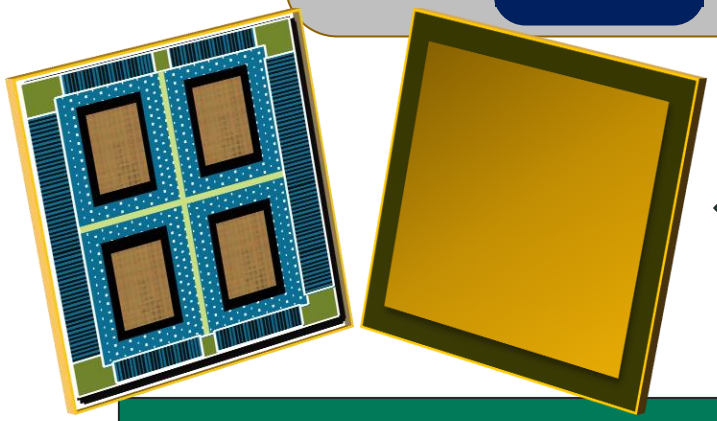
cadence®

Analog/RF Market Landscape

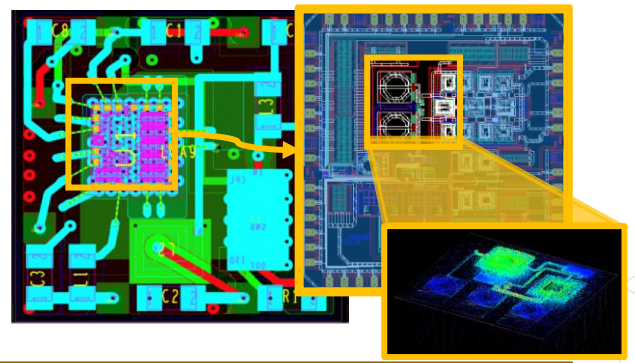
The RF market is rapidly expanding with 5G, Automotive, and A&D

Aero/Defense | Automotive | IoT | 5G | Mobile



SiP module content and complexity, increasing with multiple technologies for IC, filters, switches, and other components

While SiP layout module content is increasing, geometries are getting smaller creating a higher risk for coupling



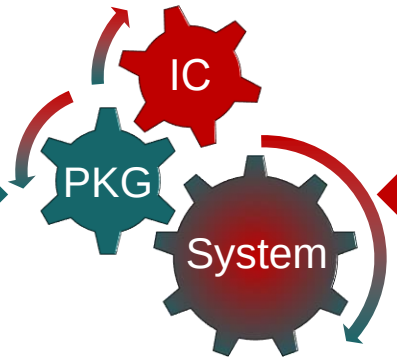
Disjointed tool flows are no longer sufficient to address the level of complexities and time-to-market constraints

The Needs of IC and Systems Designers are Converging

OSATs (SWaP)

Board design impact on packaging

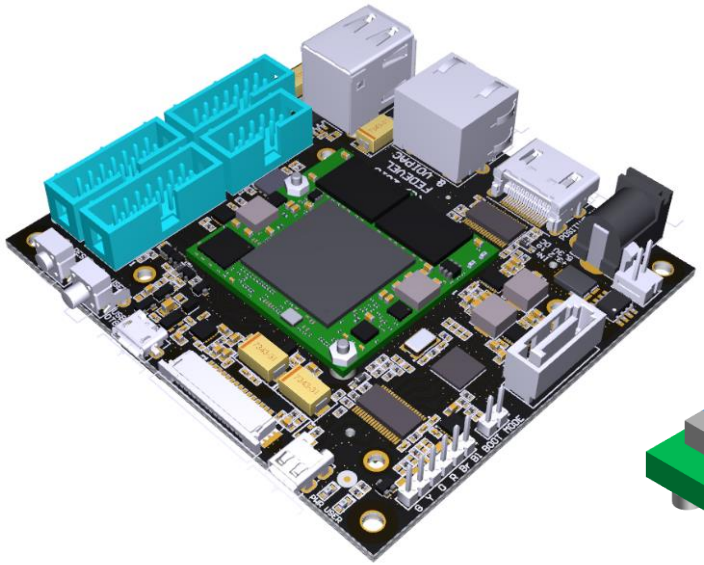
1980-2010



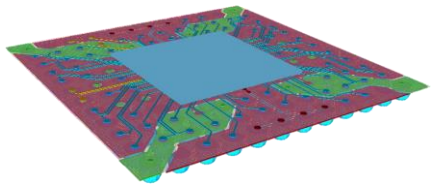
Foundries (PPA)

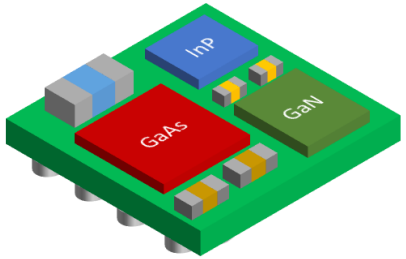
IC design impact on packaging

2011-Now

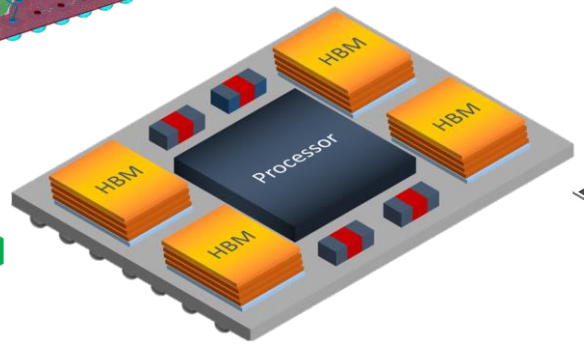


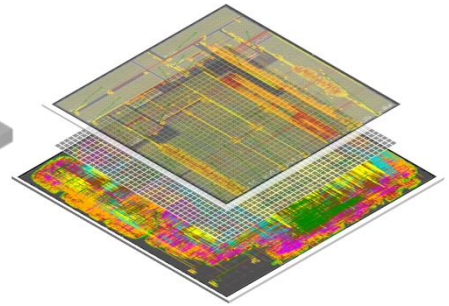
PCB Layout Flow
System-Level Analysis



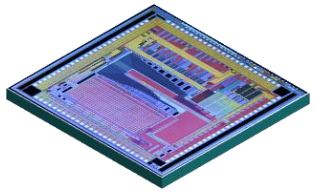


PCB-like Flow
System-Level Analysis



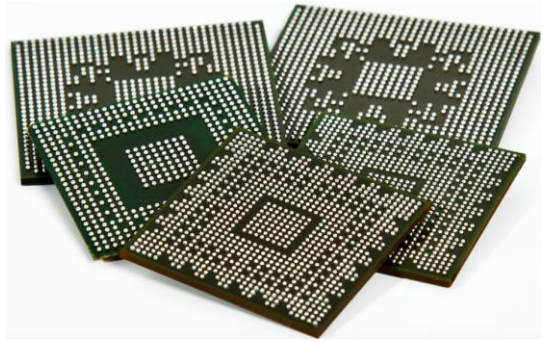
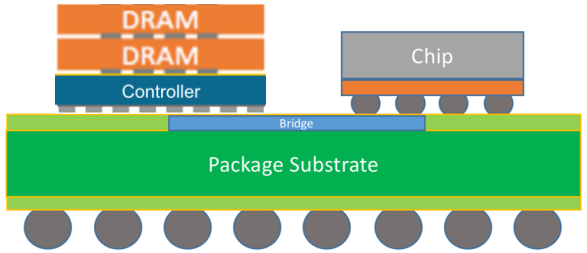
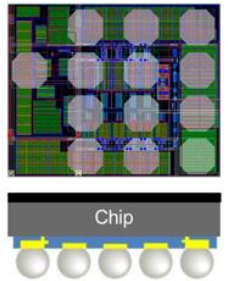
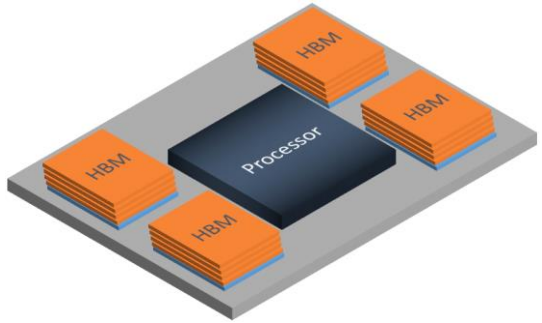
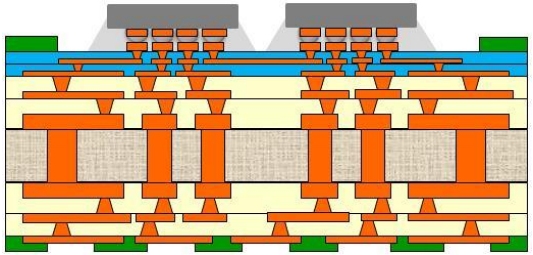
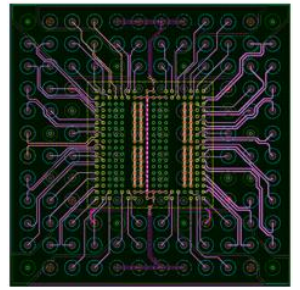
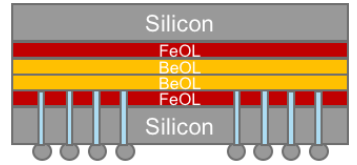


IC-like Implementation Flow
IC signoff Methodology and
System-Level Analysis

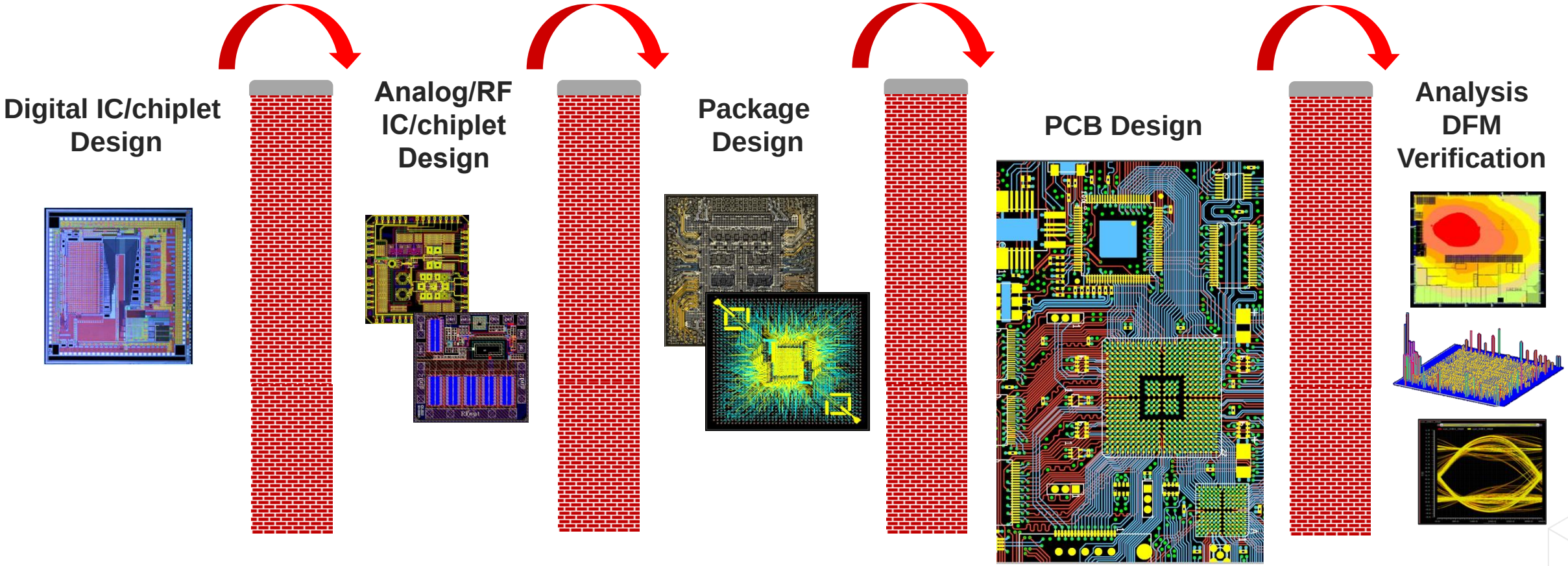


IC Flow
IC signoff Methodology

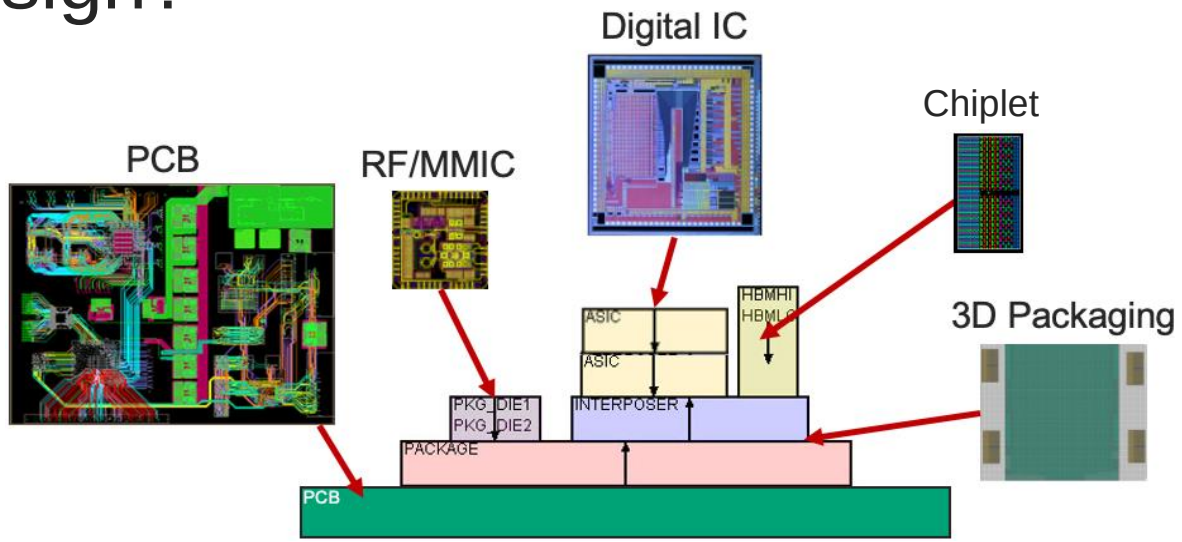
There is No One Way to Integrate/Package Die/Chiplets

Mechanical Leadframe	Substrate Based Organic, Ceramic, Silicon	Multi-Tech Substrates (Heterogeneous Substrates)	Substrate-less WLCSP, FOWLP & 3D IC
			
			
			

Over-the-Wall Design Approach Leads to Higher Costs, Longer Design Cycles and Lower Performance of Electronic Products



What is Co-Design?



Optimizing each device in context of the complete system
Digital ICs
Analog/RF ICs
Chiplets
Packaging
PCB

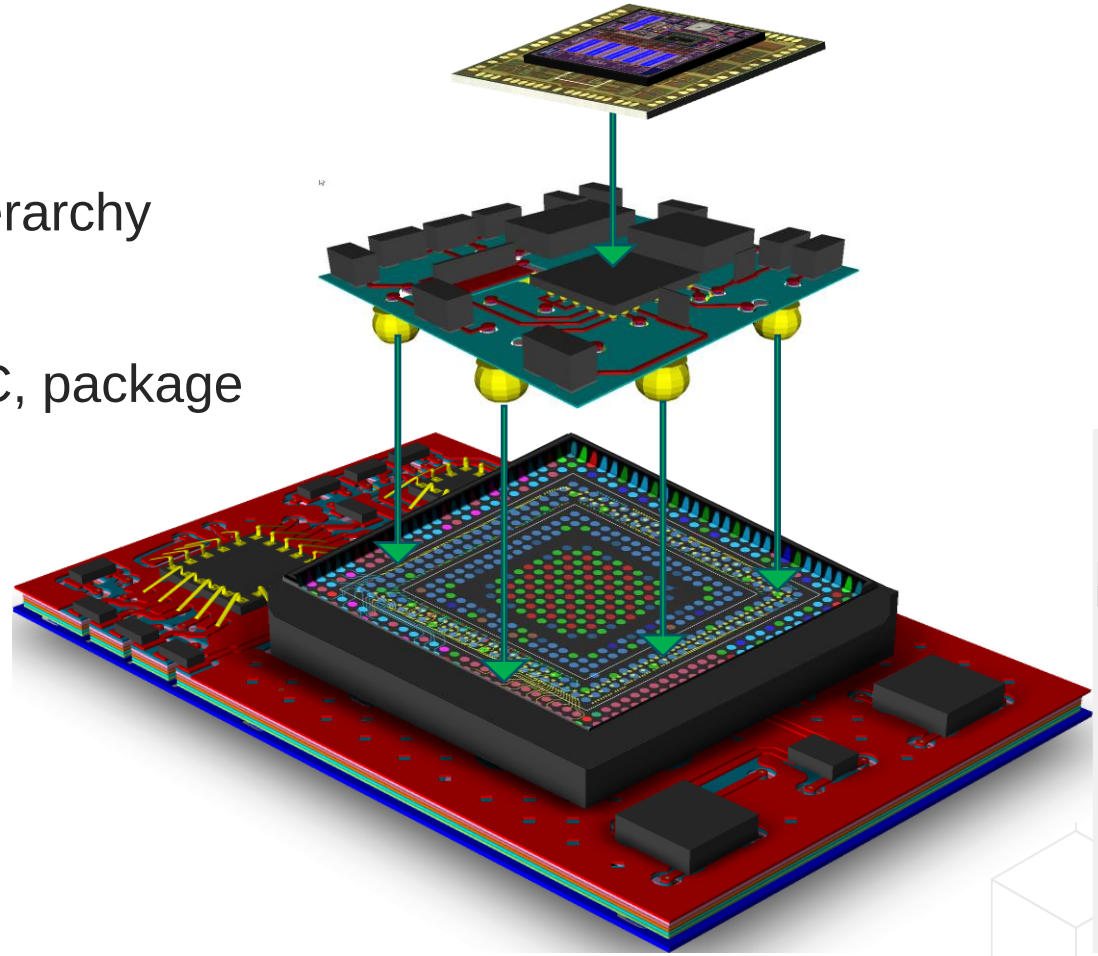
Partitioning/floor-planning in context of the complete system
I/O buffer placement and size
Power/Thermal (Heat)
D2D and full system level connectivity
Cross-device coupling/noise
Packaging technology tradeoffs

What's Needed From EDA to Enable Co-Design?

- Single design tool with concurrent editing
  - Is this possible? At what abstraction level?
- Common library across design tools
- Flexible connectivity use-model
  - Text, schematics and on-the-fly
- Seamlessly integrated system level analysis thought-out flow
  - Automatic parasitic stitching
- SystemLVS
- Assembly design kits (ADKs)
- Digital twinning
- AI/ML to improve automation

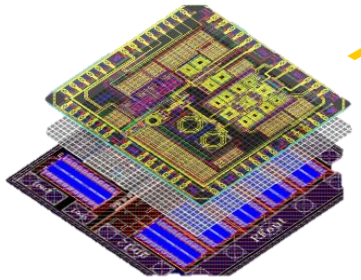
Co-Design Challenges of Analog/RF Multi-Die Systems

- Optimizing system-level performance
- Layout to EM loop
  - Design vs Layout is different in RF
  - Hard to hook up s-parameters into original design hierarchy
- Increase analysis fidelity and accuracy
  - Characterizing electromagnetic interactions across IC, package and even PCB
- SystemLVS is a big cause for re-spins
  - Common source for system-level connectivity (schematic)
  - Avoiding mistakes due to alignment of die(s), module, package and board
  - Implemented in different tools with different orientations and scaling

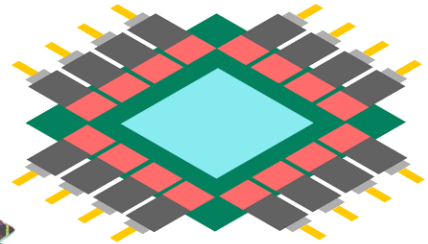


Analog/RF/Photonics Flow

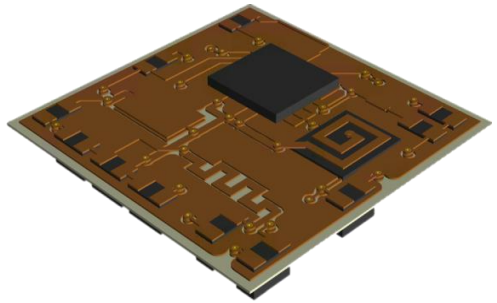
Analog/RF IC Design Platform



Analog/RF
Die Stacking



Co-Packaged
Optics

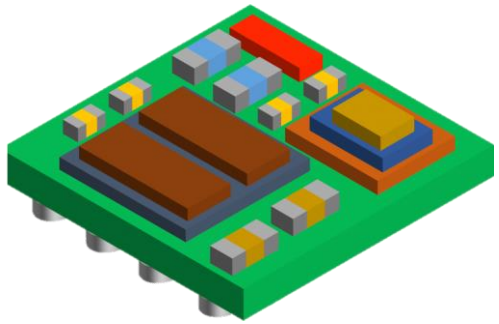


RF Module

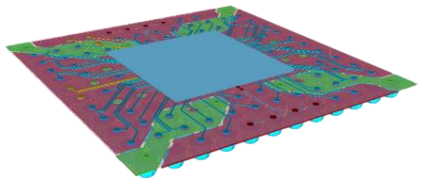
Digital System Planner

Co-Design

Package Design



SiP/MCM



FOWLP

3D-EM, Electrical and Thermal Sign-Off

- Single hierarchical schematic for complete system co-design
- Multi-tech enables multi-PDK concurrent design
- Edit-in-Concert advanced cross-domain co-design
- Seamless integration of on-chip and off-chip EM
- Modeling of die to package cross-coupling effects
- Automated layout parasitic back annotation flow
- Unified library & SystemLVS

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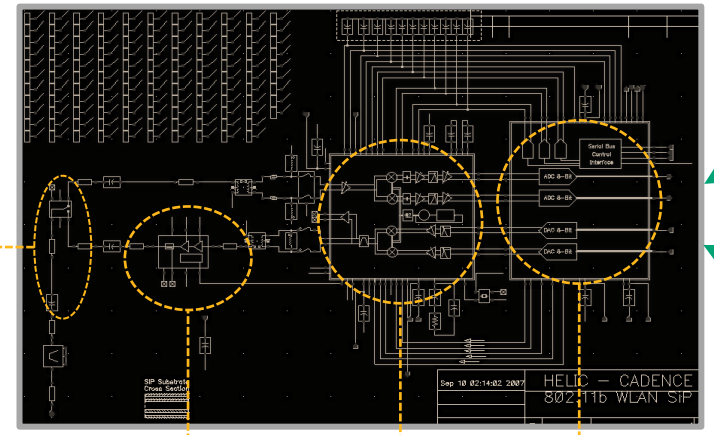
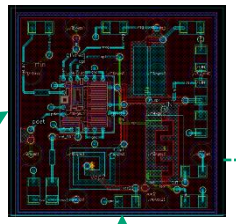
Example Flow

Hierarchical Top-Level Schematic
Representing Complete System-Level Design



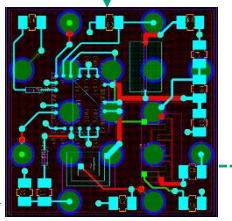
Native Analog/RF IC Layout



Constraints
Connectivity
Die Abstract

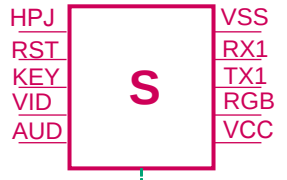
OA⇔SiP

Constraints
Connectivity



MCM/SiP Layout

Interconnect
Parasitics

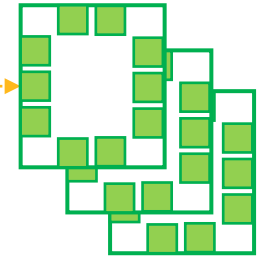


Device Models

PCB

Electromatic
Simulation

Library Instance



Package-Level
Footprints

Package
Lib

CMOS

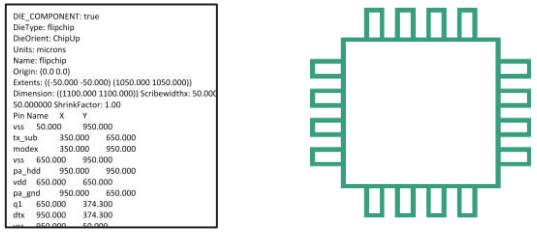
Schematic Symbol

GaAs

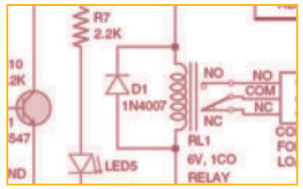
Schematic Symbol

GaN

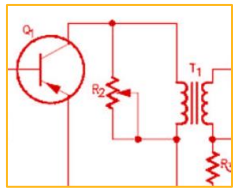
Schematic Symbol



Non-Native IC Layout



Native Analog/RF IC Layout



Native Analog/RF IC Layout

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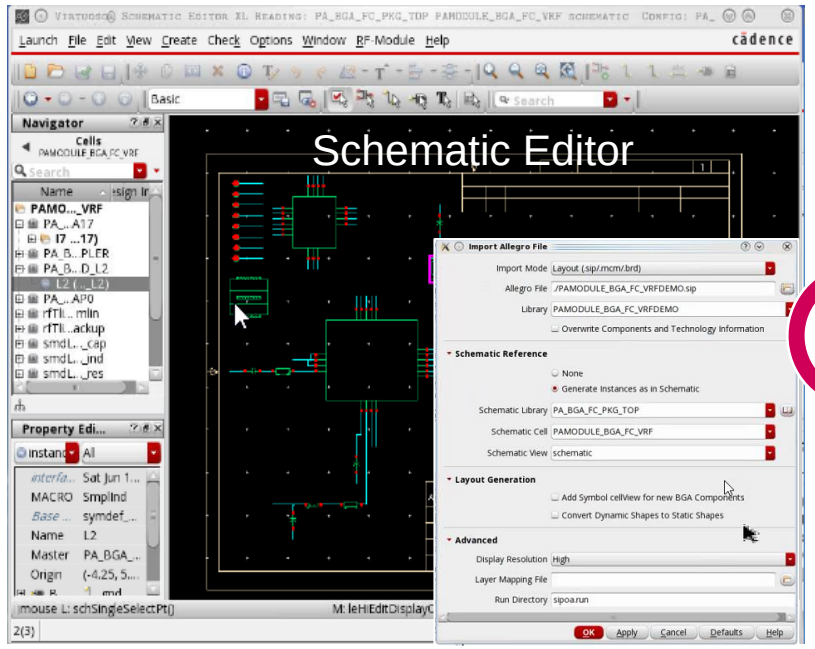
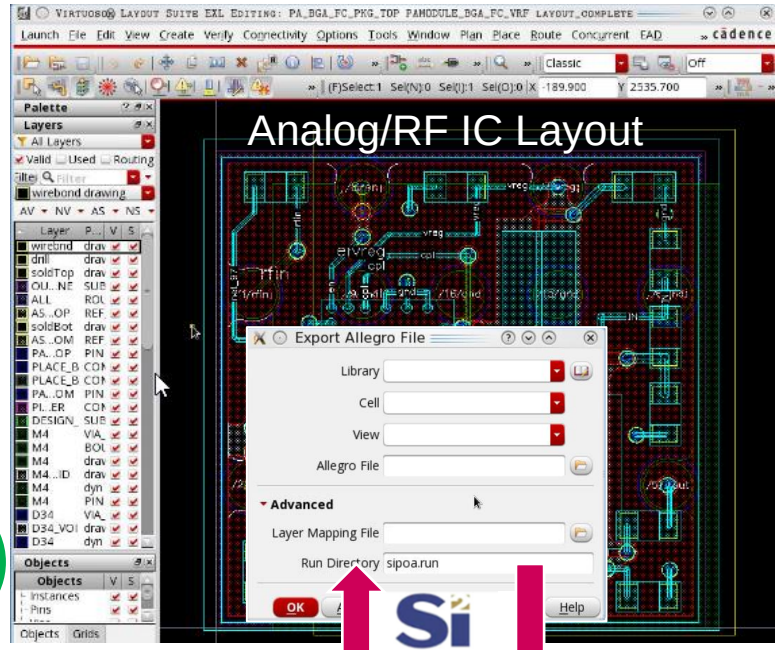
Single-Source System-Level Hierarchical Schematic



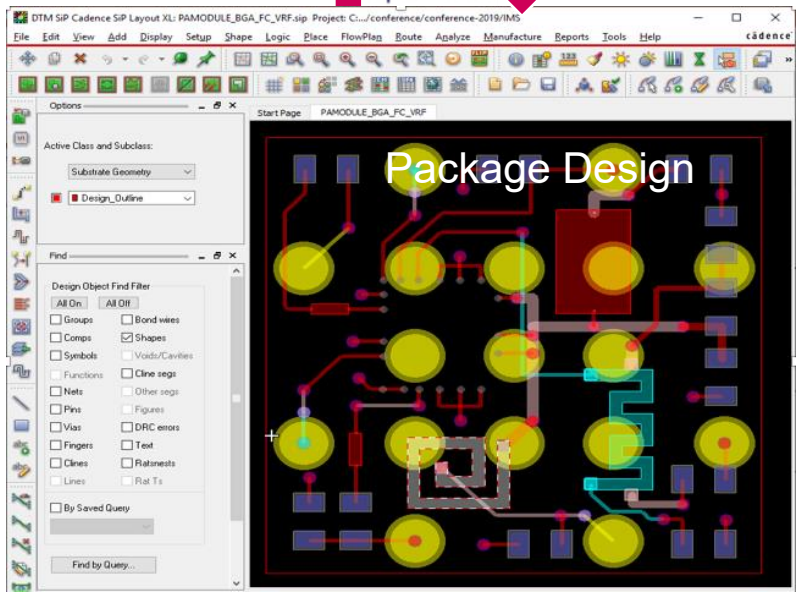
GFS

UCN

CAS



OpenAccess



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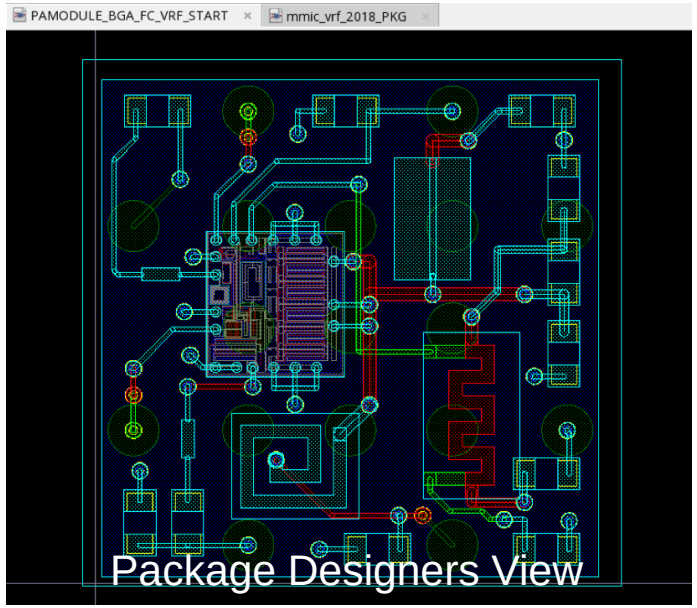
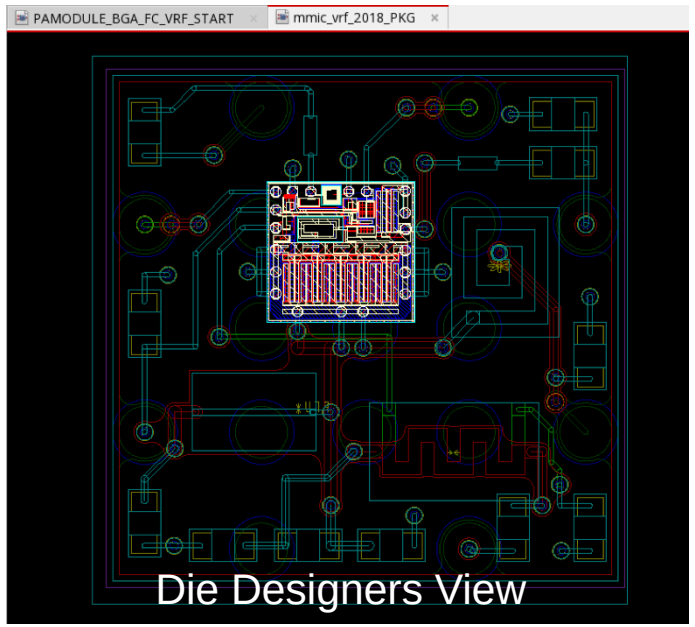
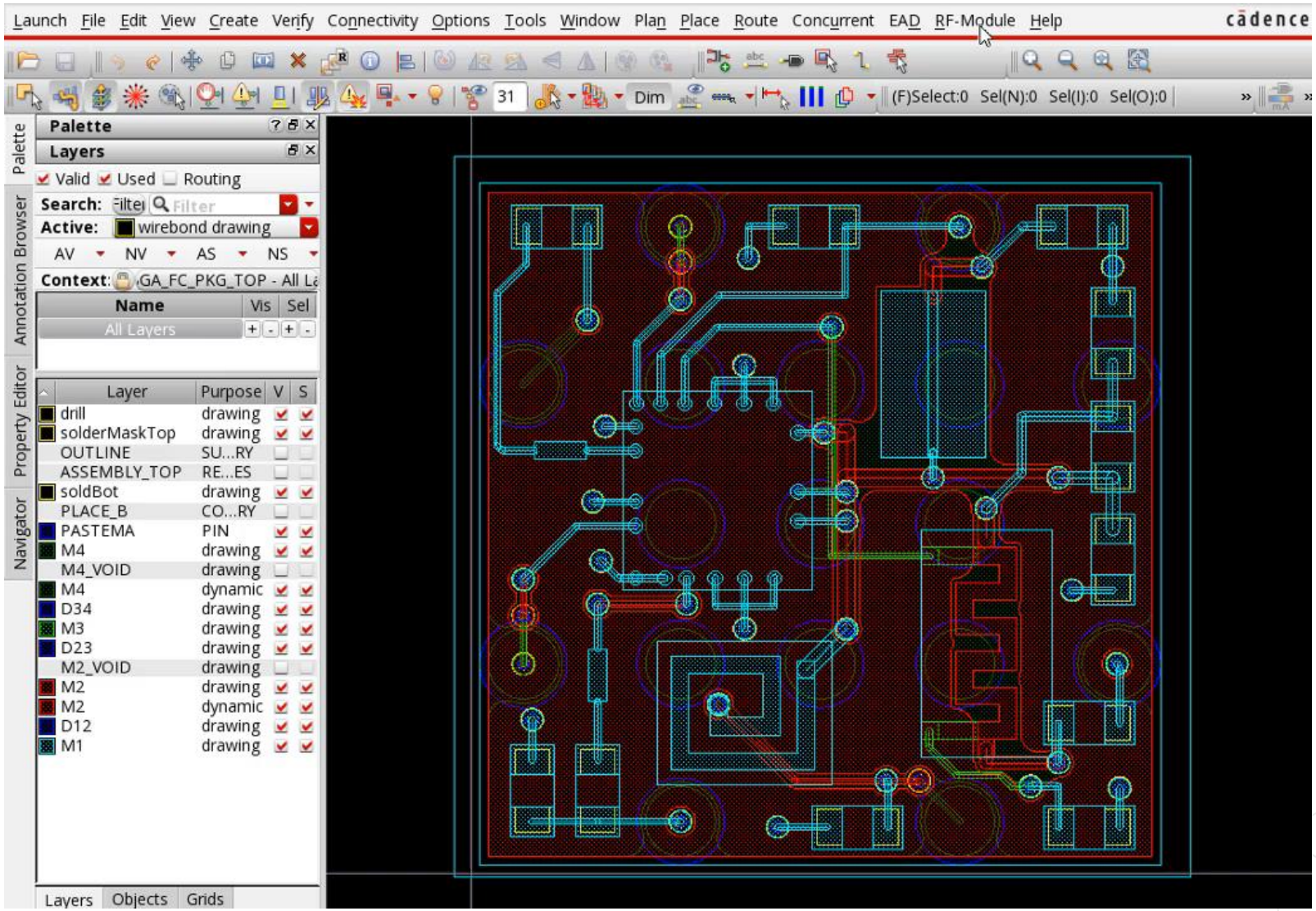
Common Database Enables True Physical IC/Package Co-Design







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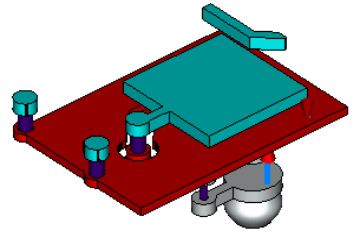
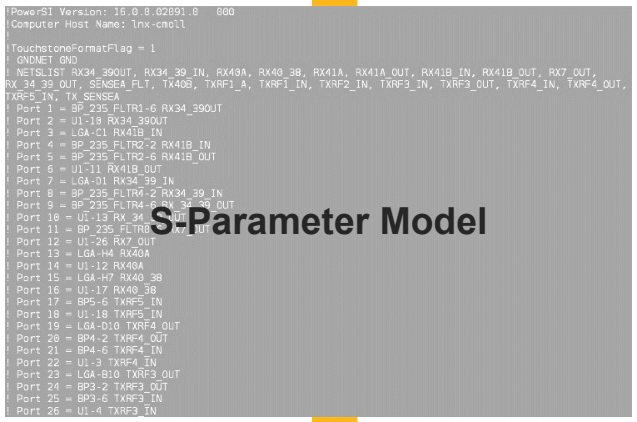
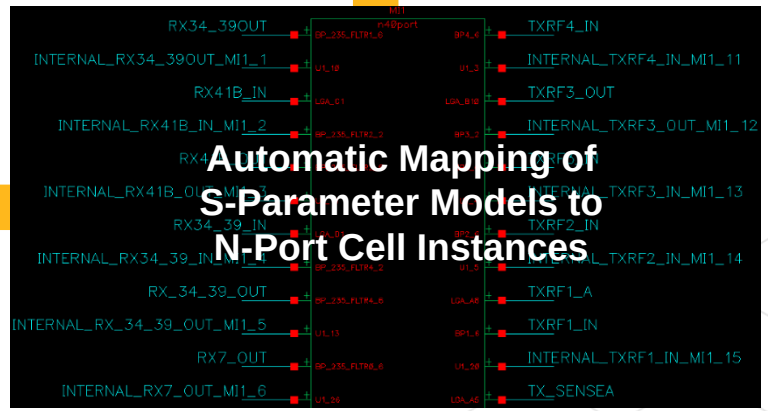
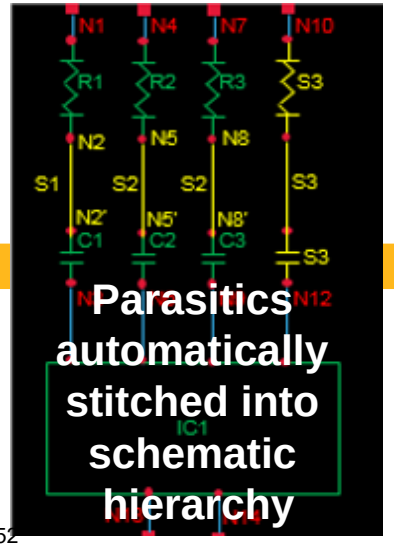
System-Level Layout Parasitic Back-Annotation and Simulation

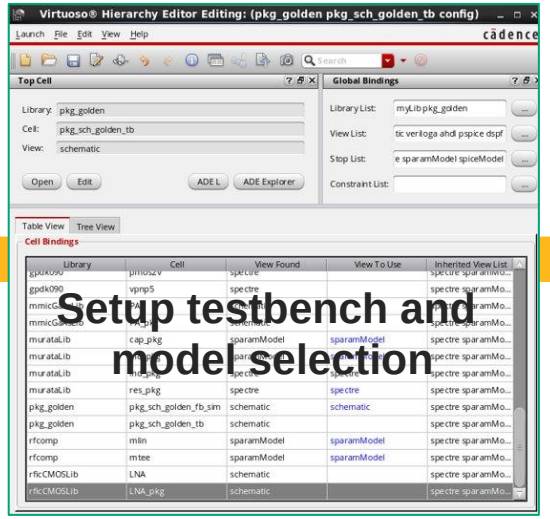
- Coupled 3D-EM extraction between chip(let), package, and PCB layout databases
  - Electromagnetic extraction integrated through an assistant
  - Support for partial/full nets, groupings, and device-level modeling
  - Direct pin mapping and eliminates double-counting of discrete devices
  - S-parameters (freq. domain) and RLGC (time domain) models
- Automatically create schematics (extracted views) that include the layout parasitics from package and PCB
  - Must support multi-PDK, multi-die solutions (namespace collision avoidance)

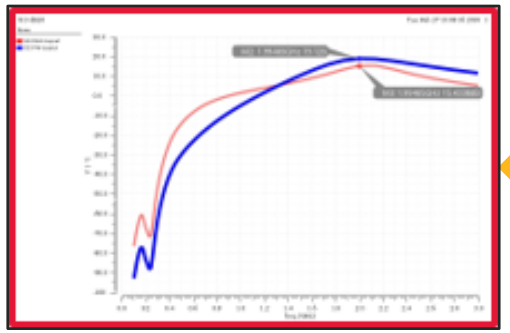








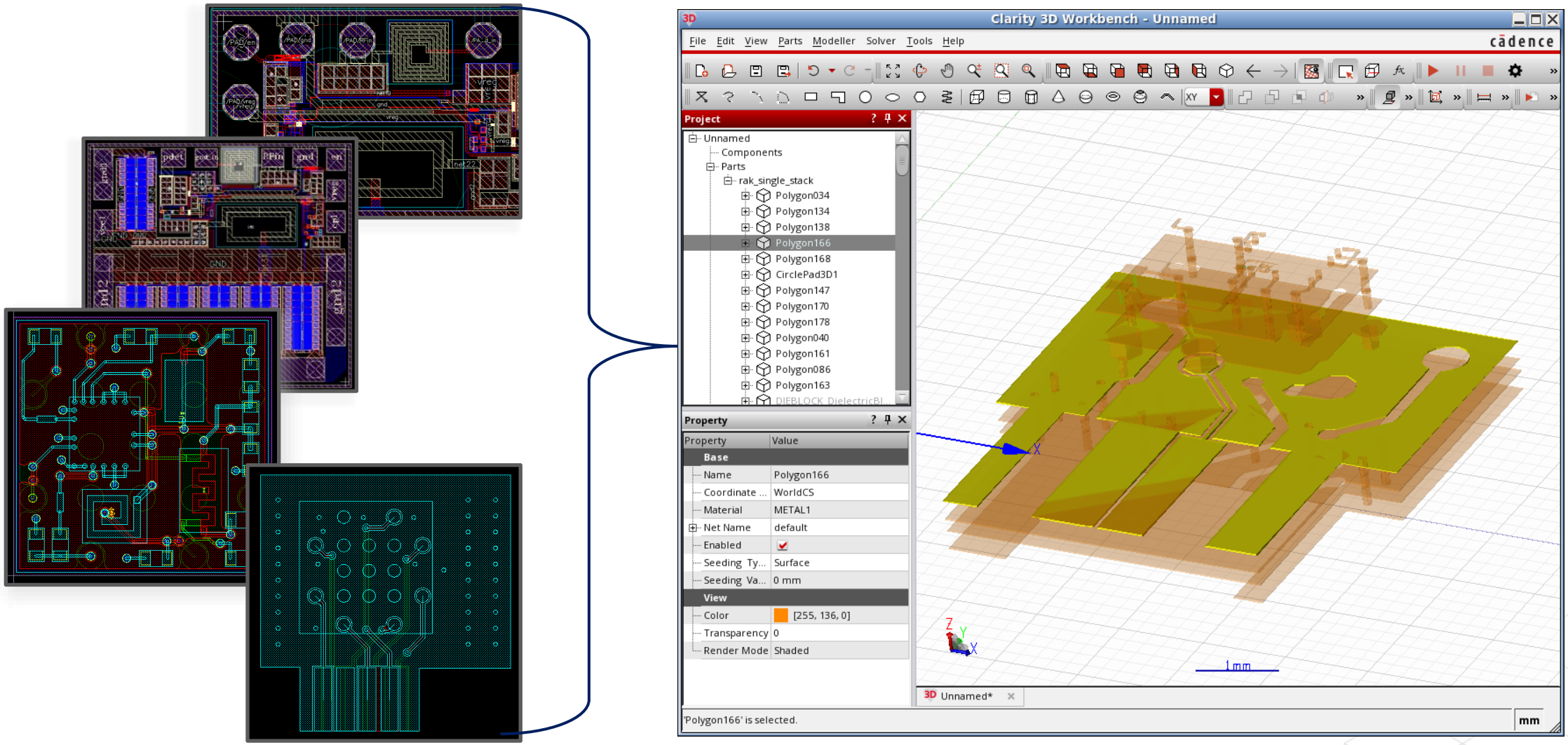




Simulate

Circuit to System – Design and Analysis Solutions

System-level EM modeling



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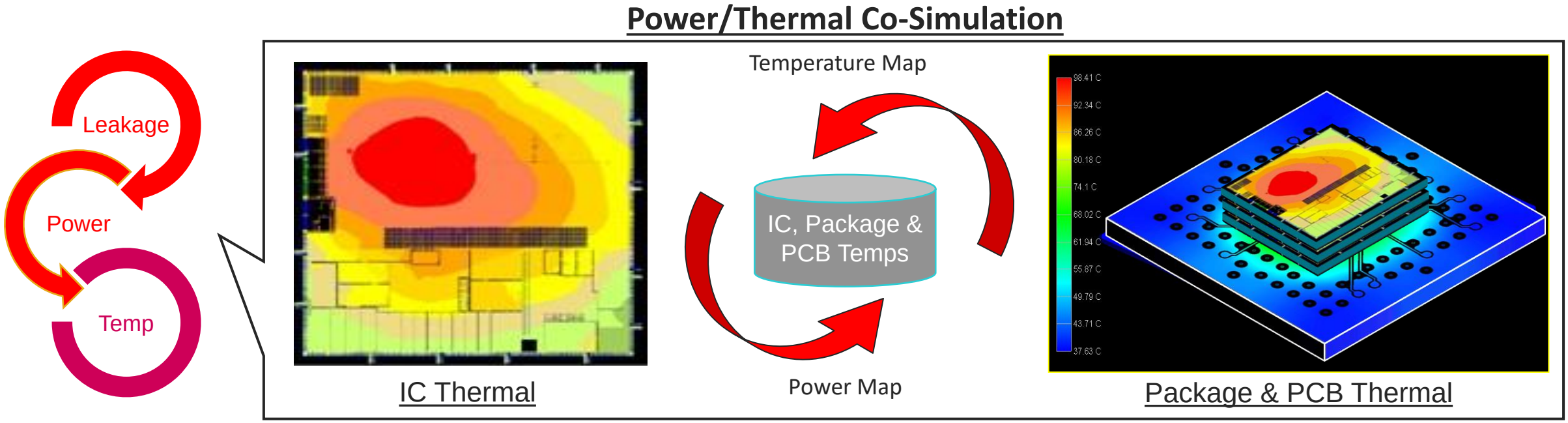
Electrical/Thermal Co-Analysis

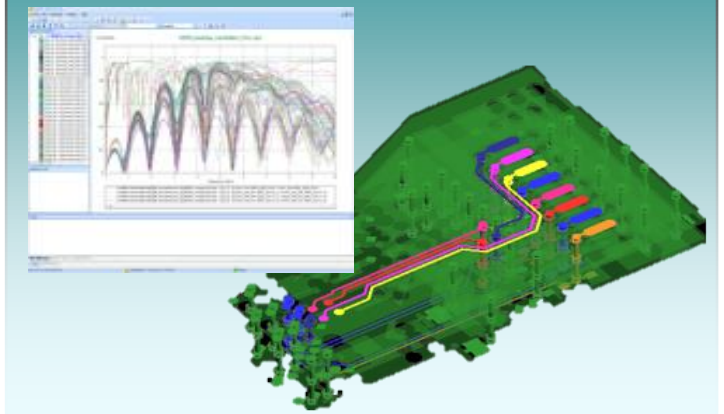


- Thermal runaway
  - Positive feedback and interaction among chip's temperature, leakage and power dissipation
  - Temperature-dependent EMIR failures
- Physics-based 3D thermal simulation
  - Solution generates temperature and location dependent "power-map" file
  - Technology to compute detailed temperature distribution for chip, package and PCB. Provides "temperature-map" file to die-level EMIR solution for iteration and convergence

Robust Technologies for System Analysis and Electrical Signoff

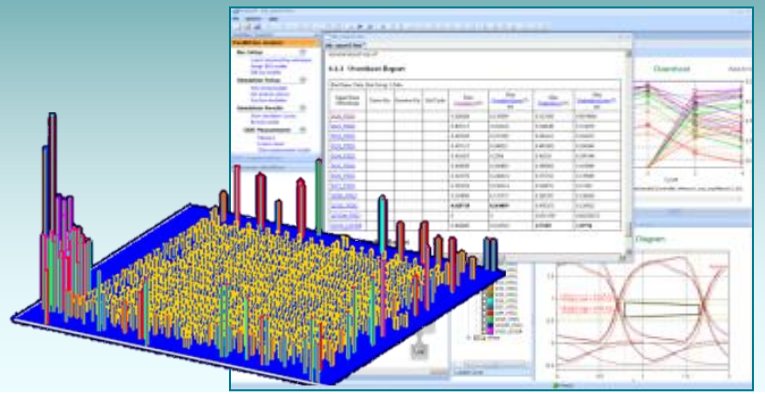
Electromagnetic (EM) Extraction

Massively parallelized matrix solver to model system-level interconnect with high accuracy



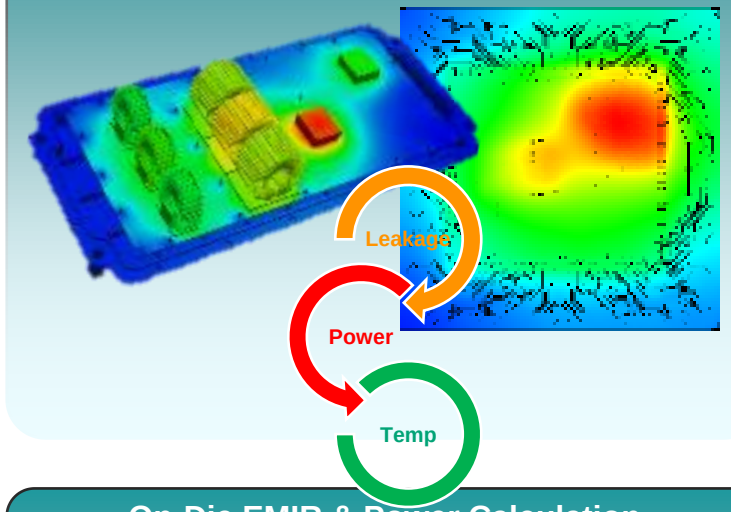
Signal and Power Integrity

Compliance Kits validate chiplet-to-chiplet connectivity
Coupled power and signal integrity analysis
Hybrid solver to model PCB and FC-BGA interconnect
XtractIM for full package model extraction



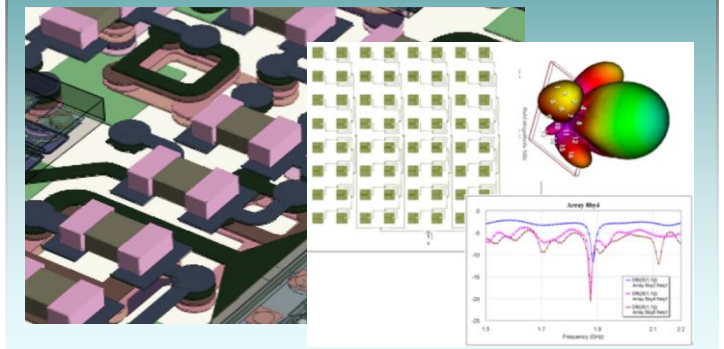
Electrical-Thermal Analysis

Steady-state and transient electro-thermal analysis with optional CFD engine



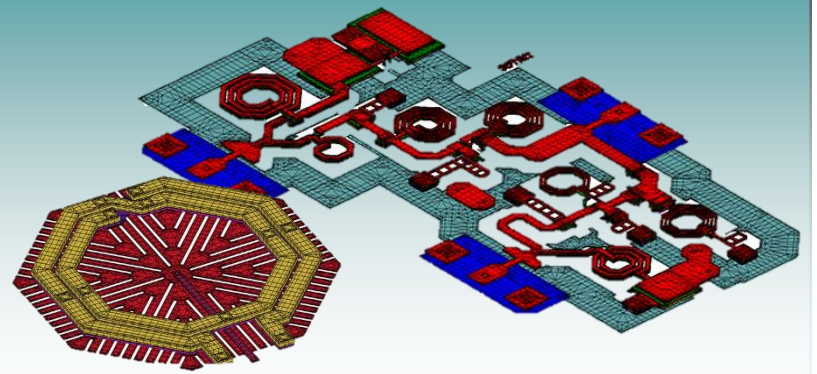
III/V Compound IC Modeling

Extraction of on/off-chip passive structures, transmission lines, planar antennas, and large patch arrays. Supports III/V devices.



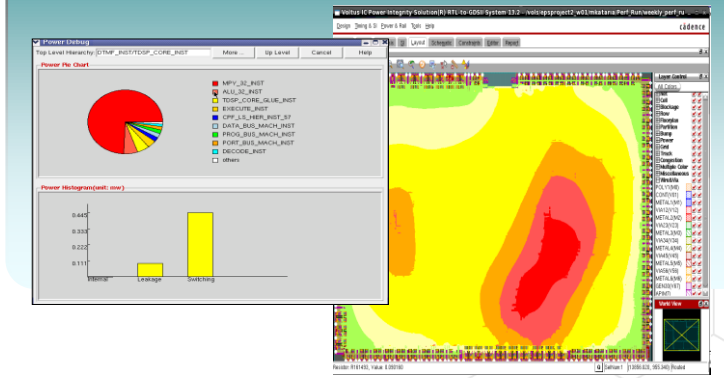
CMOS 3D EM

EM extraction for high-frequency, RF and AMS IC's



On-Die EMIR & Power Calculation

Leakage, internal and switching power
Vector-based or vector-less static and dynamic EMIR

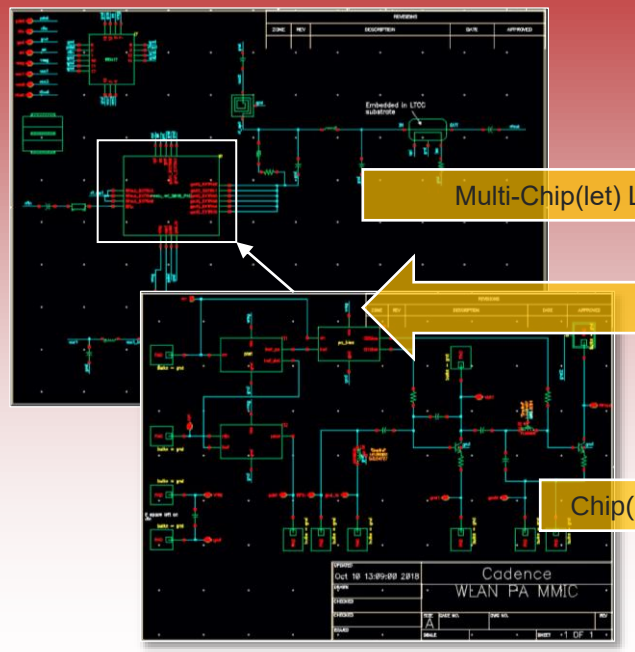


cadence

Integrated IC / Package / PCB / System Co-Design & Co-Analysis

Schematic-Driven Multi-PDK Design

Single system-level hierarchal schematic to drive multi-chip(let) design and verification

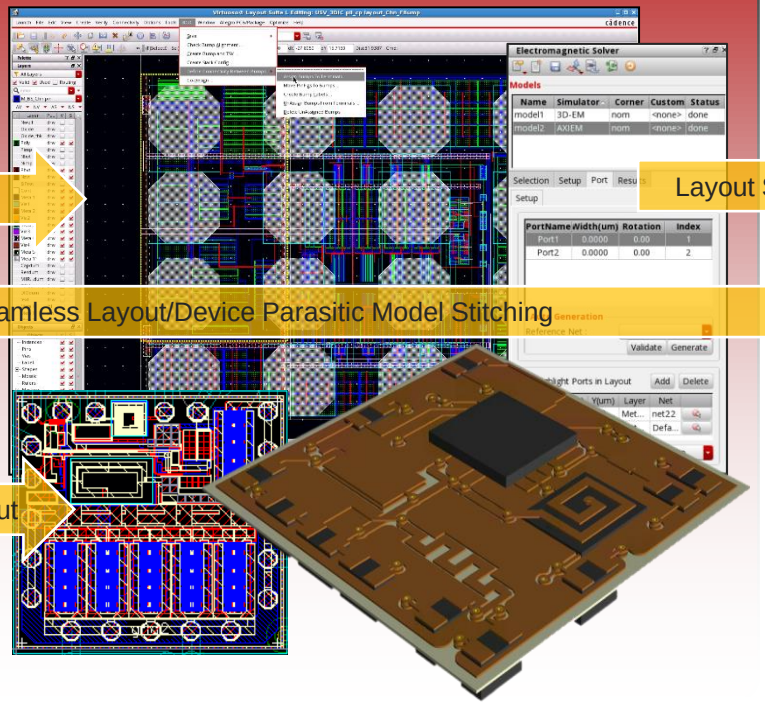


Multi-Chip(let) Layout

Chip(let) Layout

Cross-Platform Layout*

*Seamless Virtuoso/Allegro cross-platform **co-design** of chips, chiplets, packages, and modules*



Seamless Layout/Device Parasitic Model Stitching

On-Chip/Off-Chip EM/Thermal Modeling

Seamless integration with multiple EM extraction engines with automated schematic stitching and simulation flow

Layout Structures