High-end Smartphone SoC packaging Comparison - advanced PoP technology from standard, fan-out to flip-chip assembly

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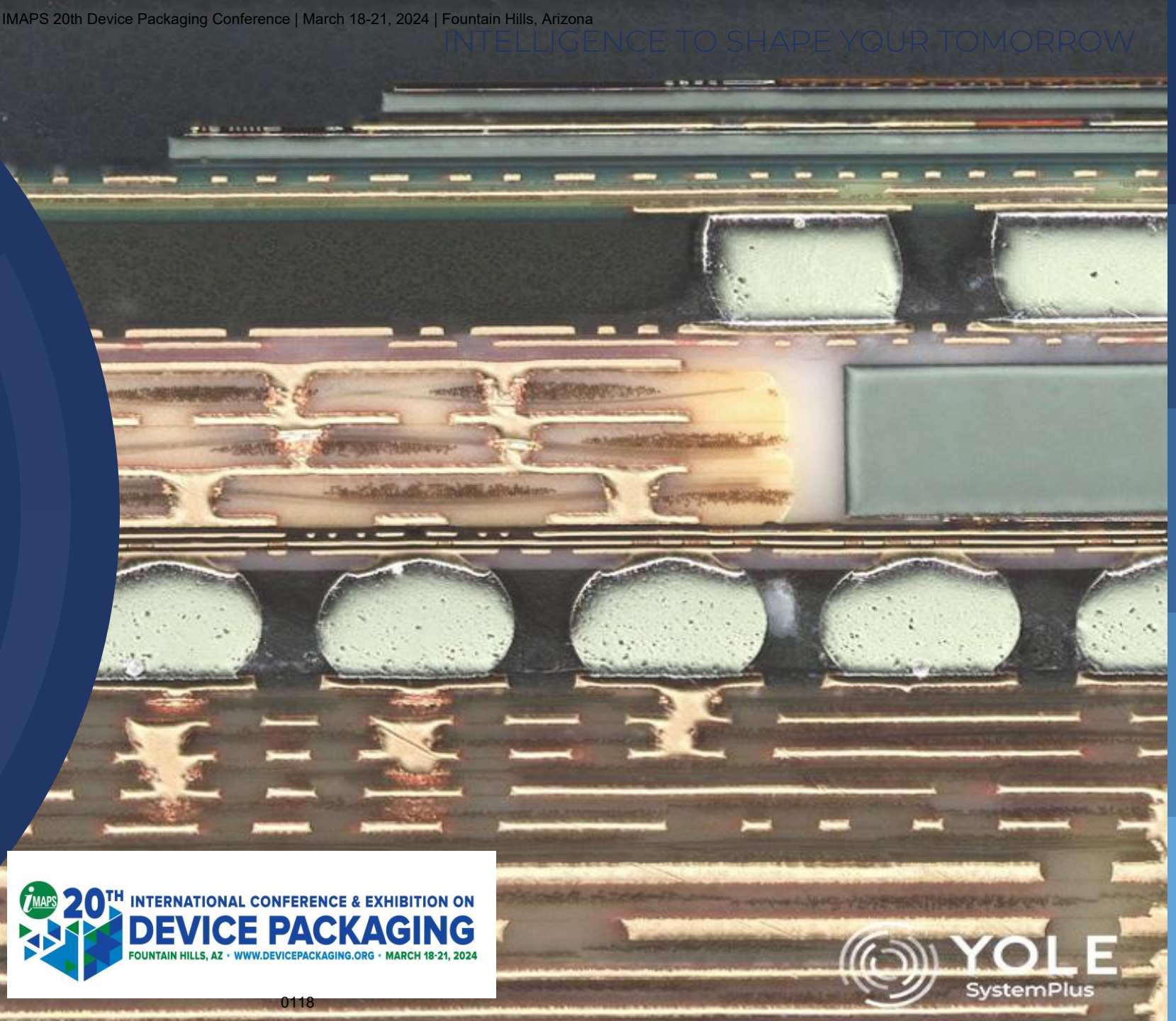
Gabriela Pereira
IMAPS DPC 2024



YOLE Intelligence

20TH INTERNATIONAL CONFERENCE & EXHIBITION ON DEVICE PACKAGING
FOUNTAIN HILLS, AZ · WWW.DEVICEPACKAGING.ORG · MARCH 18-21, 2024

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SUMMARY

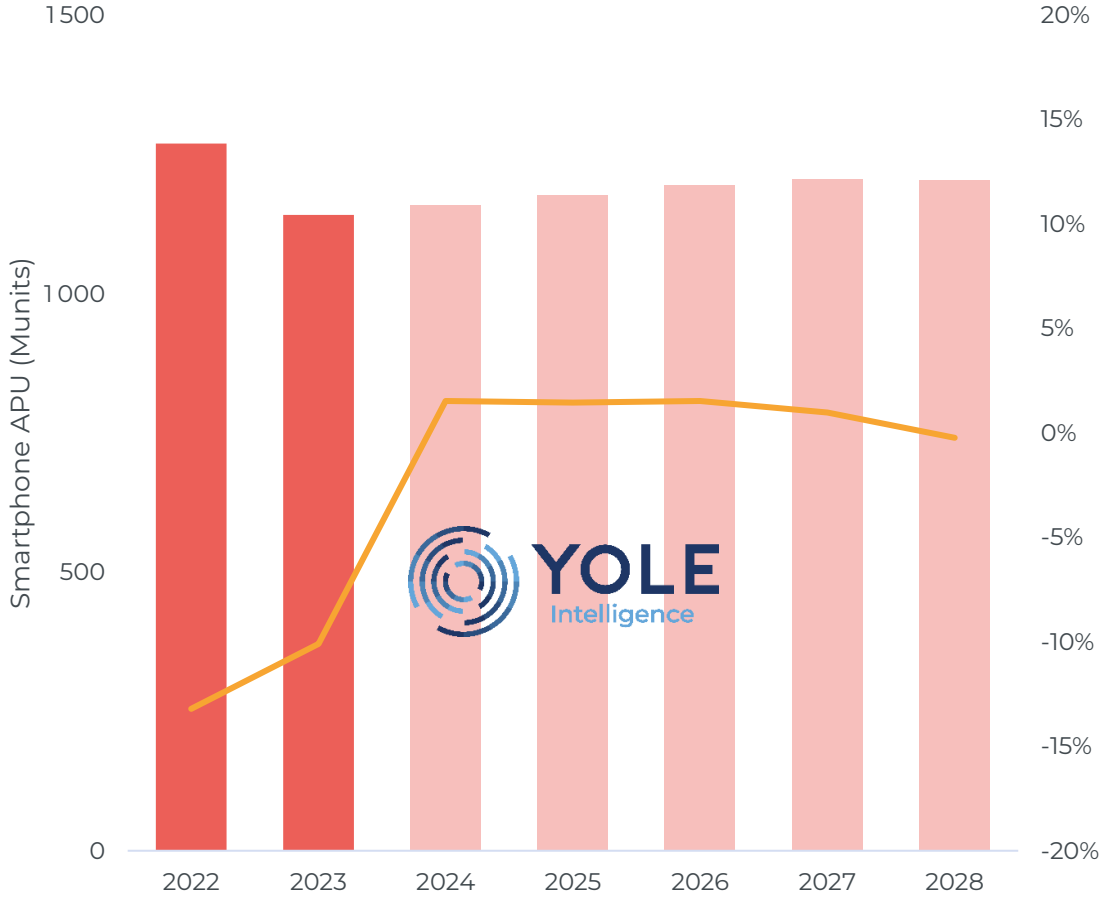
- SMARTPHONE APU MARKET
- SMARTPHONE APU PACKAGING MARKET
- SMARTPHONE POP TECHNOLOGY
- FAN-OUT TECHNOLOGY PHYSICAL ANALYSIS
- FAN-OUT PACKAGING MARKET
- TECHNOLOGY AND MARKET DRIVERS
- PACKAGING COMPARISON
- SoC COST ANALYSIS

SMARTPHONE APU MARKET

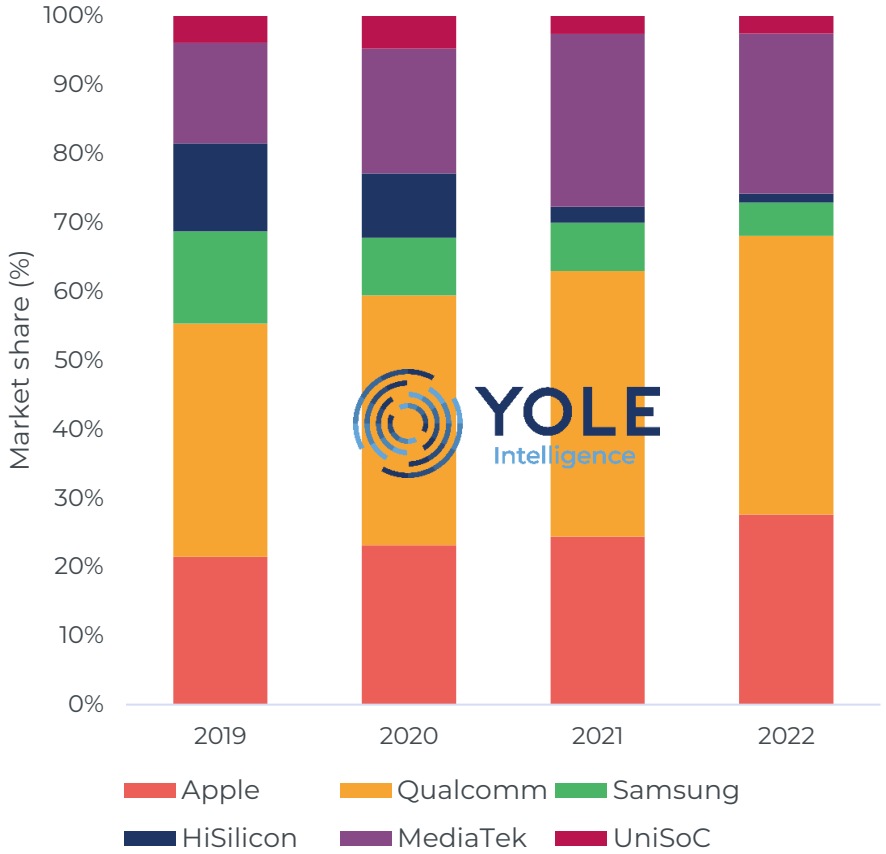
Qualcomm, Apple and Mediatek are the main smartphone APU designers.

Smartphone market is expcted to remain stagnant in the next years.

Smartphone APU Units Forecast (Munits)

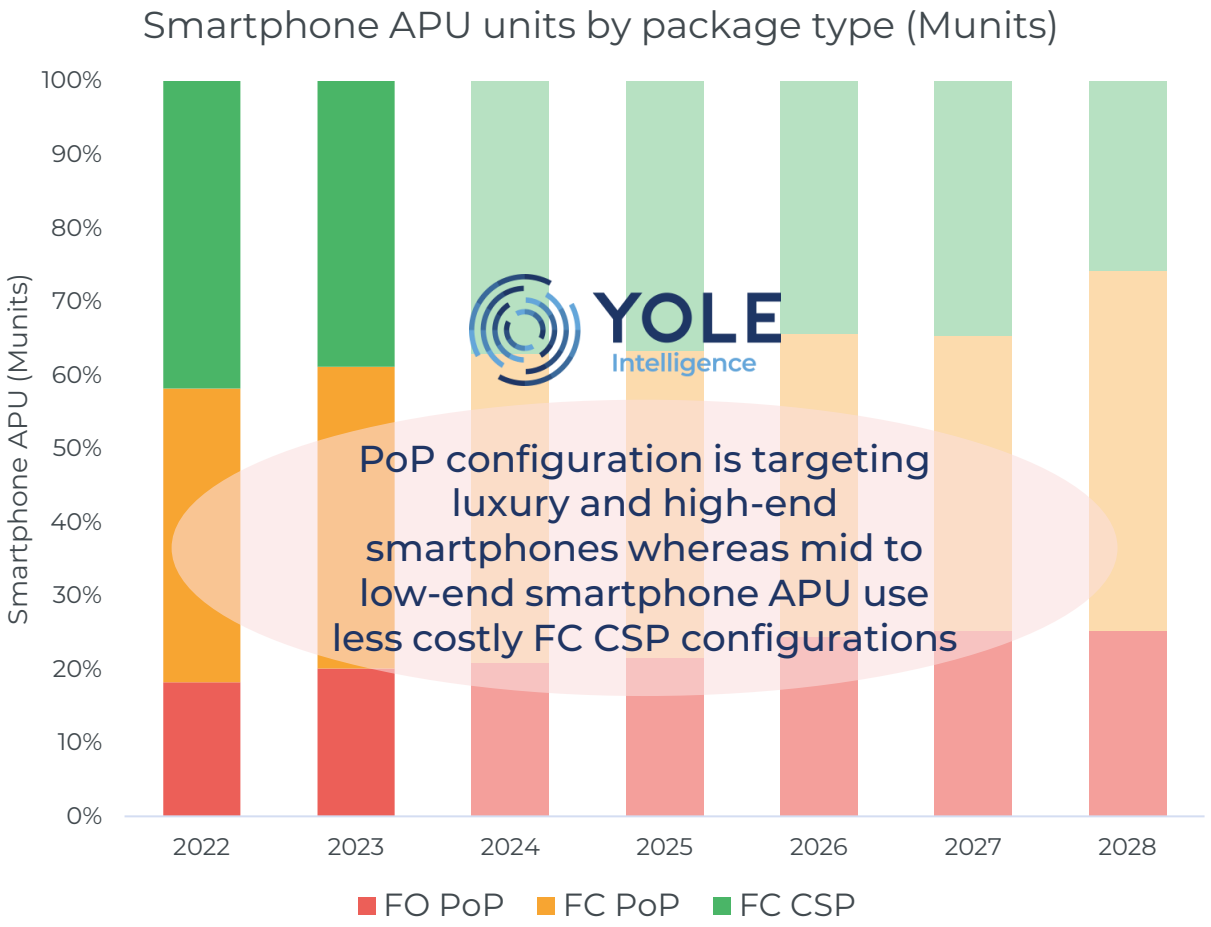


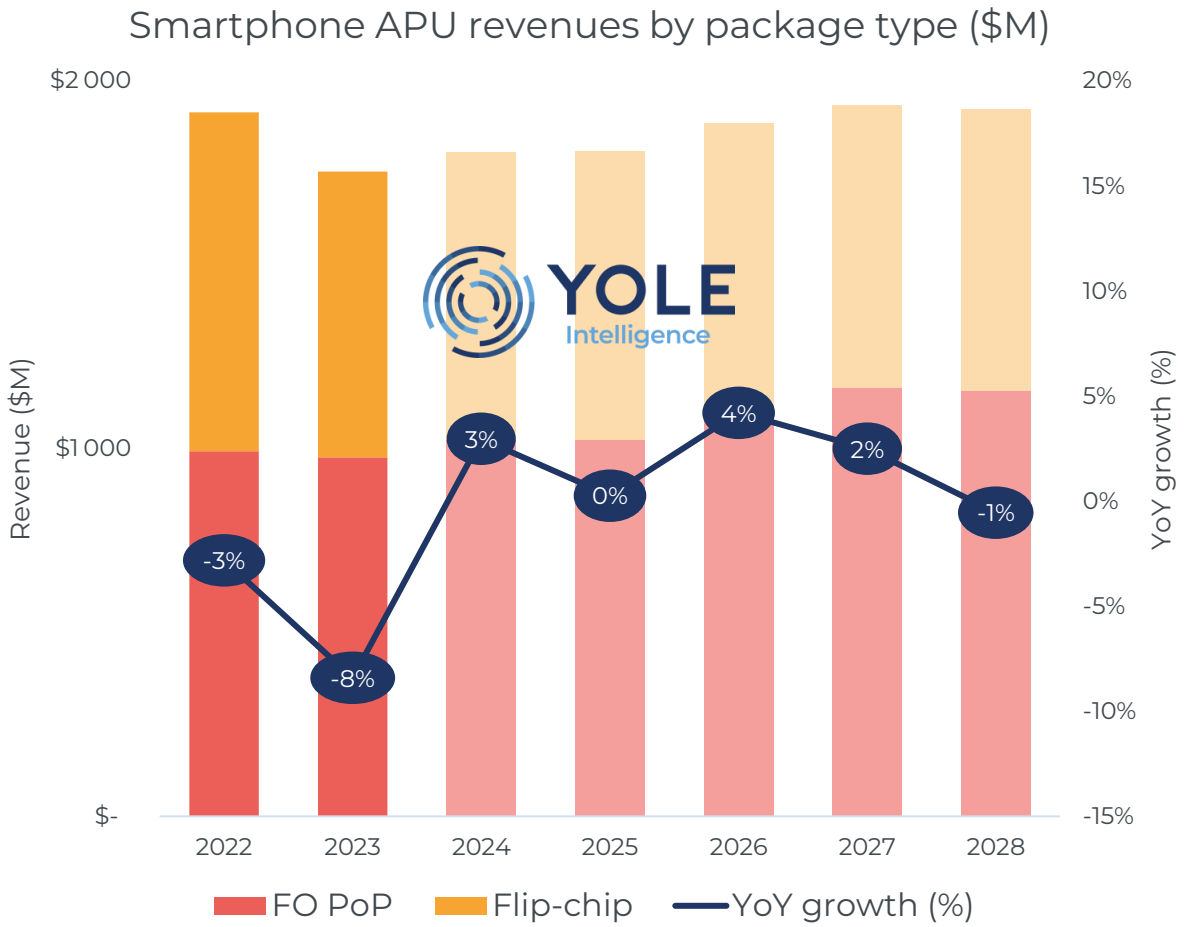
Smartphone APU revenue market share by APU designer (% | $B)



Source: Processor Monitor Q4 2023, Yole Group

SMARTPHONE APU PACKAGING MARKET





Source: Advanced Packaging Monitor Q4 2023, Yole Group

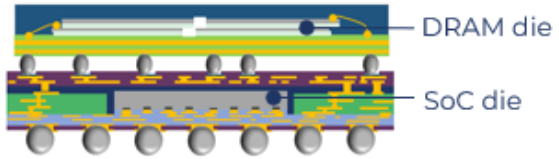
SMARTPHONE POP TECHNOLOGY

InFO PoP (tsmc)

Apple A16

FO-PLP PoP (SAMSUNG)

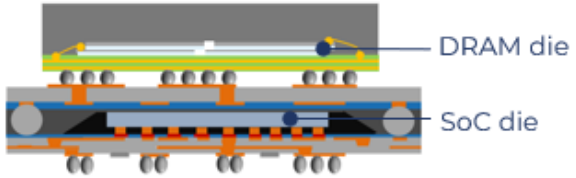
Google Tensor G2



Standard PoP (SAMSUNG OSAT)

Samsung Exynos 2100

Google Tensor G

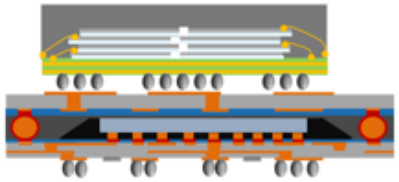


MCeP Advanced PoP BGA Packaging (SHINKO OSAT)

MediaTek Dimensity 9200

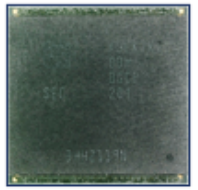
Qualcomm Snapdragon 8 Gen 2

HiSilicon Kirin 9000



MCeP-like + standard PoP (SAMSUNG)

Samsung Exynos 2200



FAN-OUT TECHNOLOGY FOR HIGH-END SMARTPHONE

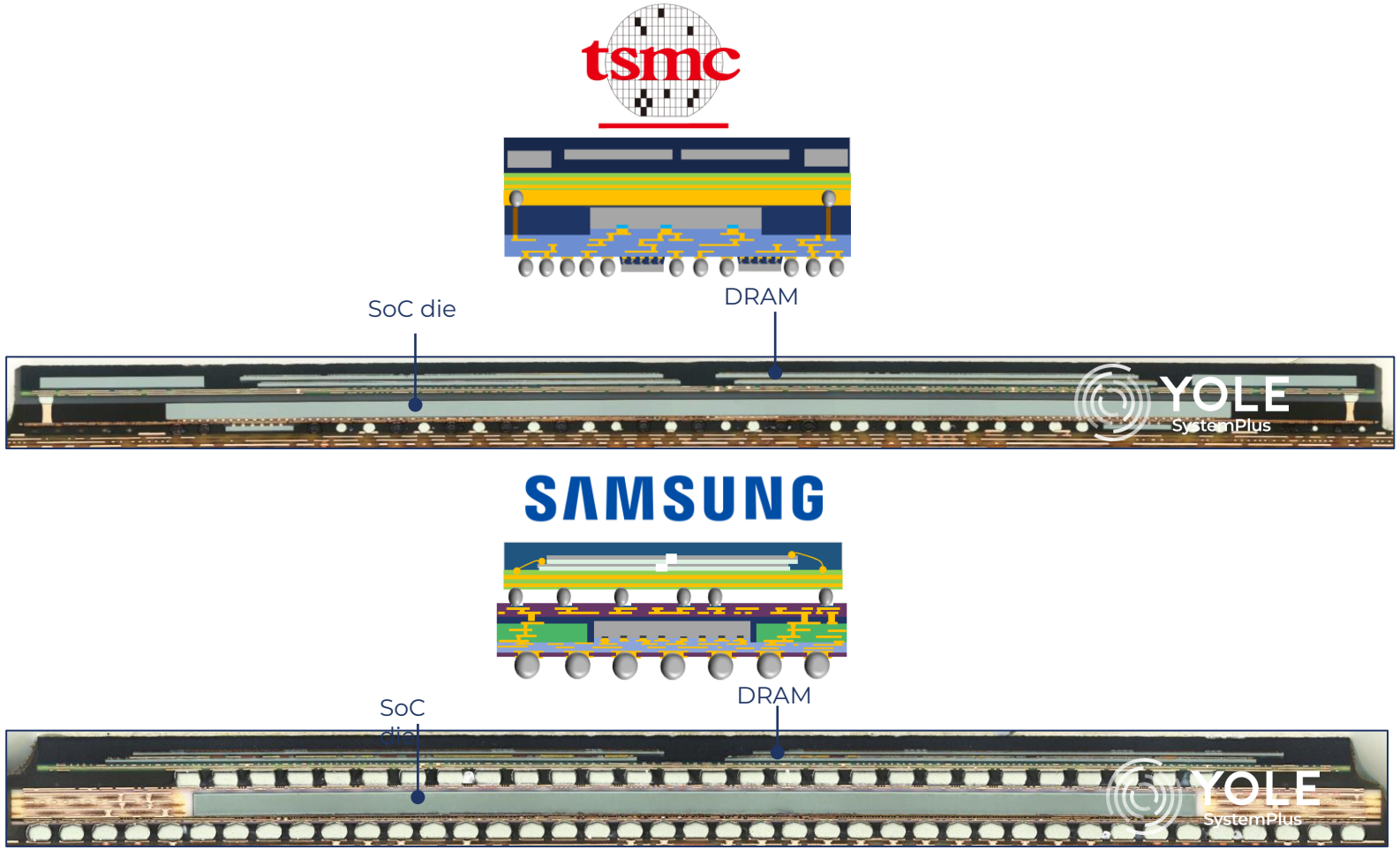
Fan-Out technology for high-end smartphone SoC assembly

TSMC Integrated Fan-Out packaging (InFO).

- Enable good electrical & thermal performances for 3D wafer level package.

Samsung Fan-Out Panel Level Packaging (FO-PLP)

- Realize the efficient power consumption
- Good thermal dissipation



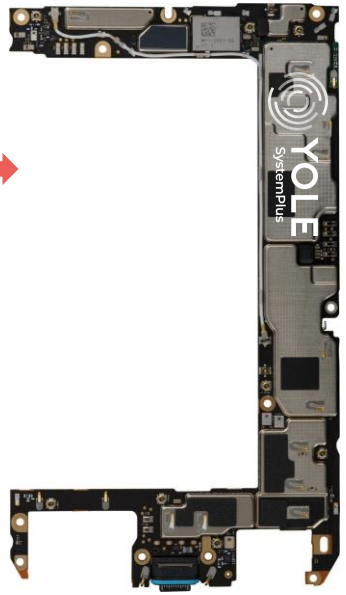
Samsung FO-PLP Package Cross-section – Optical View

FAN-OUT TECHNOLOGY FOR HIGH-END SMARTPHONE

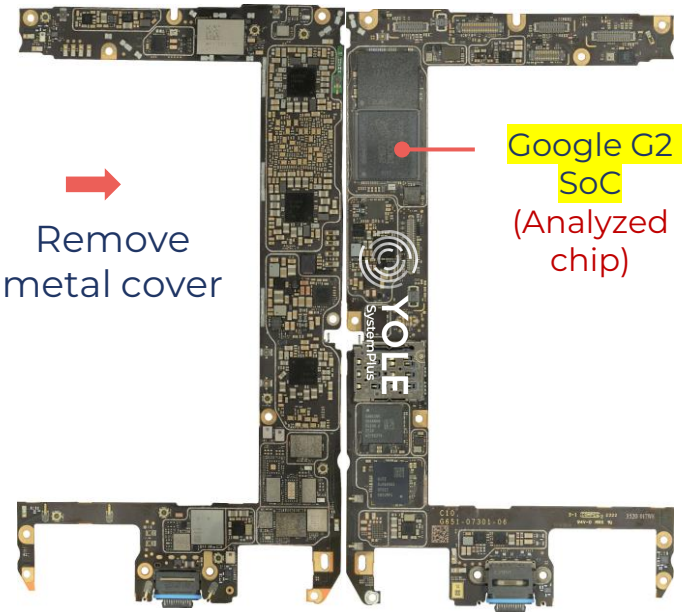
Goggle Pixel 7 Pro Smartphone Dismantle

Google Pixel 7 Pro Smartphone
©2023 by Yole SystemPlus

Google Pixel 7 Pro Smartphone Opening
©2023 by Yole SystemPlus



Remove metal cover



Google G2 SoC (Analyzed chip)

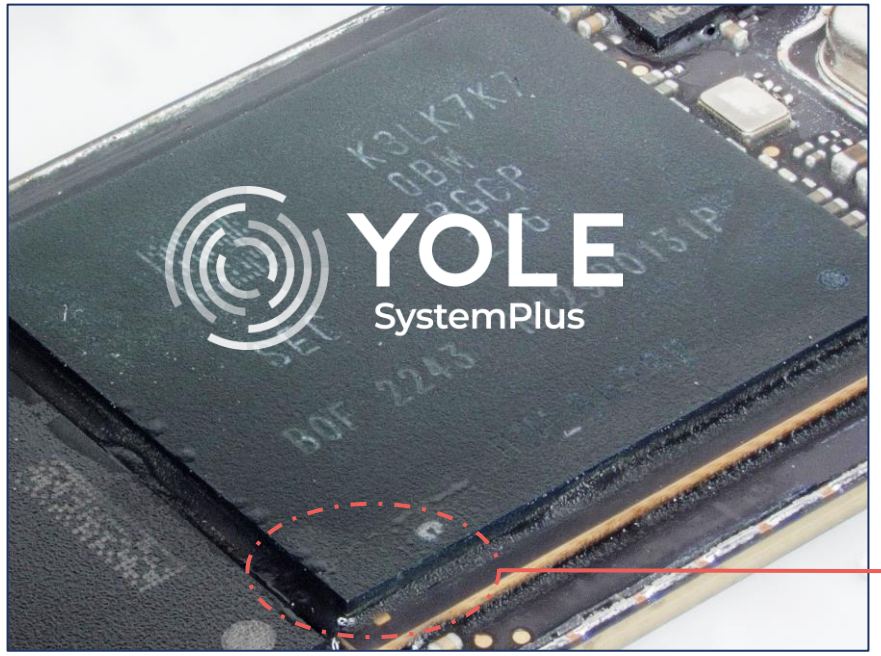
Main Board
©2023 by Yole SystemPlus

Google Tensor G2 SoC Package

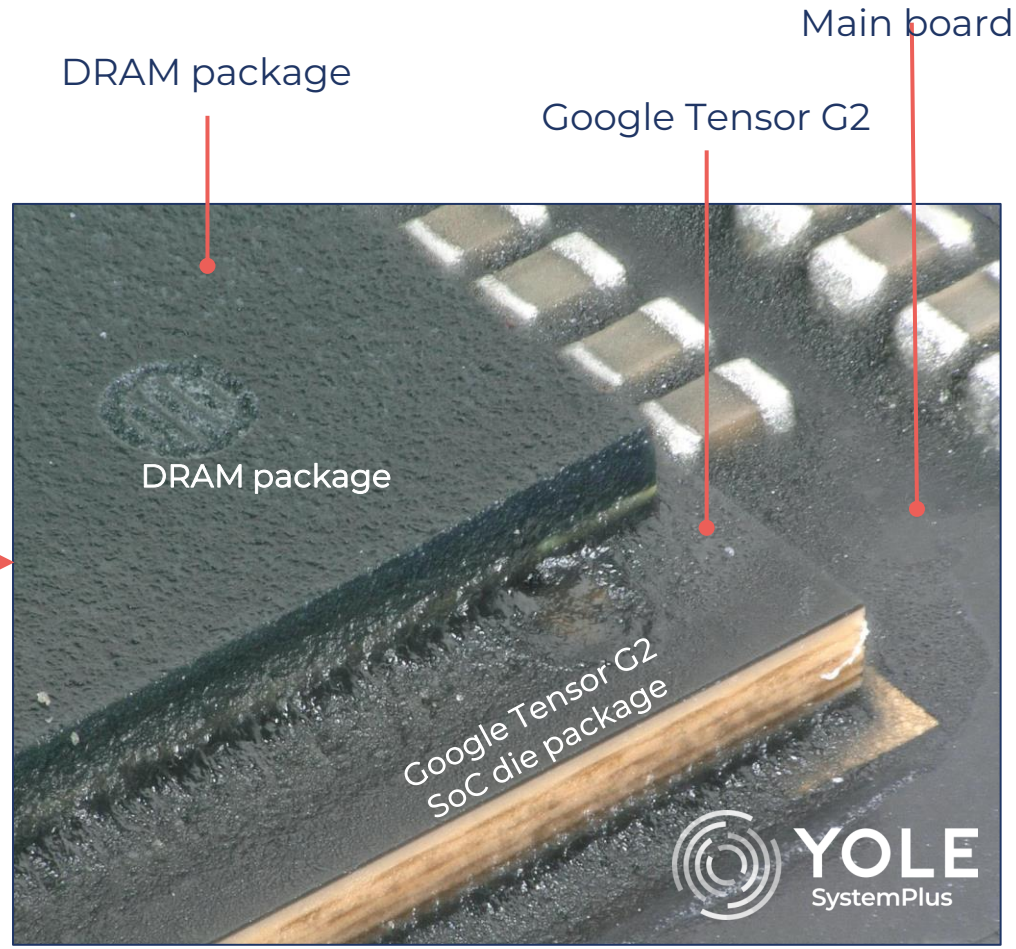
Source: *Samsung FO-PLP for Google Pixel 7 Tensor G2 SoC, Yole Group*

FAN-OUT TECHNOLOGY FOR HIGH-END SMARTPHONE

Google Tensor G2 soc Package



Google Tensor G2 SoC Package Frontside – Optical View



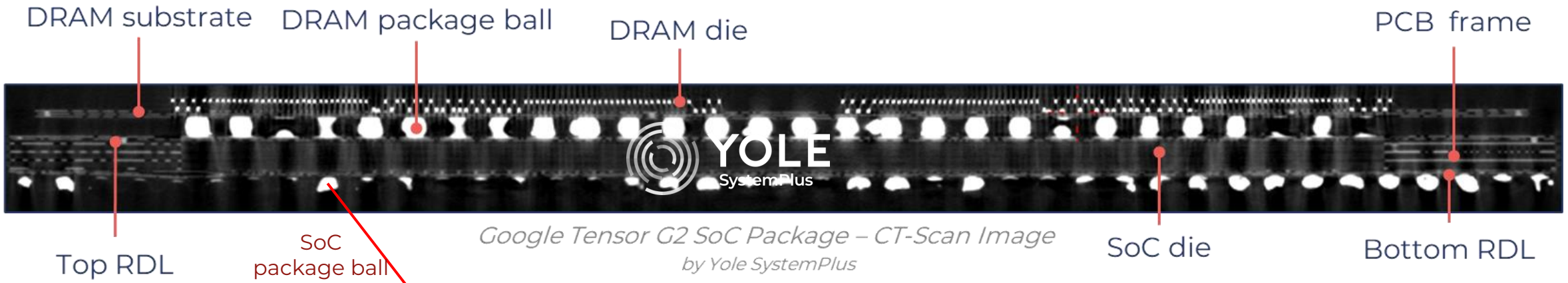
SoC Package Sideview – Optical View

- The DRAM package is stacked on the Google Tensor G2 SoC die package.
- The whole chip is assembled with PoP (Package-on-Package) technology then integrated to the main board of smartphone.

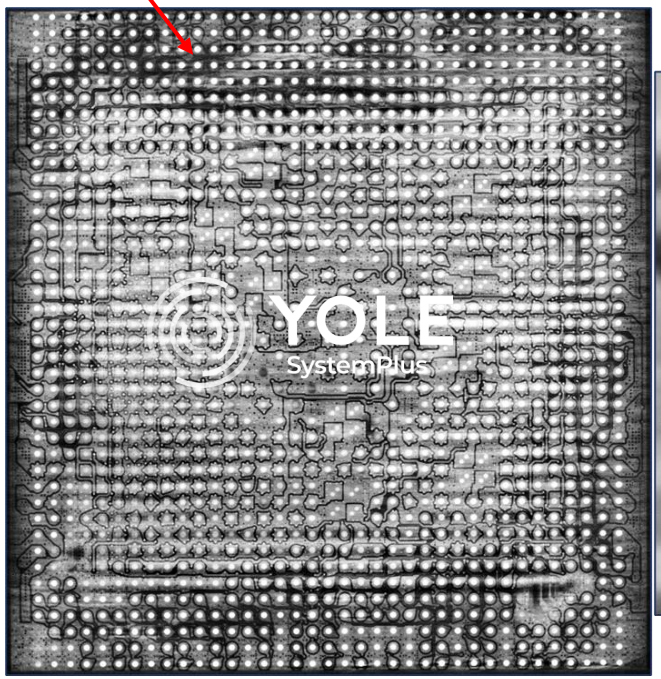
Source: Samsung FO-PLP for Google Pixel 7 Tensor G2 SoC, Yole Group

FAN-OUT TECHNOLOGY FOR HIGH-END SMARTPHONE

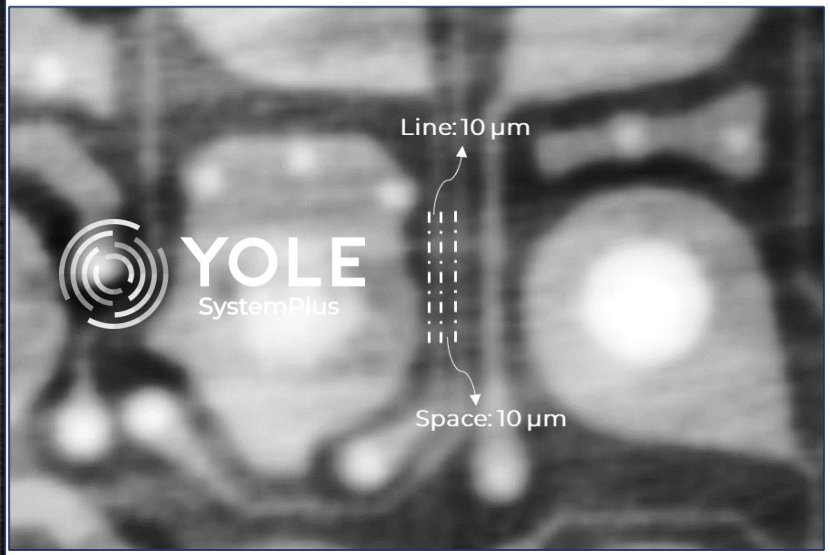
X-Ray images



Google Tensor G2 SoC Package – CT-Scan Image
by Yole SystemPlus



SoC Die Bottom RDL #3 – CT-Scan Image
by Yole SystemPlus

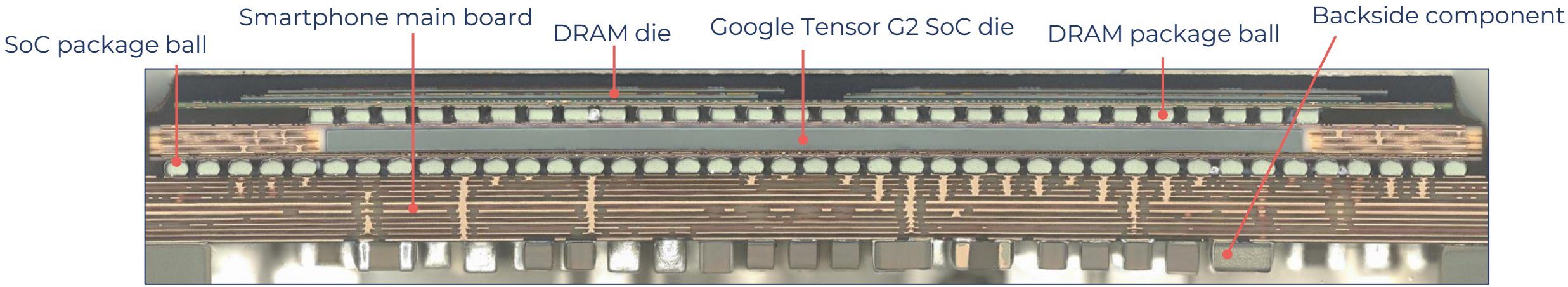


Source: *Samsung FO-PLP for Google Pixel 7 Tensor G2 SoC, Yole Group*

FAN-OUT TECHNOLOGY FOR HIGH-END SMARTPHONE

Package Cross Section

Package Frontside Cross Plan
by Yole SystemPlus

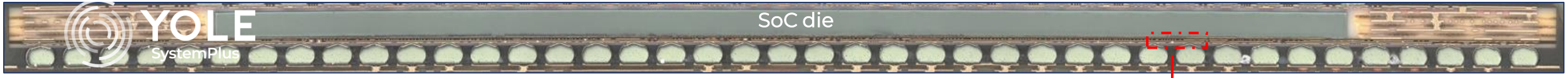


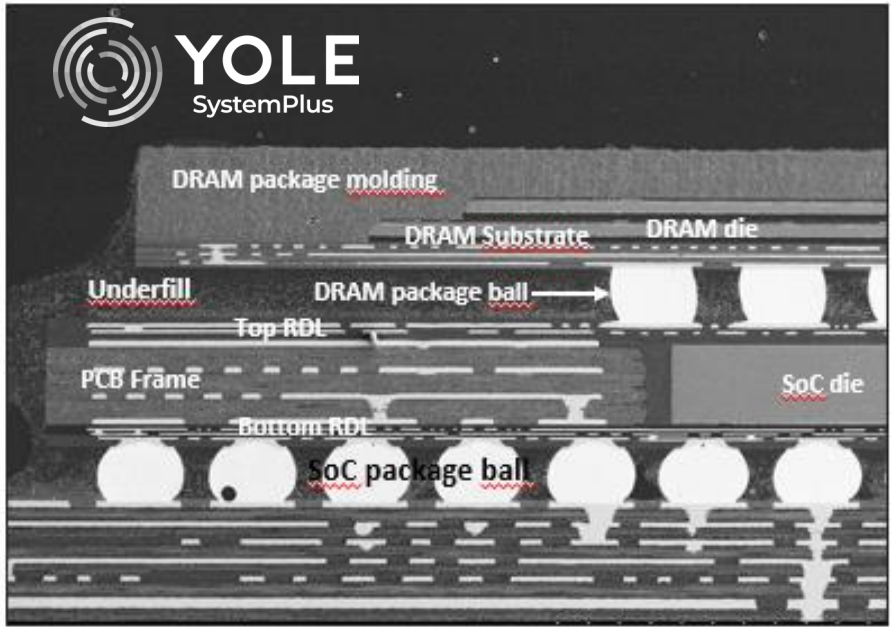
Package Cross-section – Optical View
by Yole SystemPlus

Source: *Samsung FO-PLP for Google Pixel 7 Tensor G2 SoC, Yole Group*

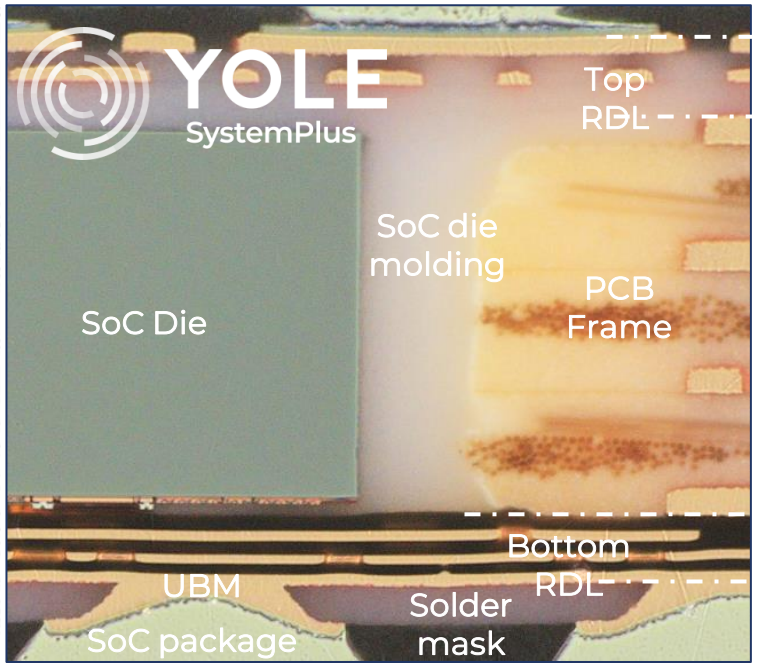
FAN-OUT TECHNOLOGY FOR HIGH-END SMARTPHONE

Package Cross Section





Package Cross-section



SoC Die Package Cross-section

Package Cross-section

Source: Samsung FO-PLP for Google Pixel 7 Tensor G2 SoC, Yole Group

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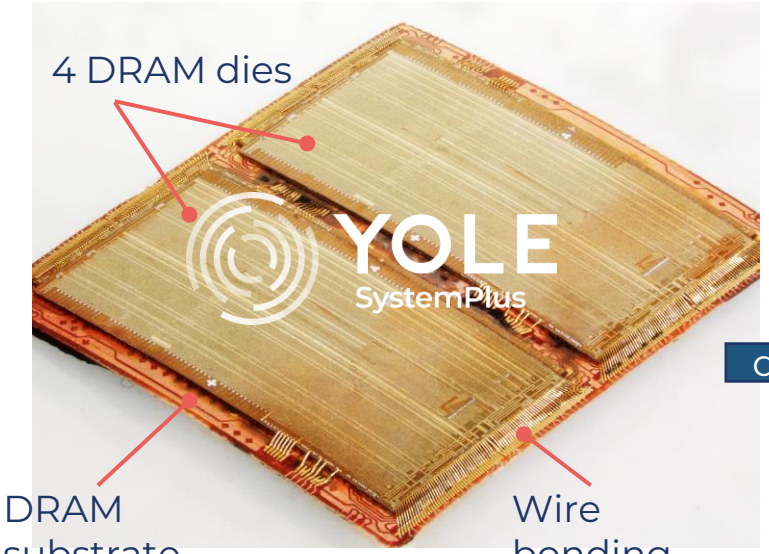
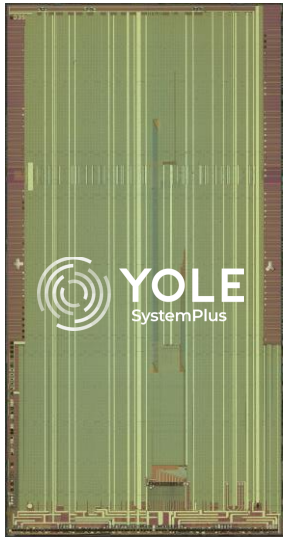
FAN-OUT TECHNOLOGY FOR HIGH-END SMARTPHONE

DRAM



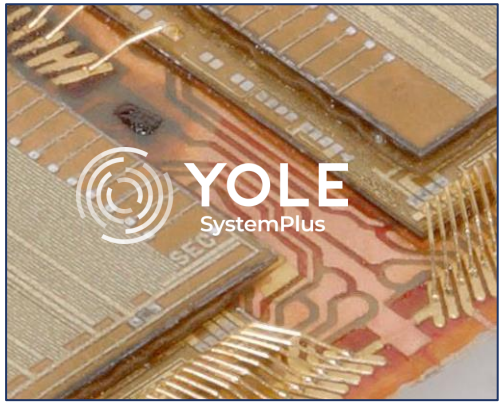
DRAM Package Opening

dismantle



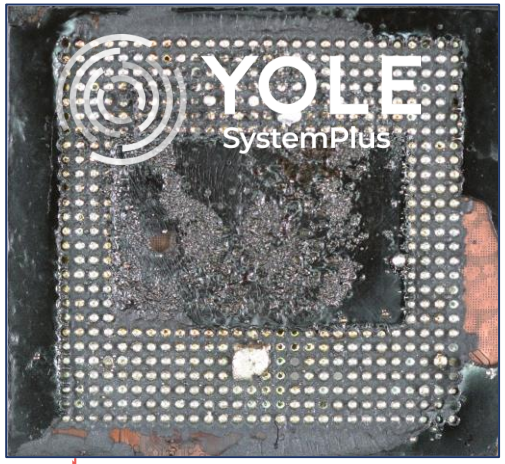
LPDDR5X DRAM Die

- Package opening reveals 4 DRAM dies.
- Wire bonding
  - Material: Gold wire
  - Wire number total: 384
  - Wire number per die: 96
  - Wire diameter: 19 µm
  - Wire average length: 400 µm



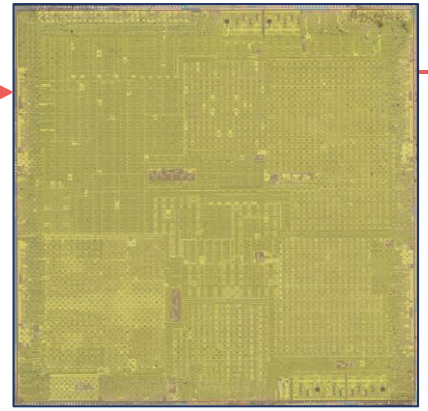
FAN-OUT TECHNOLOGY FOR HIGH-END SMARTPHONE

SoC Die



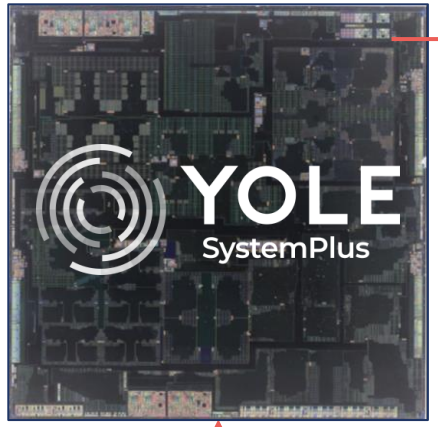
SoC Die Package

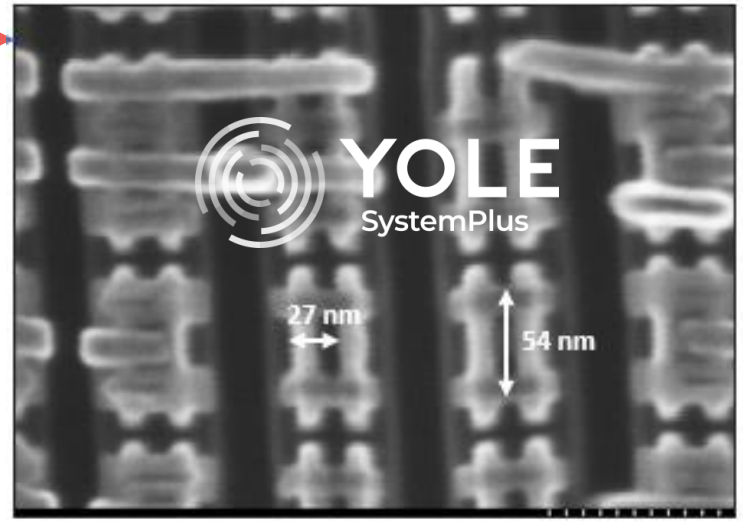
Remove substrates



Remove metal layers

SoC Die Delayering





FinFET Transistors – SEM View

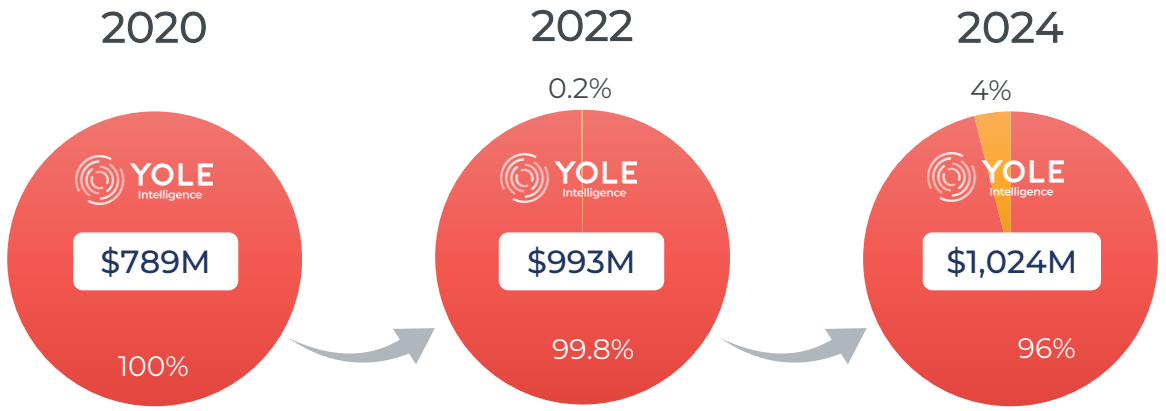
- The process uses FinFET transistors
- FinFET transistor:
  - Fin pitch: 27 nm
  - Gate pitch: 54 nm
- From the fin/gate pitch and public information, we assume the die is manufactured by using Samsung 5nm FinFET technology.

Source: Samsung FO-PLP for Google Pixel 7 Tensor G2 SoC, Yole Group

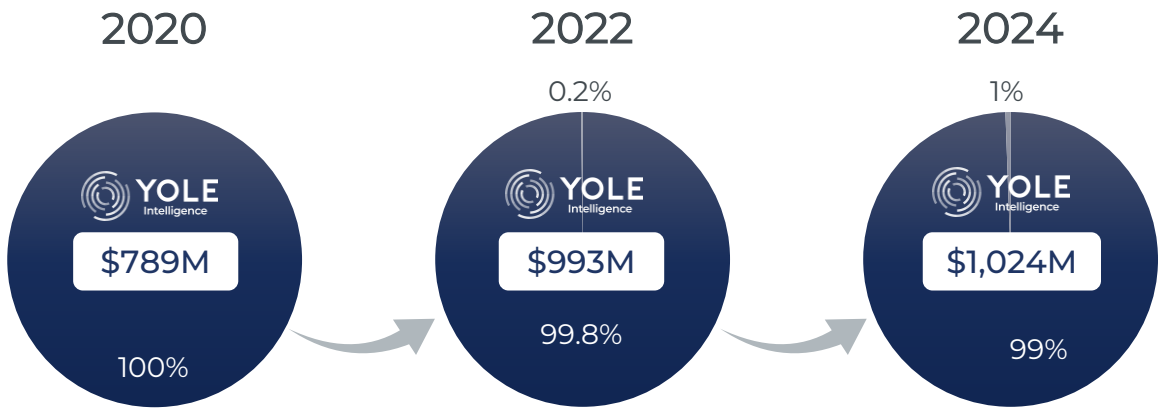
FAN-OUT PACKAGING MARKET

FO Packaging market trend evolution

Fan-out package supplier market share (%)



Carrier type market share (%)



2016: TSMC starts HVM of InFO_PoP for Apple's A-series APUs.

...

2022: Samsung supplies Google with its FOPLP packaging technology.

2024: Samsung adopts its FOWLP technology for Exynos 2400 APU.

> 2024: Qualcomm, MediaTek and HiSilicon can potentially adopt fan-out WLP/PLP technology on its smartphone APUs

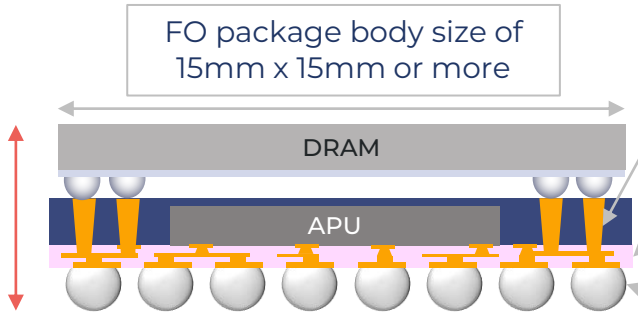
Sources: Advanced Packaging Monitor Q4 2023, Yole Group
Fan-Out Packaging 2023, Yole Group

TECHNOLOGY AND MARKET DRIVERS

FO Packaging technology trend and cost

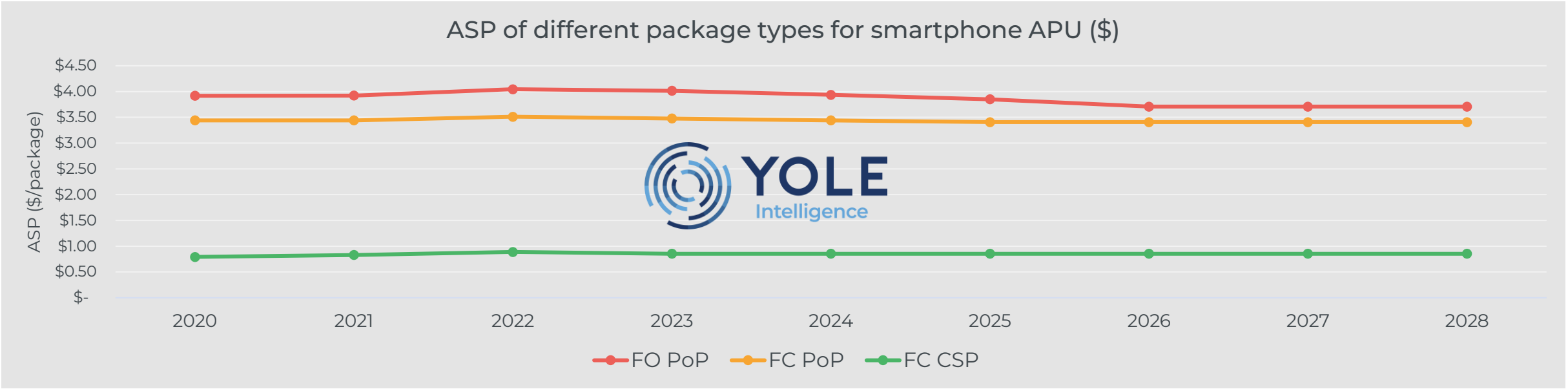
Why moving to a FO package?

A thin package is the main parameter of interest by eliminating the substrate



- Through-mold-vias (TMVs) to get through the package
- Three or more RDLs. With min. L/S of 2/2µm possible providing higher interconnect density.
  Better signal integrity
  Better thermal performance – lower heat resistance
- High number of I/Os: over 1000

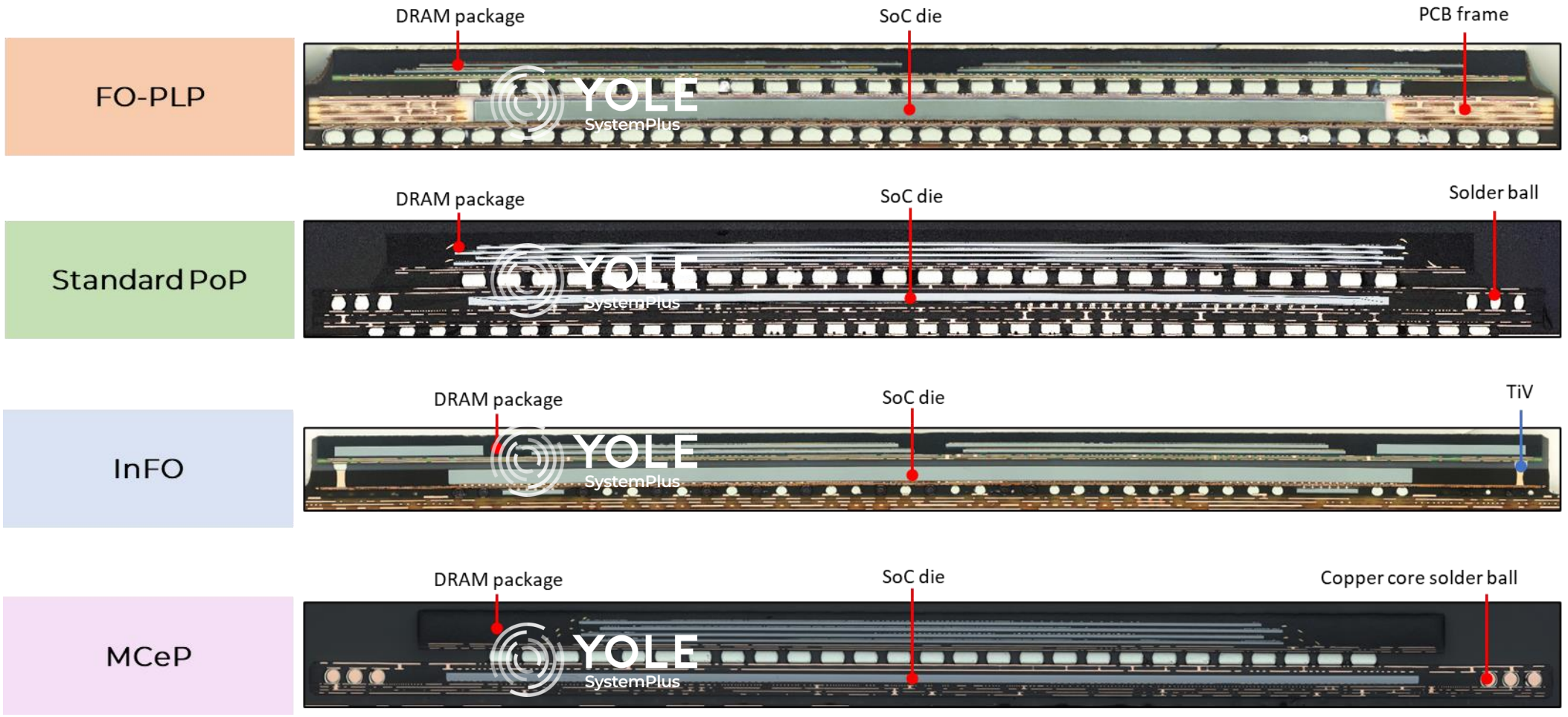
But… Is cost a problem?



Sources: Advanced Packaging Monitor Q4 2023, Yole Group
Fan-Out Packaging 2023, Yole Group

PACKAGING COMPARISON

High-End Smartphone PoP Technology

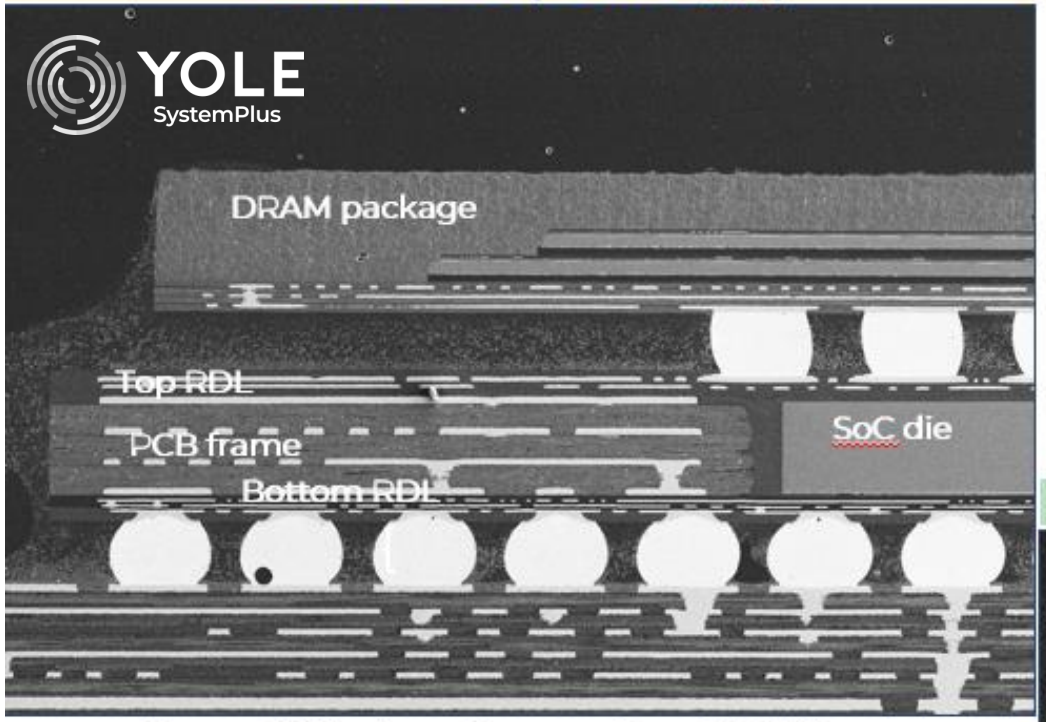


Source: Samsung FO-PLP for Google Pixel 7 Tensor G2 SoC, Yole Group

PACKAGING COMPARISON

Packaging Structure (FO_PLP PoP v.s. Standard PoP)

Tensor G2 SoC (FO_PLP PoP)

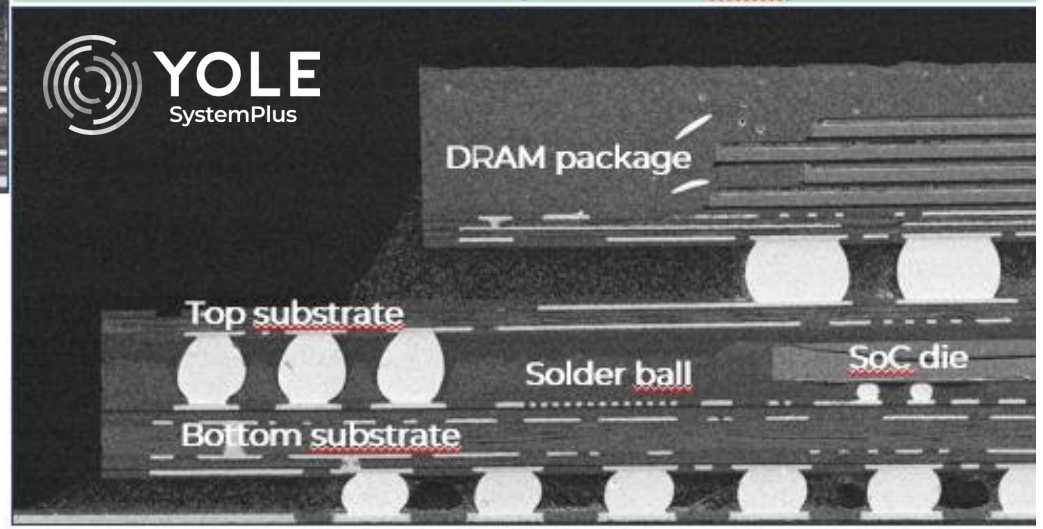


Tensor G2 Package Cross-section – SEM View
by Yole SystemPlus

- FO_PLP RDL minimum line/space: 7/10 µm
- Standard substrate minimum line/space: 15/15 µm

- In Standard PoP, the tin-based solder balls are used as the interconnect between top substrate and bottom substrate. The solder is slightly deformed during the reflow process.
- In FO_PLP PoP, the PCB frame has the same function as solder balls in Standard PoP but has no ball deformation issue.
- Compared to the top & bottom substrate of Standard PoP, the RDL in FO_PLP provides thinner package thickness.

Tensor G SoC (Standard PoP)

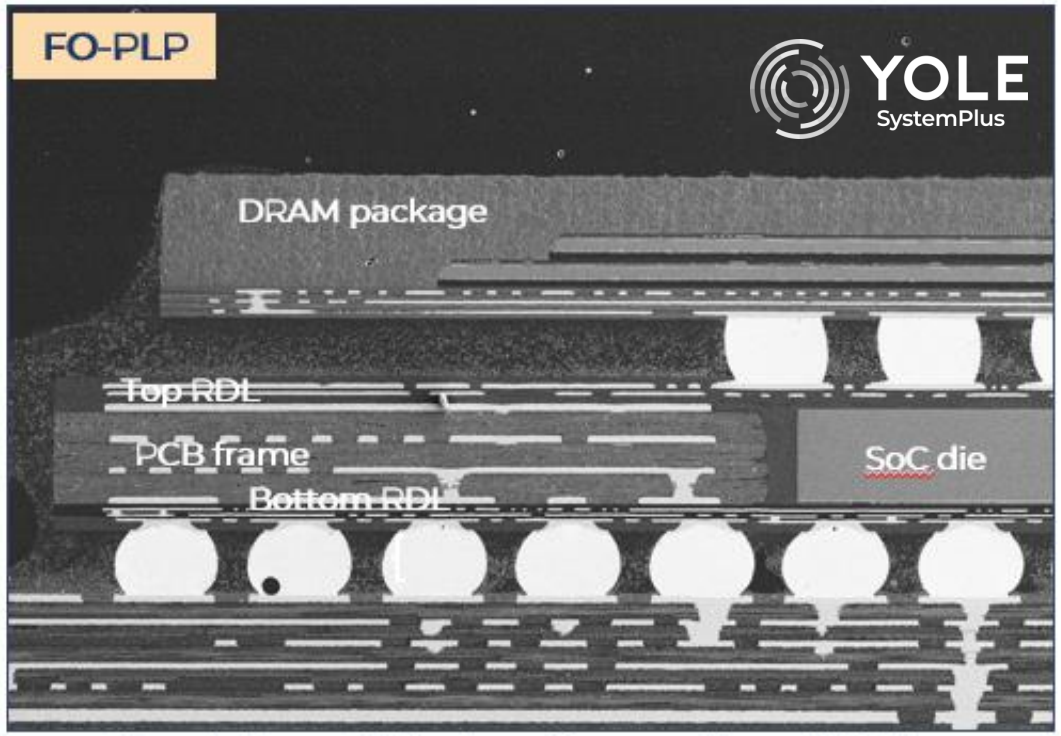


Tensor G Package Cross-section – SEM View

Source: Samsung FO-PLP for Google Pixel 7 Tensor G2 SoC, Yole Group

PACKAGING COMPARISON

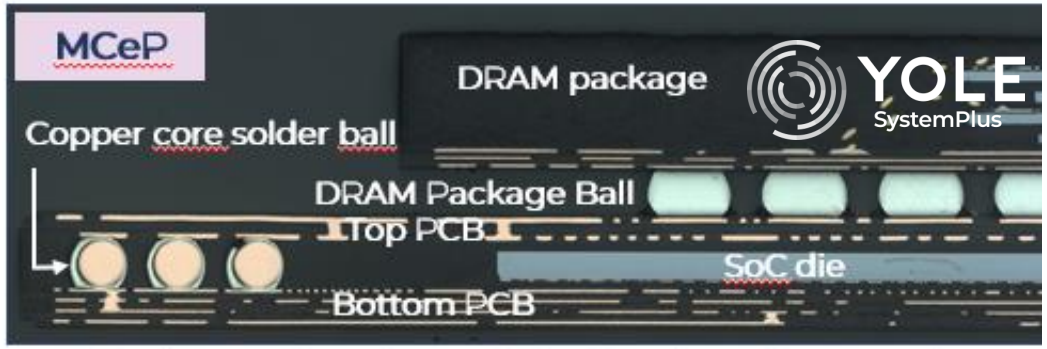
Packaging Structure (MCeP v.s. FO-PLP)



Google Tensor G2 Package Cross-section – SEM View

- In FO-PLP packaging structure, the PCB Frame has the same purpose with less copper material. Compared to MCeP's copper ball, the copper lines in PCB frame doesn't have deformation issue.
- The PCB frame height is 100 µm larger than the one of copper core solder ball. It allows to integrate thicker SoC die, which is assumed to have better mechanical reliability.
- MCeP (SD 8G1) min. Line/Space width: 14/14 µm
- FO-PLP (Google G2) min. Line/Space width: 7/10 µm

- In MCeP, copper core solder balls are used as the interconnect between top PCB and bottom PCB.
- The copper balls slightly shift during the reflow process.

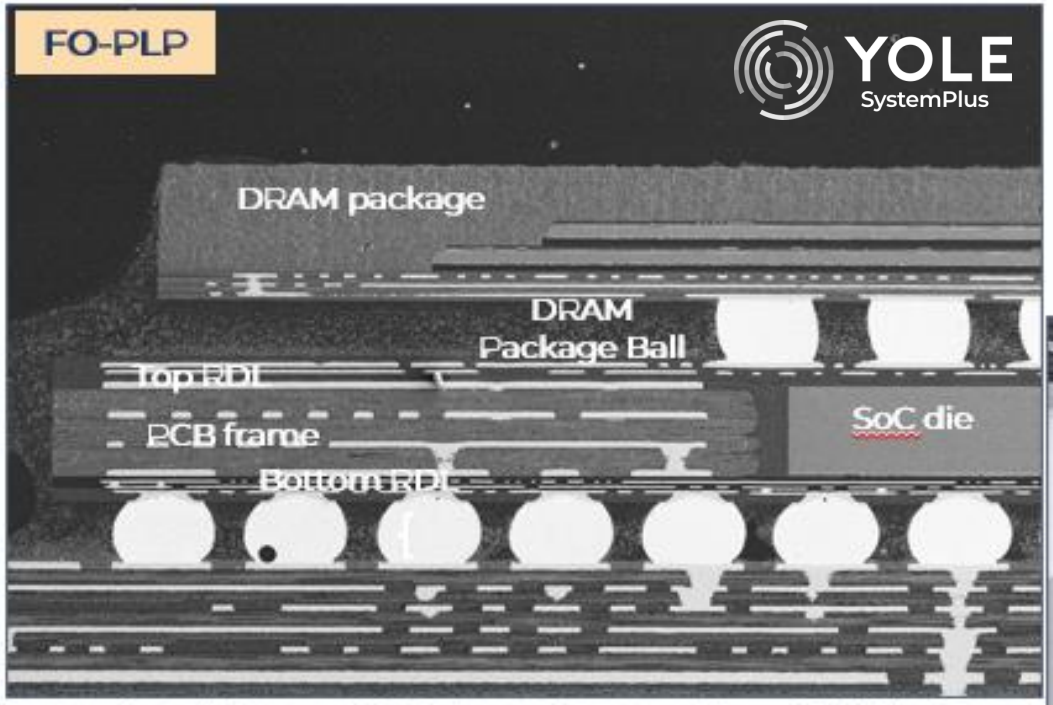


Qualcomm Snapdragon 8 Gen 1 Package Cross-section

Source: Samsung FO-PLP for Google Pixel 7 Tensor G2 SoC, Yole Group

PACKAGING COMPARISON

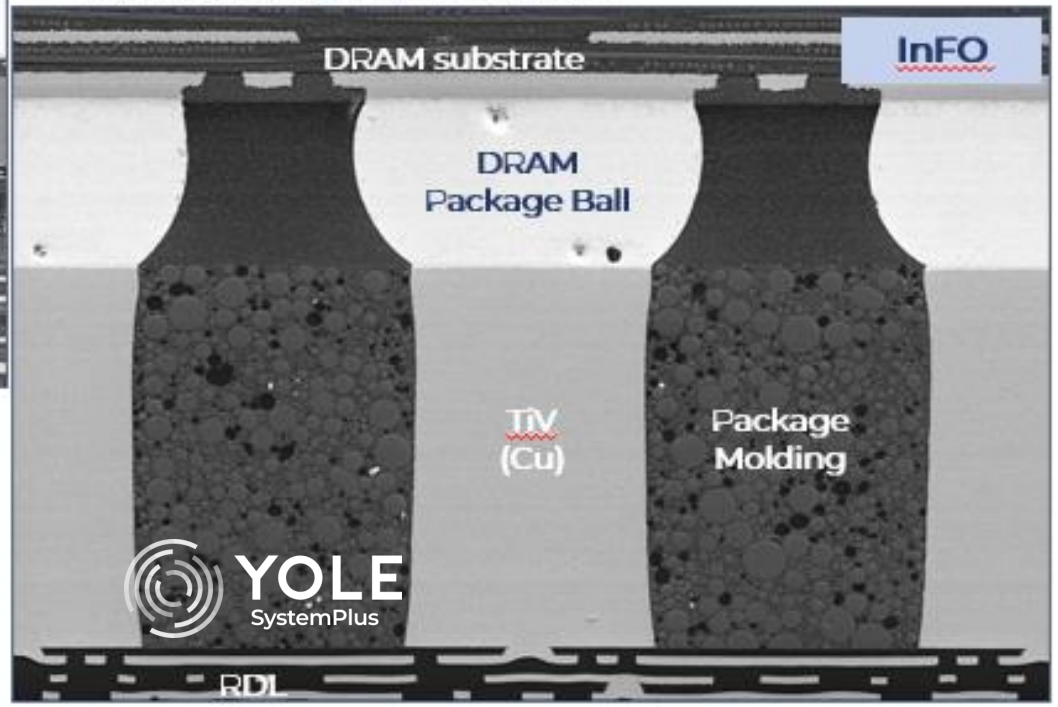
Packaging Structure (InFO v.s. FO-PLP)



Google Tensor G2 Package Cross-section – SEM View

- In InFO packaging, the TiV is used as an interconnect between DRAM package ball and RDL. There is no top routing between TiV and and DRAM package.
- Compared to MCeP, both TiV (InFO) and PCB frame (FO-PLP) have a solid structure without deformation during reflow process.

- The PCB frame takes more space compared to the TiV but allows an additional routing around the die. It functions more than a connection to the top component.
- By using top RDL, FO-PLP is able to match any pitch and also reroute signal in PoP configuration without using any interposer.



Apple A16 Package Cross-section – SEM View

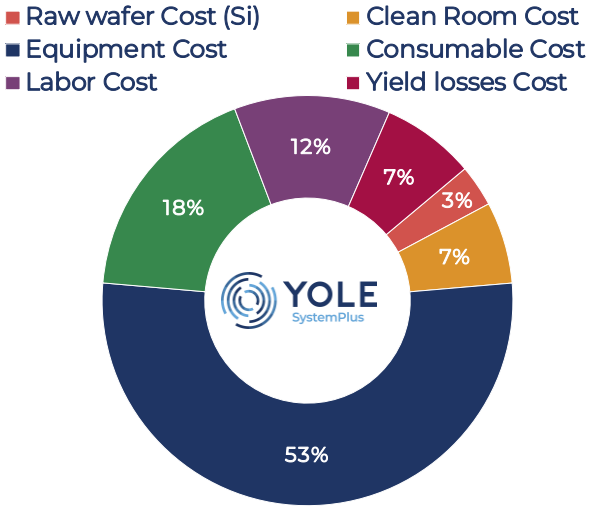
Source: Samsung FO-PLP for Google Pixel 7 Tensor G2 SoC, Yole Group

SOC COST ANALYSIS

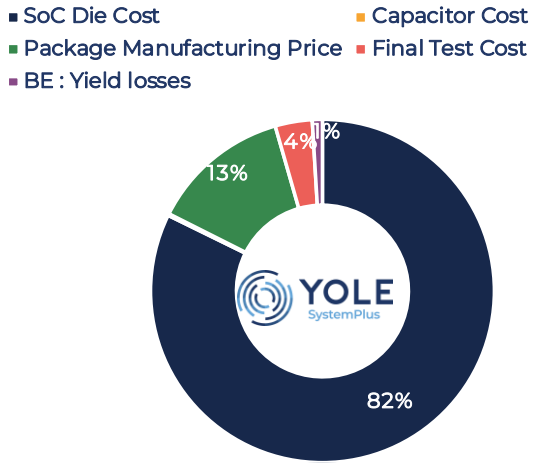
Google Tensor G2 system-on-chip (SoC) Cost Analysis

Source: *Samsung FO-PLP for Google Pixel 7 Tensor G2 SoC, Yole Group*

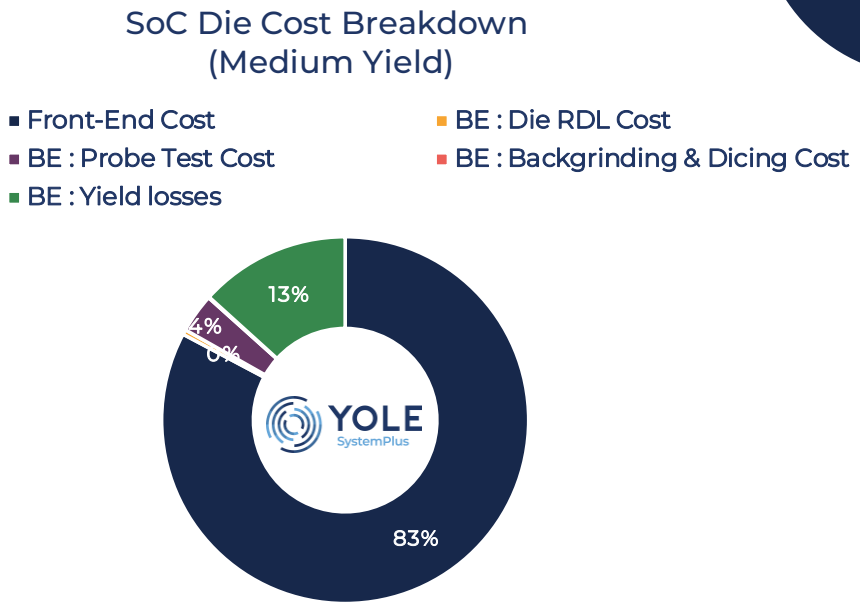
SoC Die Front-End Wafer Cost Breakdown (Medium Yield)



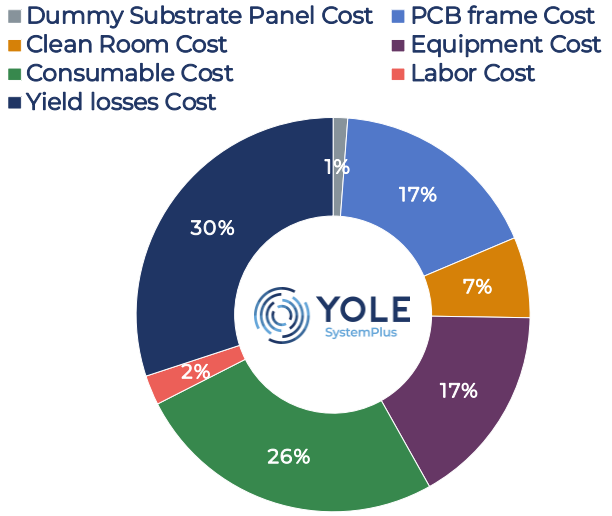
SoC Die Component Cost (Medium Yield)



SoC Die Cost Breakdown (Medium Yield)



SoC Die Packaging Cost Breakdown (Medium Yield)

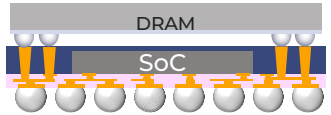


MORE ADOPTION OF FAN-OUT TECHNOLOGY… AND WHAT'S NEXT?

OSATs solutions

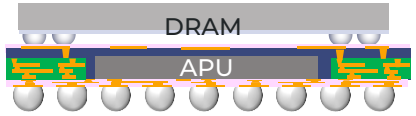
ASE GROUP · Amkor Technology · nepes · SPIL · Powertech Technology Inc. · JCET

InFO_PoP



2016 … 2022 2024

FOPLP



SAMSUNG Google

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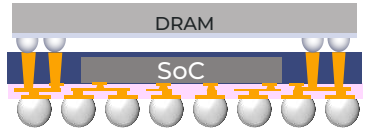


SAMSUNG

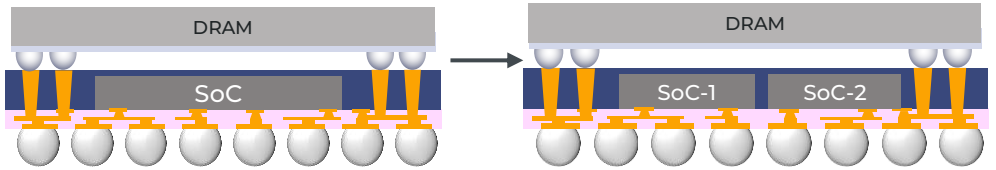
Chiplets?

Fan-out RDL interconnections are one approach to achieving high-density connections in die partitioning.
The use of chiplets in the mobile APU could result in several advantages:

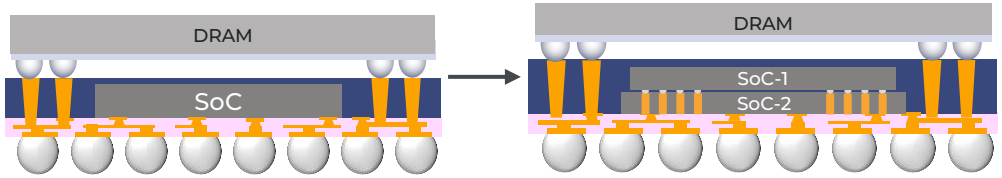
- Decrease the cost of the system
- Increase performance

Different approaches for integration

Side-by-side integration



3D Stacking
TSV + microbumps or Hybrid bonding



Source: Fan-Out Packaging 2023, Yole Group

Thank You for listening