Fraunhofer IZM

Fraunhofer Institute for Reliability and Microintegration IZM

High Density Organic Substrates for Chiplet Technologies

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20th IMAPS Device Packaging Conference

March 18 – 21, 2024 – Fountain Hills, Arizona

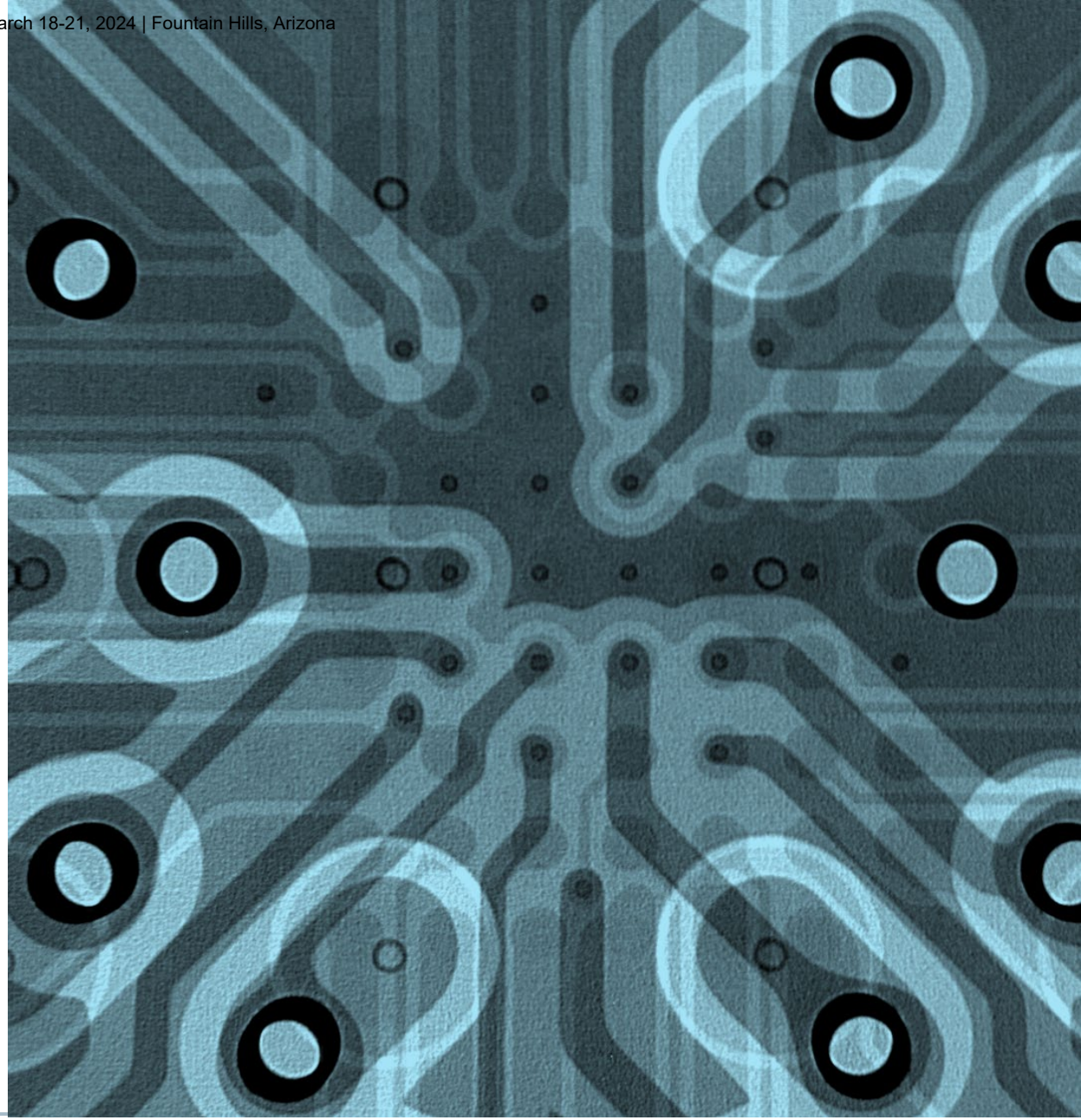
Outline

1. Introduction to High Density Substrates Technologies

2. Advanced Semi Additive (aSAP) - RDL Process
   - Overview
   - Vertical Interconnects - Via
   - Horizontal: Lithography, Plating, Strip & Etch

3. Process Control / Electrical Testing

4. Outlook & Summary

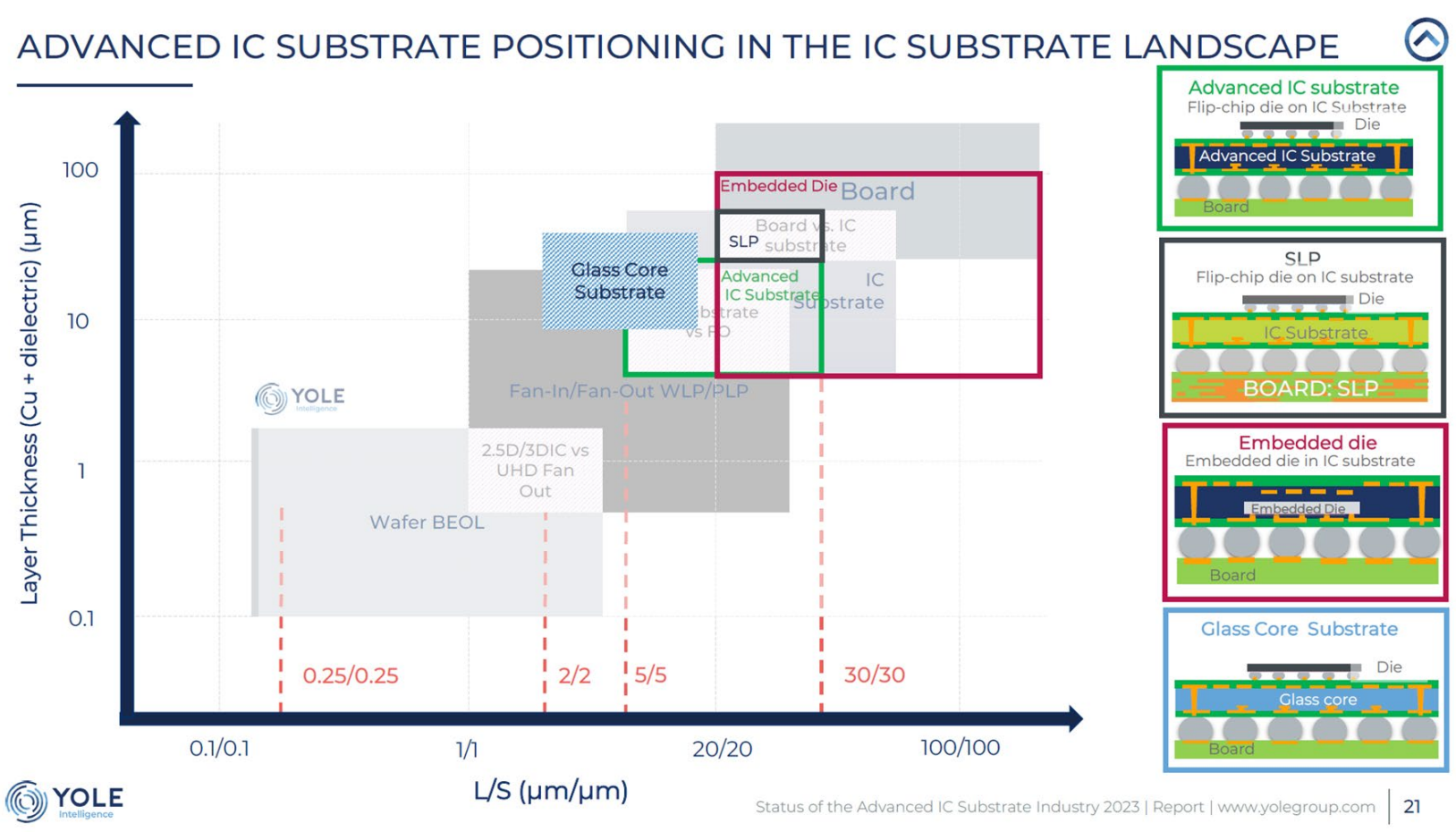


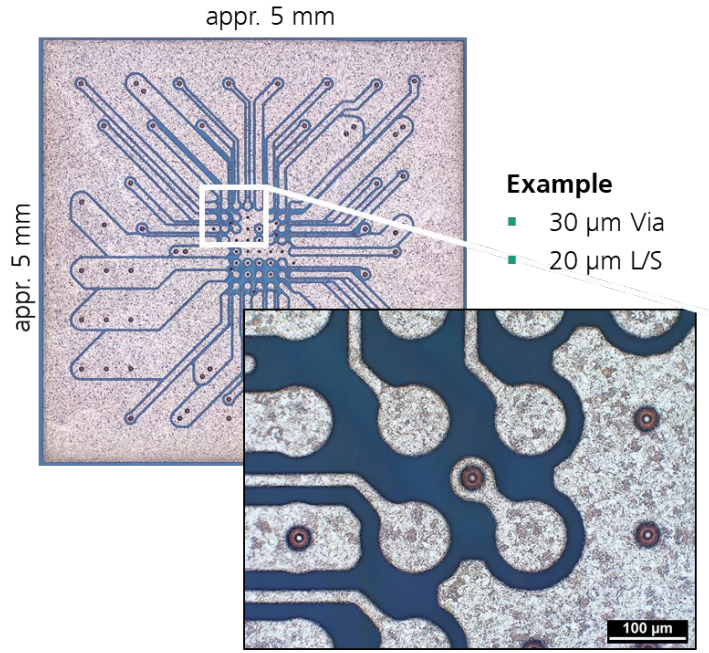
01

Introduction to High Density Substrates Technologies

Introduction Advanced Substrates Technologies

Landscape of Advanced Substrates

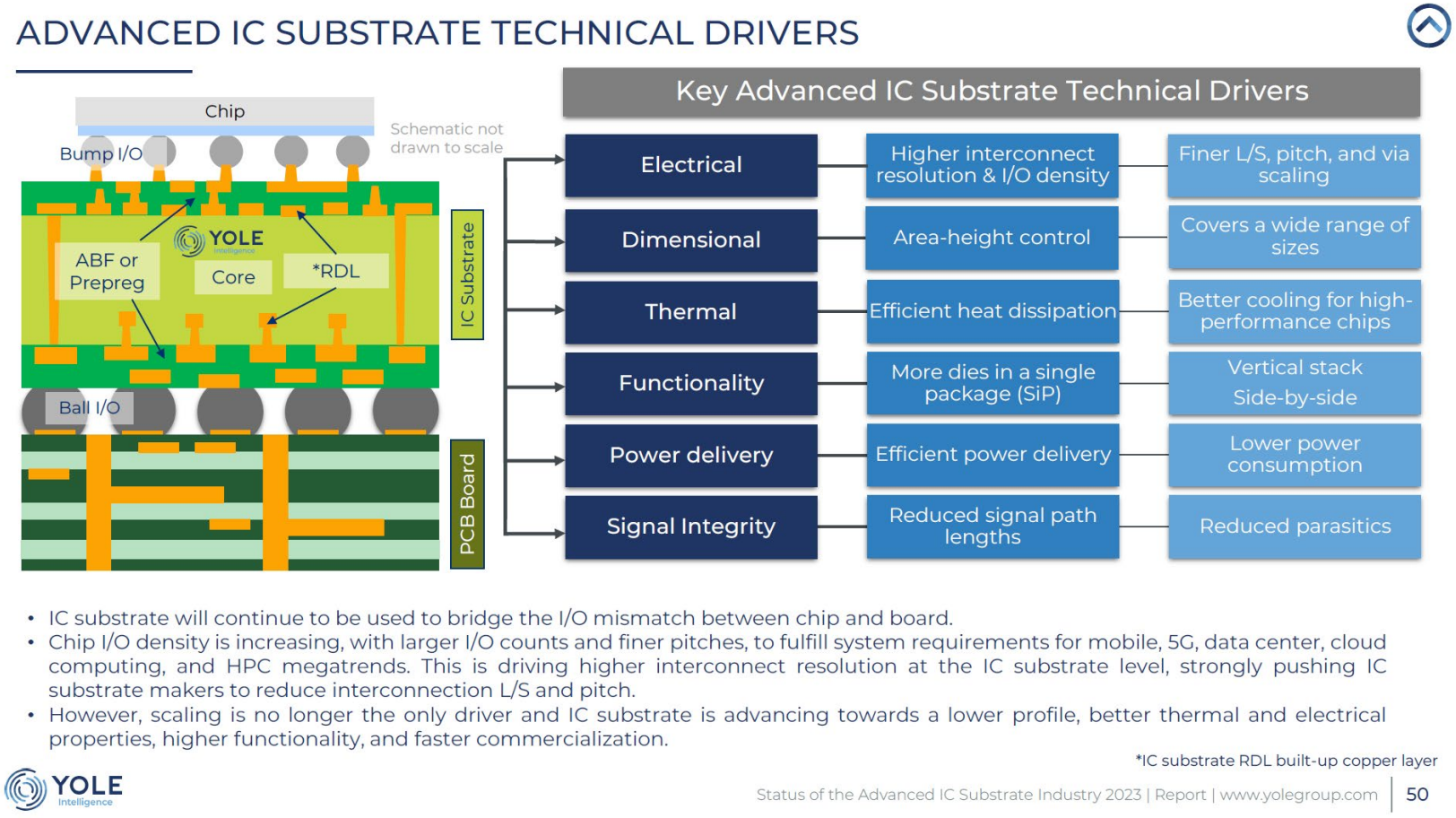




Source: Yole Status of the Advanced Substrate Industry 2023

Introduction Advanced Substrates Technologies

Drivers of Advanced Substrates



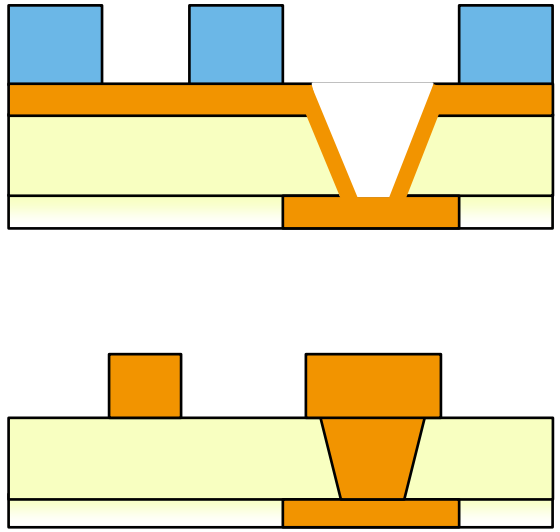
Source: Yole Status of the Advanced Substrate Industry 2023

Drivers

- Continuation of bridging the I/O mismatch between chip and board with increased demands on:
  - Pitch & wiring density
  - Thermal performance
  - Electrical performance / signal paths
  - Dimension

mSAP, SAP, aSAP - Panel technologies towards smaller line pitch

mSAP

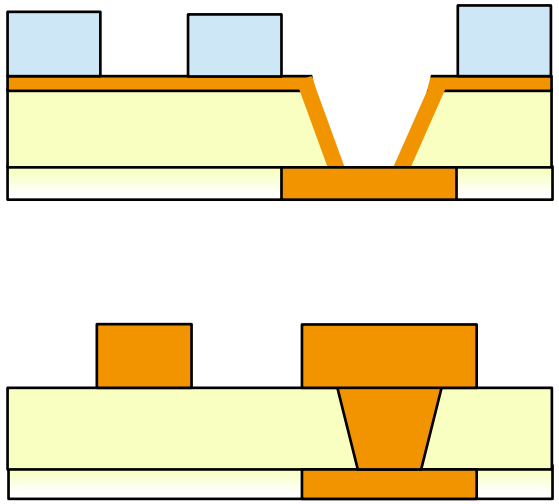


Cu clad base: 1.5 - 3µm

+ E-less Cu: 1 - 2 µm

L/S: > 20µm

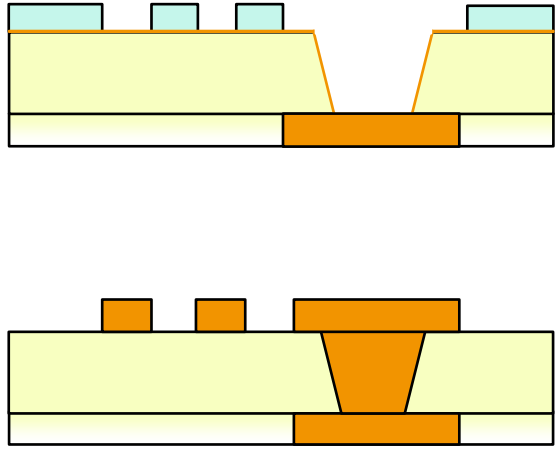
SAP



E-less Cu: 1 - 2µm

20µm - 10µm

aSAP

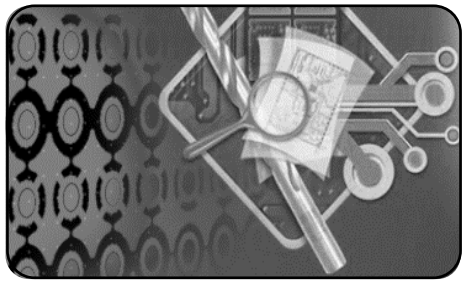


PVD Cu: 50 - 500nm

10µm - 5µm and below

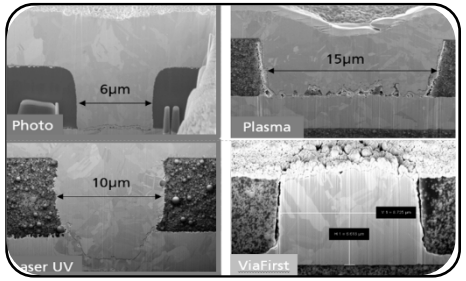
Advanced Substrates Technologies

Process Flow

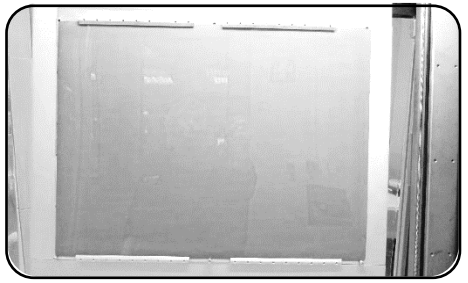


CAM & EDA

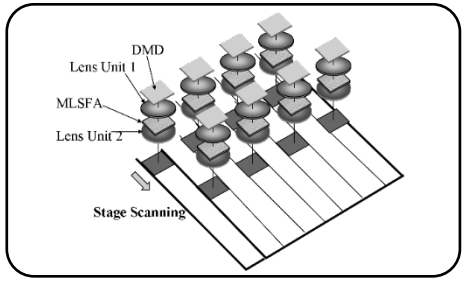
Dielectric



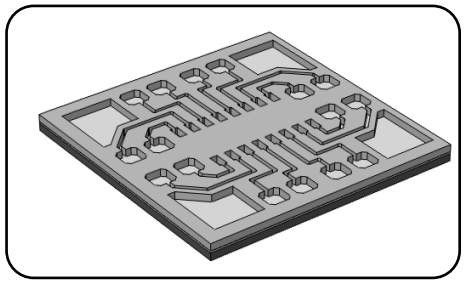
Via Formation



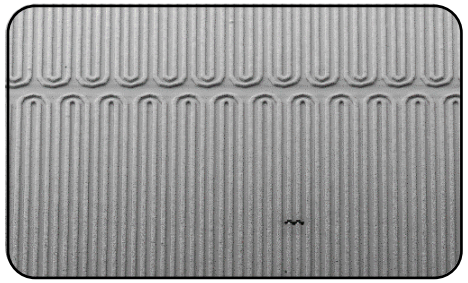
PVD



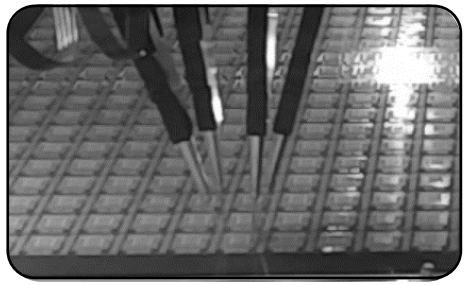
Resist + DI Litho.



Pattern Plating



Strip & Etch



Electrical test

IZM Panel Level Packaging Line

Process line for the production of IC substrates at the IZM – Nov. 2023

mech. Drill

Schmoll MX1

Etch

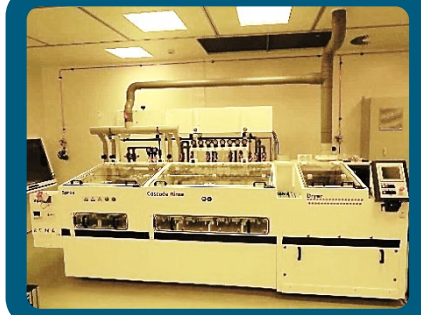
Schmid Combi Line

Laser Drill

Schmoll UV Picodrill

Cleanroom

Clean / Condition



RENA STR/DI

PVD Sputter

Creavac CMet600

VAC Lamination

Dynachem/ Lauffer

DI Image

- Schmoll MDI-ST Ultra 2µm
- Orbotech Paragon Ultra200

Cu Plate

- Semsysco VHSP
- Ramgraber

AOI

- Rudolph Firefly
- Impex proX3

E-Test

ATG A9+

Advanced Substrates Technologies

Material Options

Base Materials

- Organic: Ultra Low CTE CCL
- Glass: TGV Glass Core
- Epoxy Mold Compound - FOPLP

Dielectric Films

- Non-Photo dielectrics
- Photo-Imagable Dielectrics preferred in film format

Metal layer

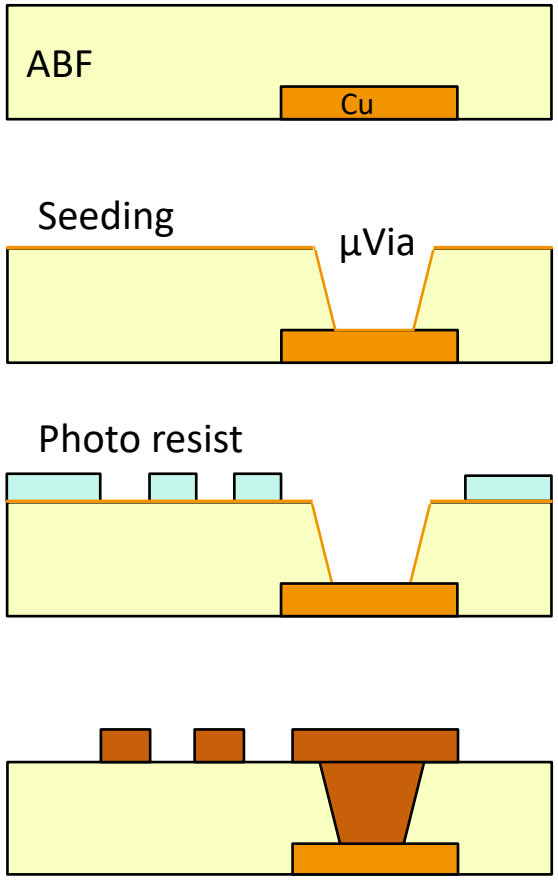
- PVD Seed layer: Ti/Cu
- RDL Lines: Electrolytic Cu
- Final Finish: ENiG, ..

02

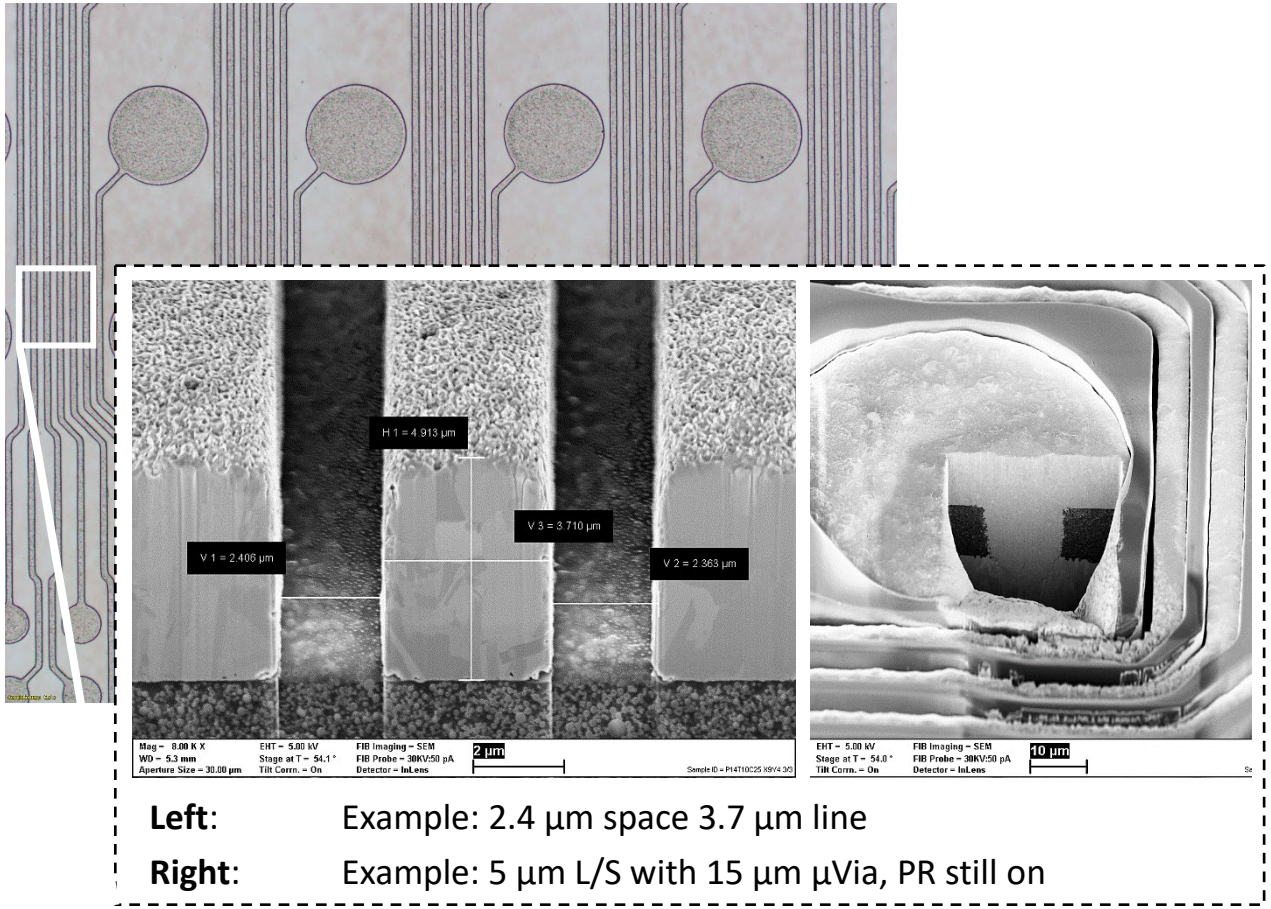
Advanced Semi Additive (aSAP) - RDL Process

Advanced Semi Additive (aSAP) - RDL Process

Process Overview



- Dielectric application
- Via formation
- PVD seeding
- Photo resist application
- Lithography
- Electrolytic Cu deposition
- Differential etch



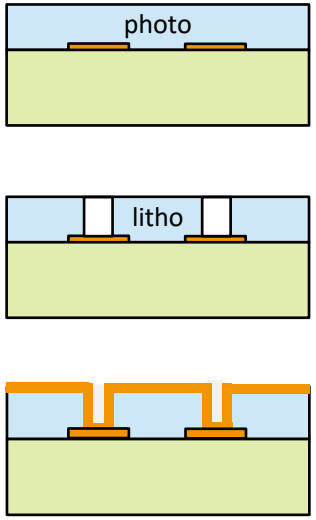
Left: Example: 2.4 µm space 3.7 µm line

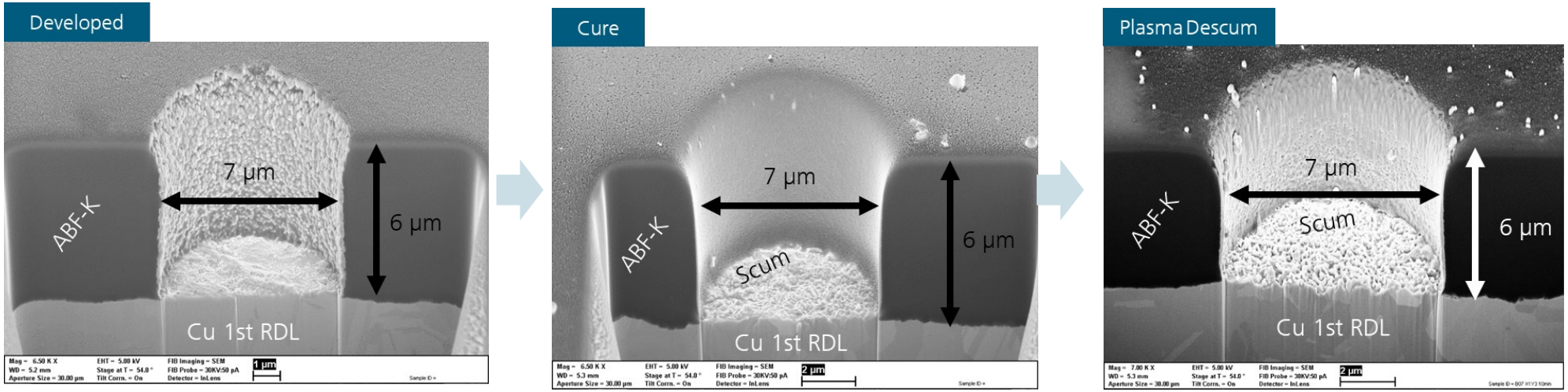
Right: Example: 5 µm L/S with 15 µm µVia, PR still on

Advanced Semi Additive (aSAP) - RDL Process

Vertical Interconnects – Photo Via

Photo Dielectric PID - Unfilled





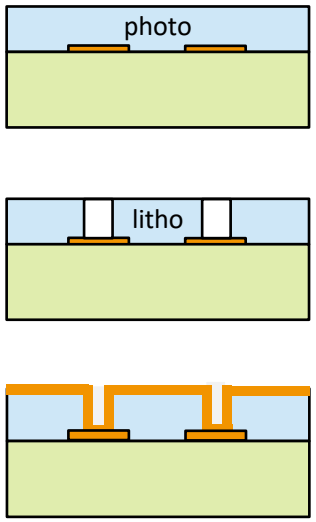
Pro: High resolution possible using suitable exposure systems
Fast and parallel processing

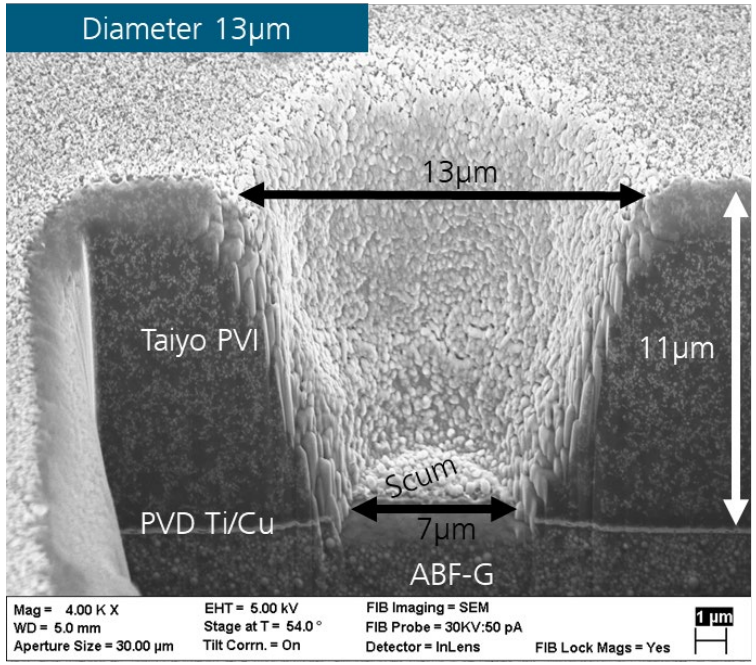
Con: Formulation of PID, Develop and Stripping chemistry
Unfilled system and resulting thermo-mechanical properties

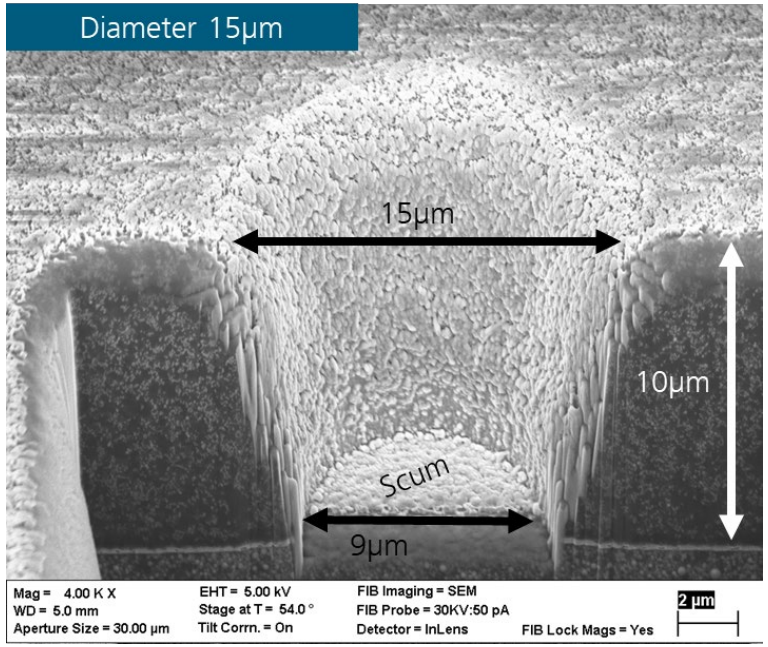
Advanced Semi Additive (aSAP) - RDL Process

Vertical Interconnects – Photo Via

Photo Dielectric PID - Filled







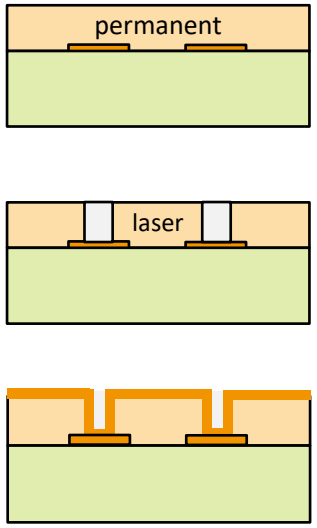
Pro: High resolution possible using suitable exposure systems
Fast and parallel processing
Better-thermo-mechanical properties than non-filled

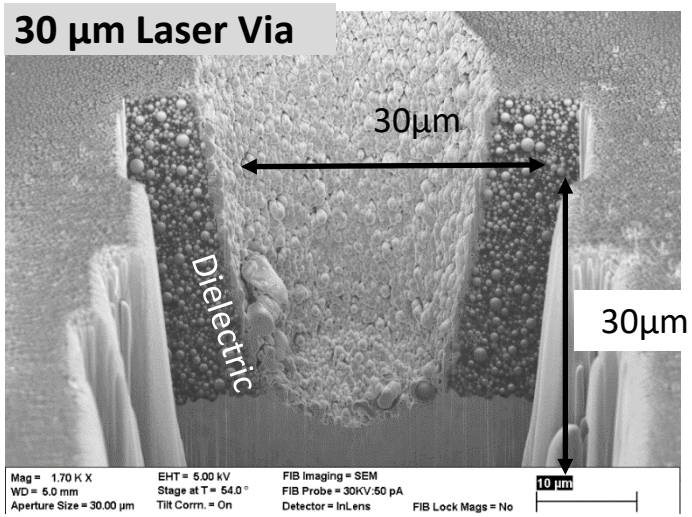
Con: Resolution and resulting Via diameter limited by filler particles

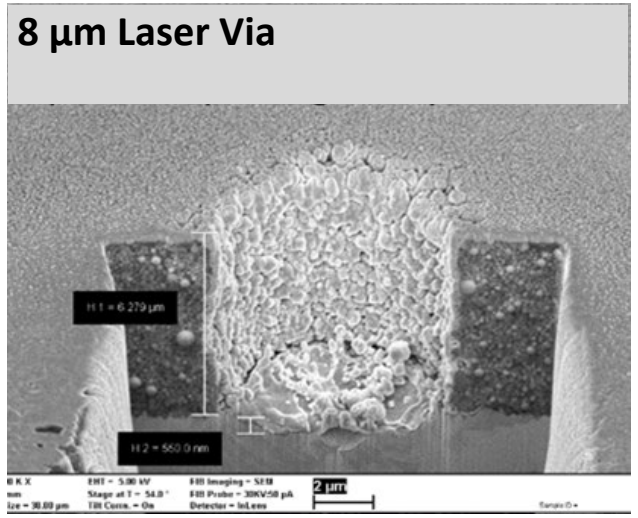
Advanced Semi Additive (aSAP) - RDL Process

Vertical Interconnects – Laser Via

Non-photo dielectric







Pro: Established process, derived from HDI substrates
Filled materials with good thermo-mechanical properties

Con: Minimum diameter limited by focal spot of laser
Serial process results in time dependence from number of vias for processing

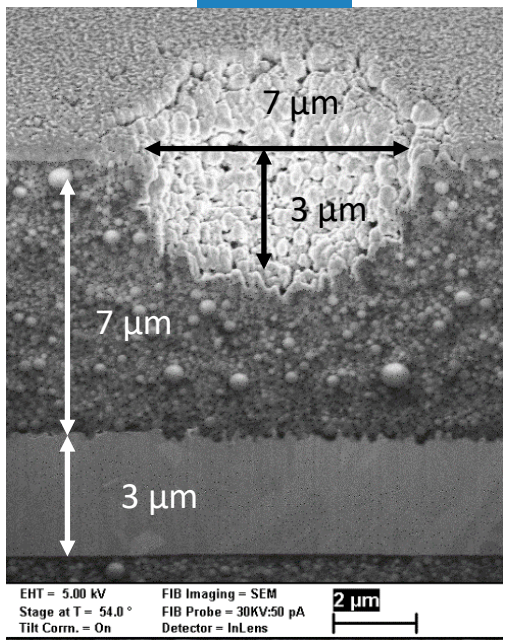
Advanced Semi Additive (aSAP) - RDL Process

Vertical Interconnects – Laser Via

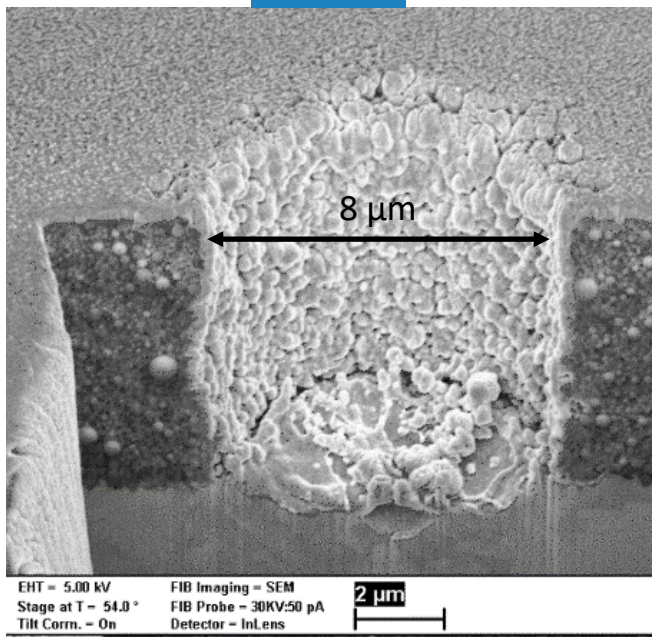
Impact of drilling parameter:

- Pulsed pico second laser: 355nm, focal spot 20µm
- Punch modes with 0.5W power with PET
- Appearance of via using Five to eight pulses

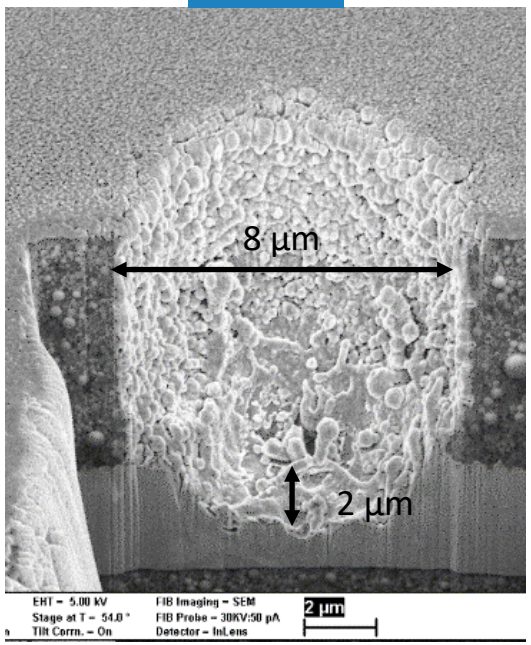
5 Pulses



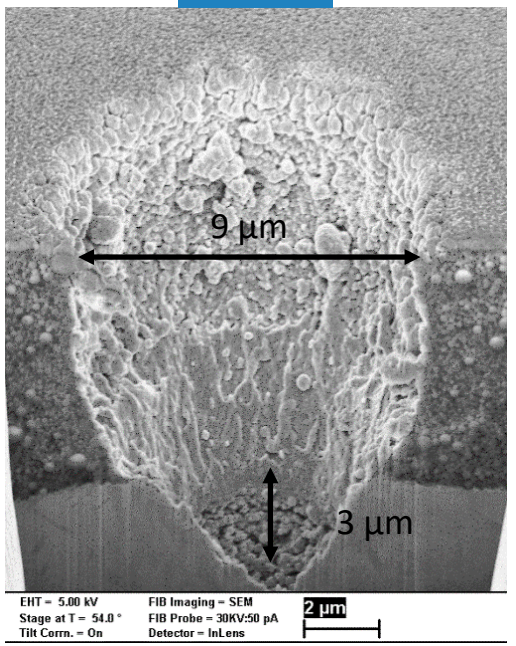
6 Pulses



7 Pulses



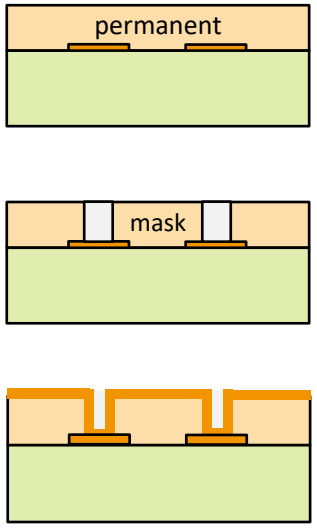
8 Pulses

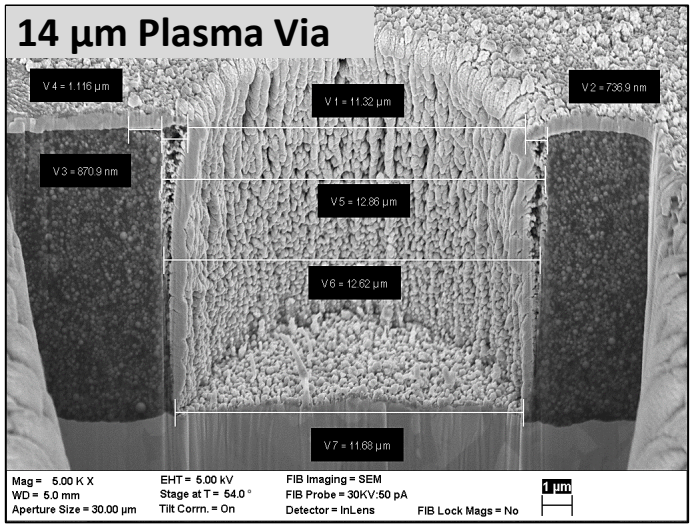


Advanced Semi Additive (aSAP) - RDL Process

Vertical Interconnects – Plasma Via

Plasma via in non-photo dielectric





Pro: Dry, plasma-based process, using metal mask
Via dimensions defined by lithography limits for metal mask
Highly parallel processing possible

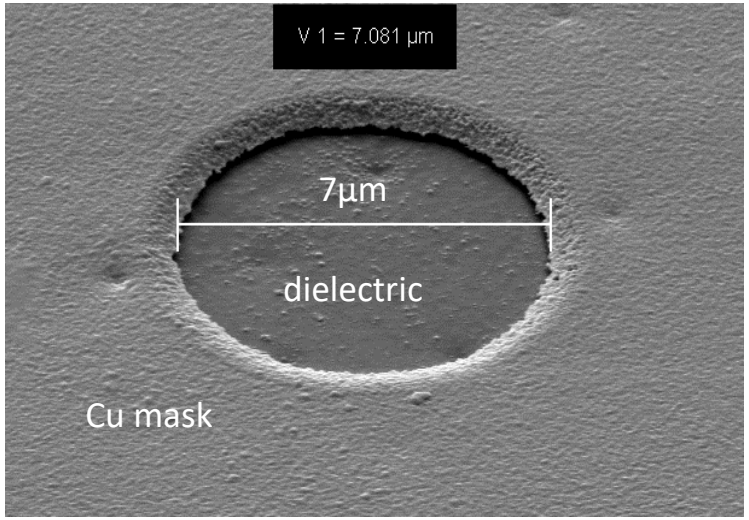
Con: Polymer redeposition, Fluor gases,
Still low etching rates result in long process times

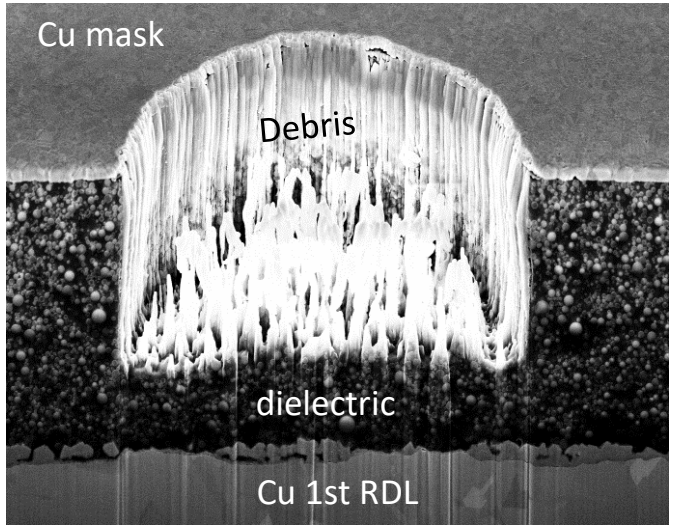
Advanced Semi Additive (aSAP) - RDL Process

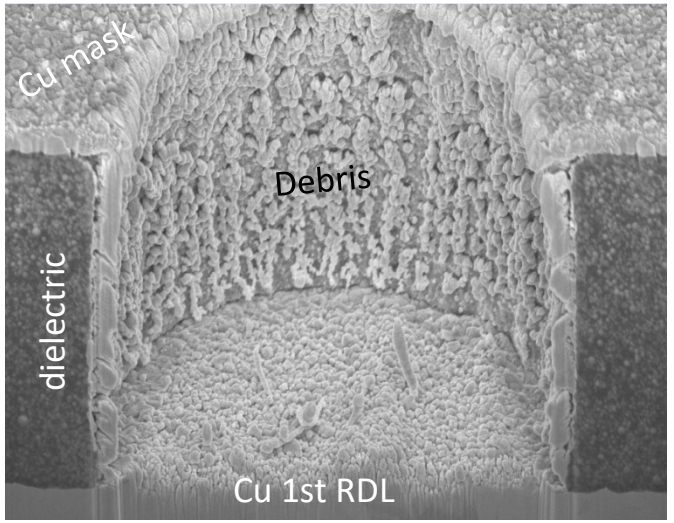
Vertical Interconnects – Plasma Via

Process sequence:

- Formation of metal mask
- RIE etching of dielectric, consisting out of etching and cooling cycles
- Cleaning of polymer debris out of via

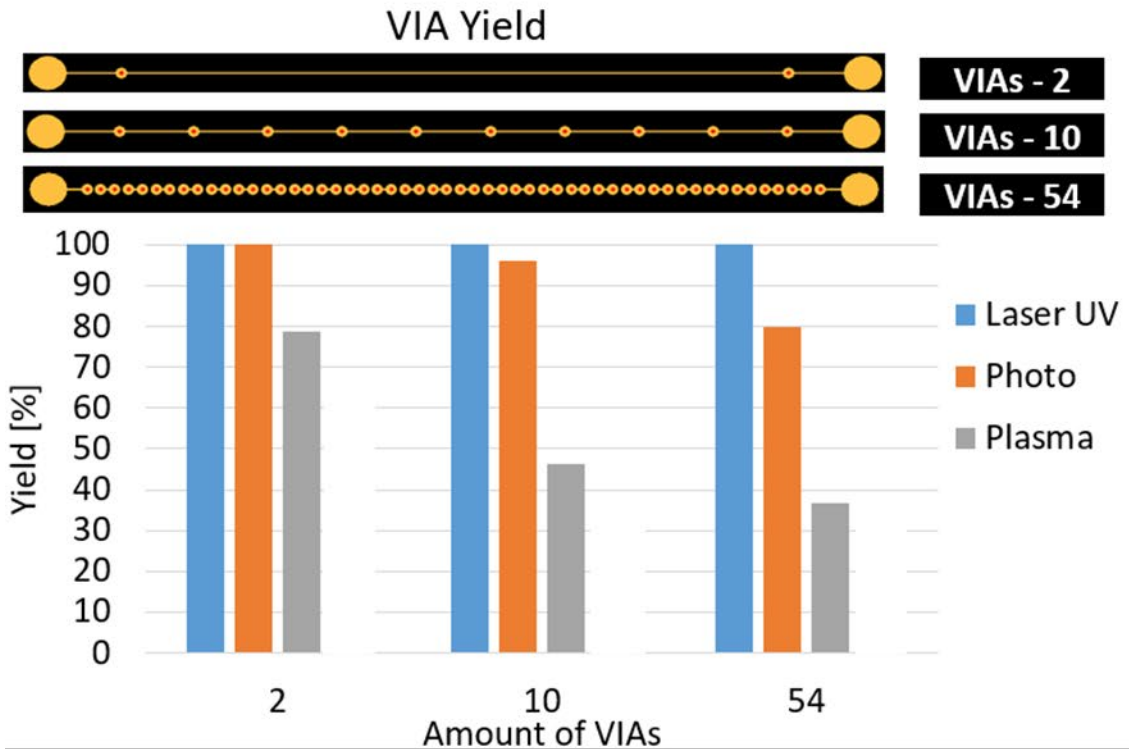


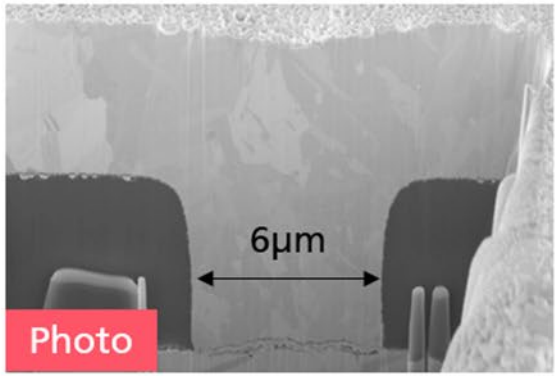


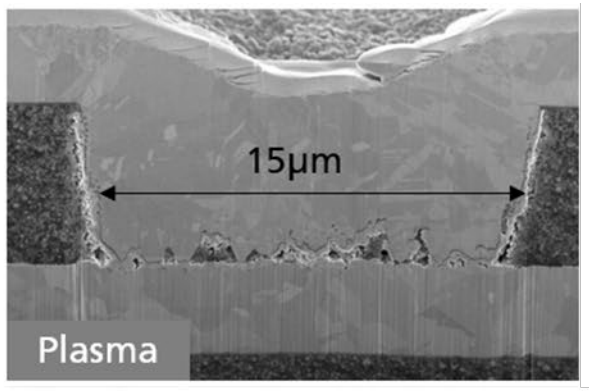


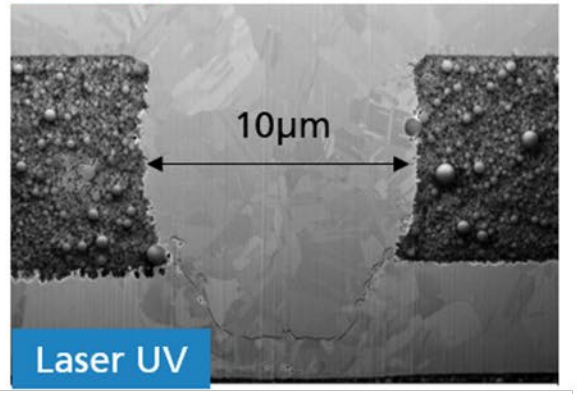
Advanced Semi Additive (aSAP) - RDL Process

Impact of via technology on yield









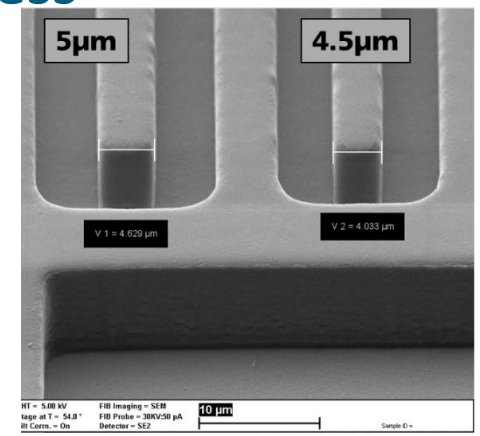
- Laser via: Achieves best yield, due to the well understand technology
- Photo via: Needs improvement towards descum after formation in order increase yield
- Plasma via: Removal of redeposited polymers essentially to increase yield

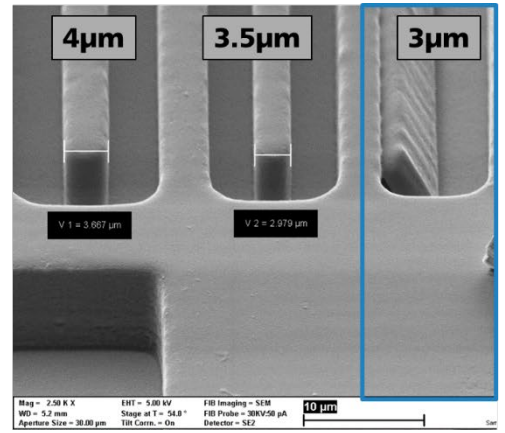
Advanced Semi Additive (aSAP) - RDL Process

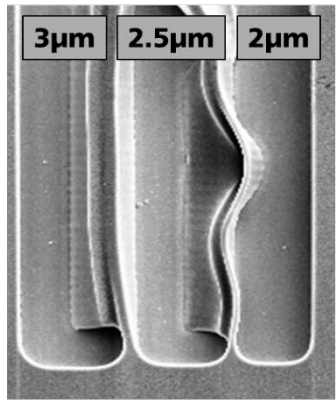
Horizontal – Lithography process

Photo resist & application

- Need for suitable photoresist for ultra fine line definition
- Method of application on panel:
  - Dry film: Ideal due to application by lamination
  - Liquid: Spraying, dipping,…
- Examples:
  - Dry film Resonac RY5107
  - Spin-on & sprayed liquid resist Sumitomo XI 4920
- Current limits in film thickness, 7µm DFR / 4µm liquid sprayed, have significant impact on Cu line thickness
- Exposure using high-resolution DI system

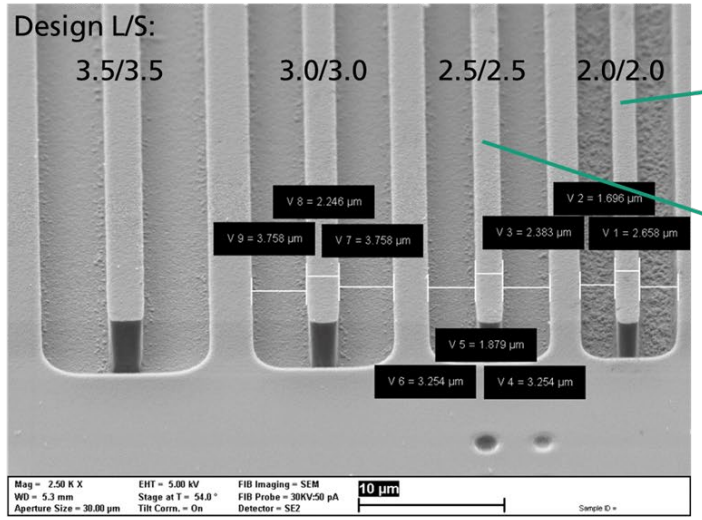


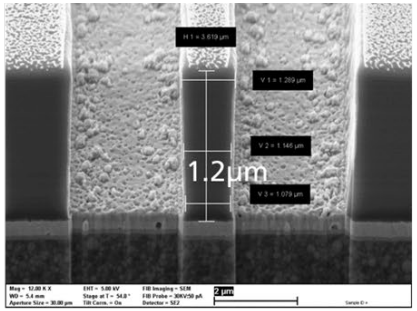


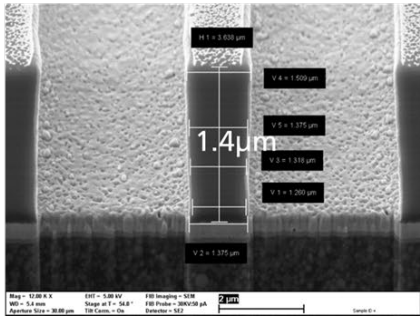


Dry film

- Resolution: approx. 3,5µm L/S







Results liquid photo resist

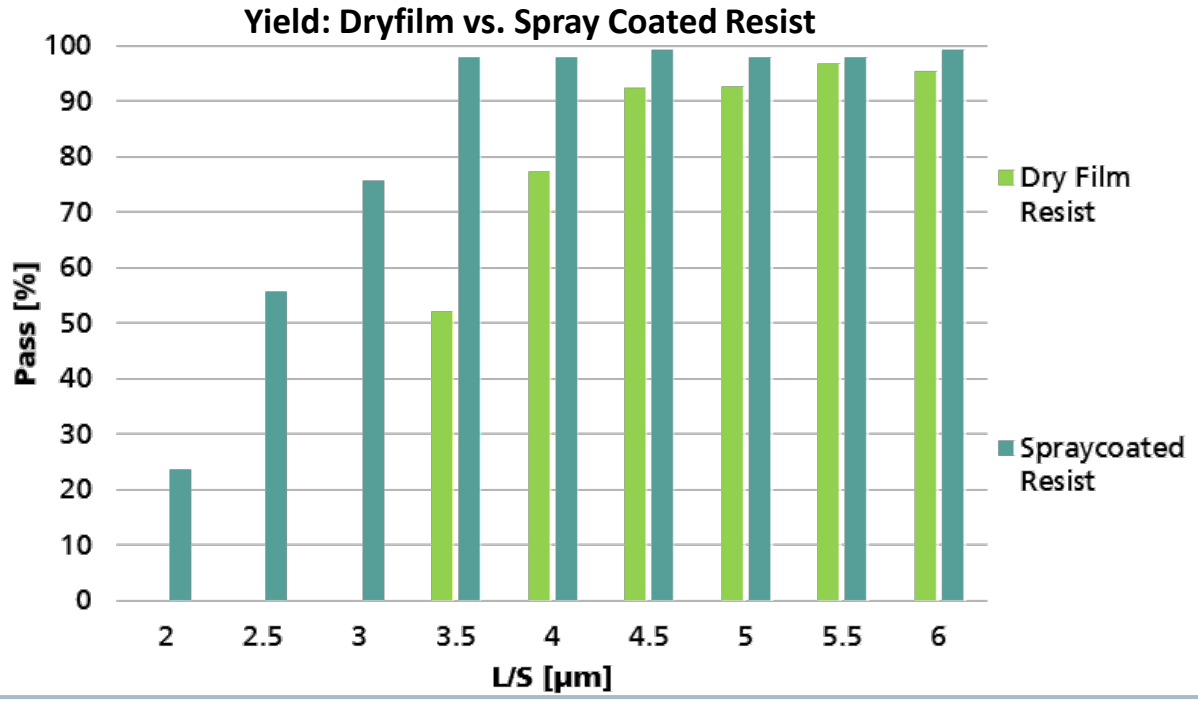
- Resolution: approx. 2,5µm L/S

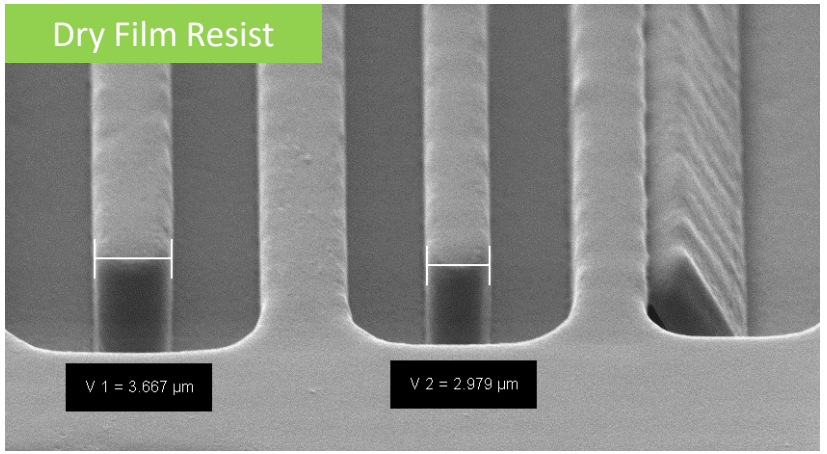
Advanced Semi Additive (aSAP) - RDL Process

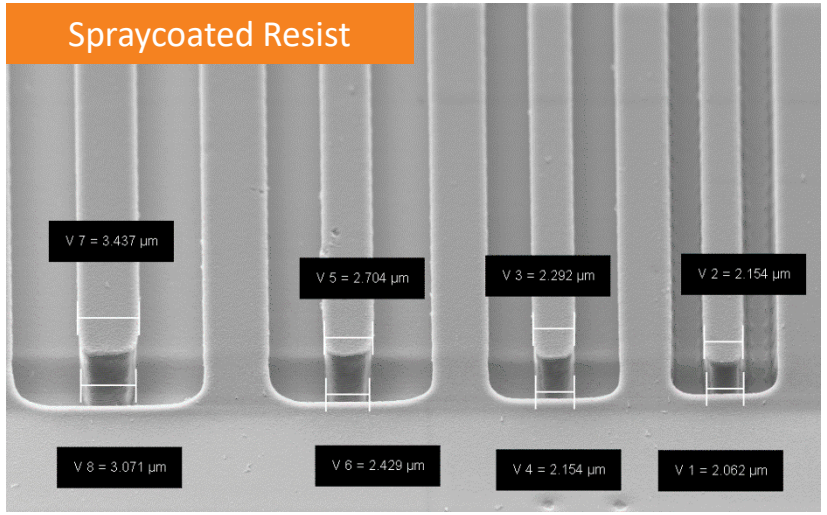
Horizontal – Lithography process

Impact of resist system: Spray coated liquid vs. dry film, to yield

- Electrical test of resulting RDL for opens and shorts
- Dry Film Resist: Confirmation of appearance after develop resulting in significant drop of yield below 5µm
- Spray coated Resist: high yield down to 3.5µm, below also significant drop





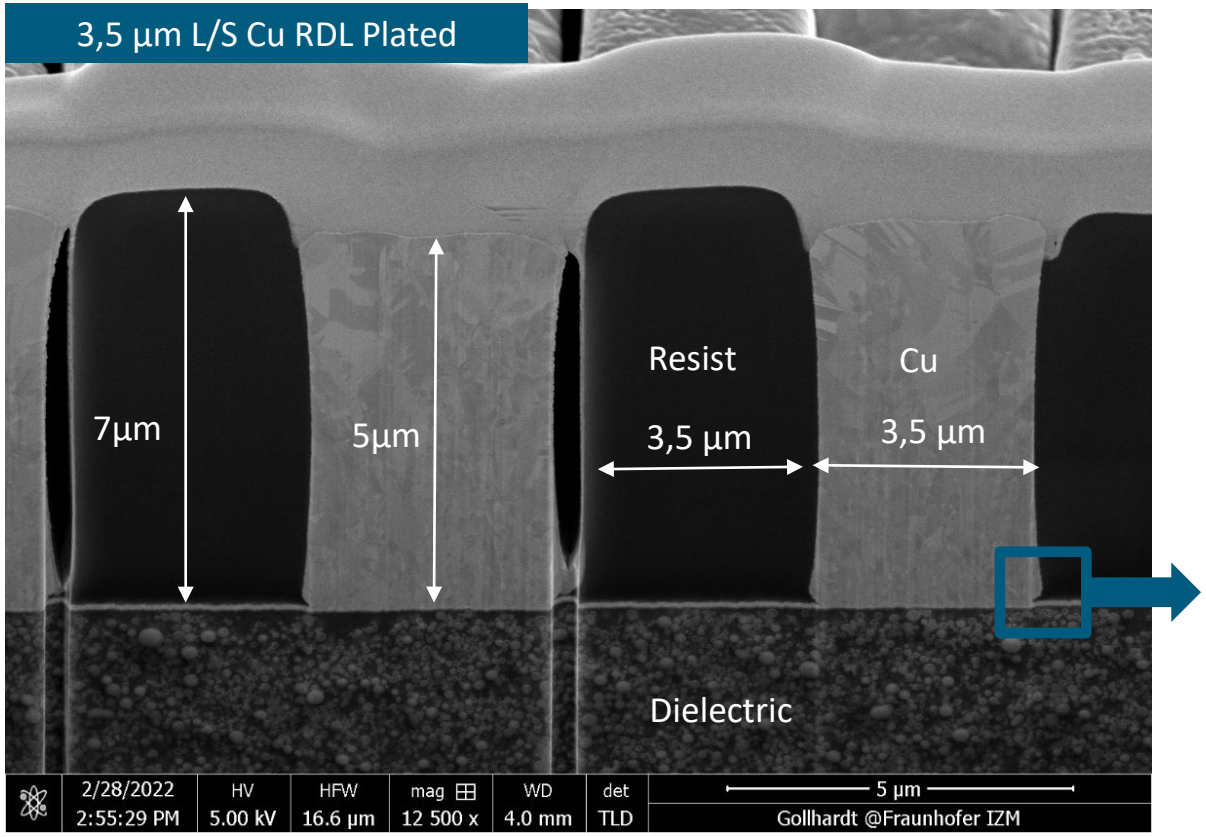


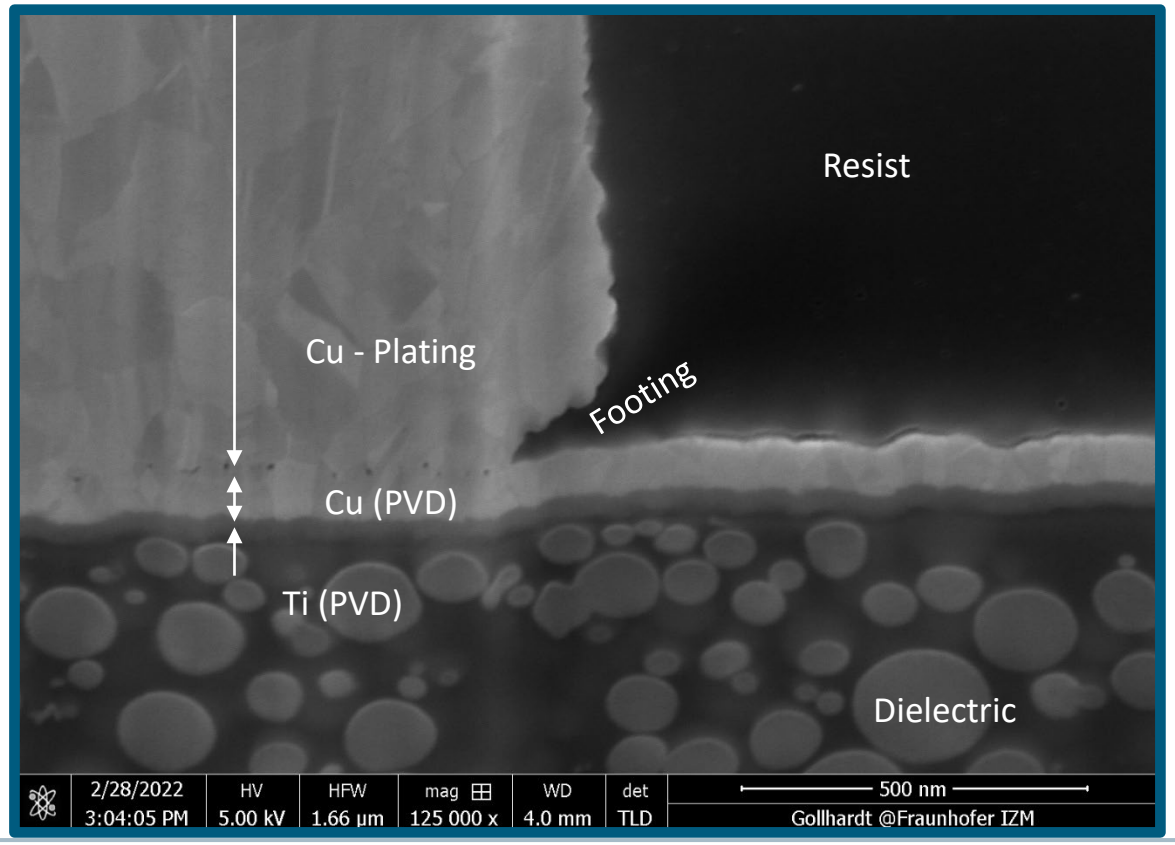
Advanced Semi Additive (aSAP) - RDL Process

Horizontal – Cu Plating

Plating in dedicated panel plating equipment

- Pretreatment: Descum and pre-wet
- Electrolytic Cu plating, example: 5µm in 7µm thick resist





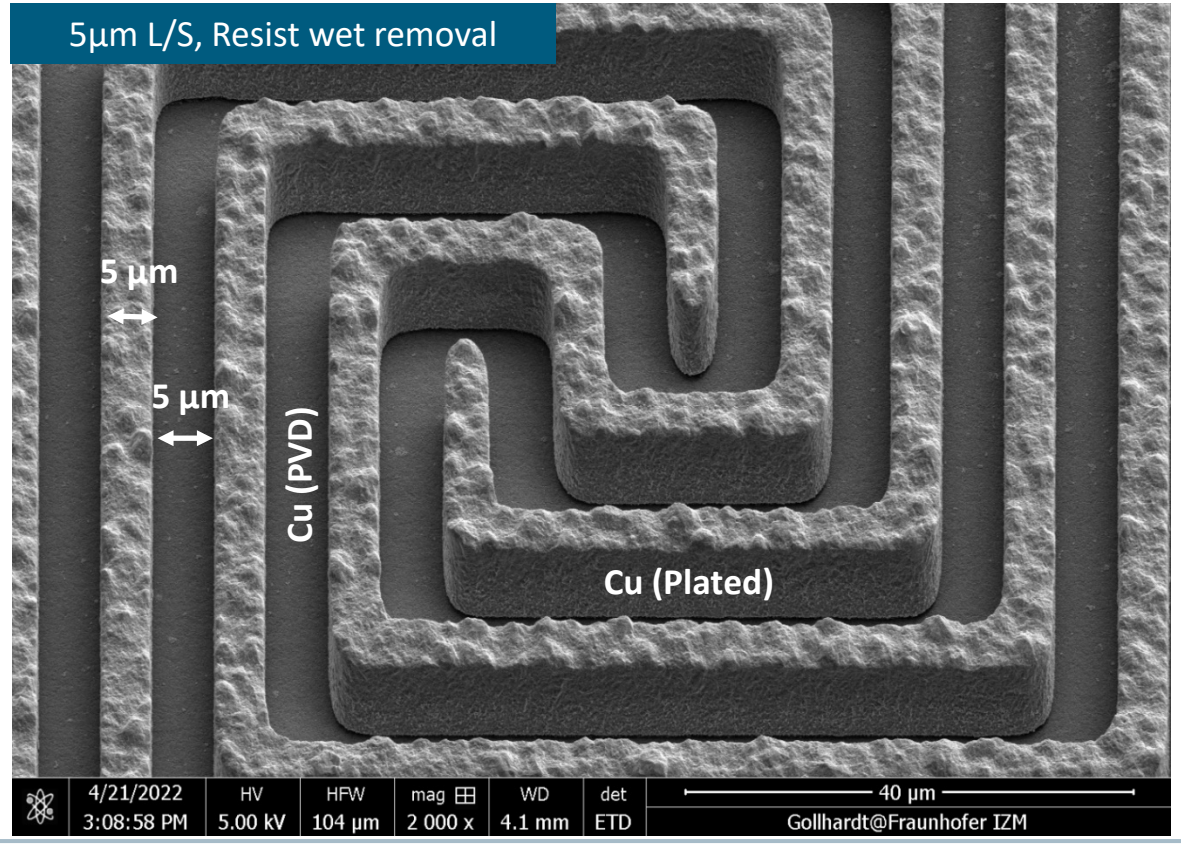
Advanced Semi Additive (aSAP) - RDL Process

Horizontal – Resist removal

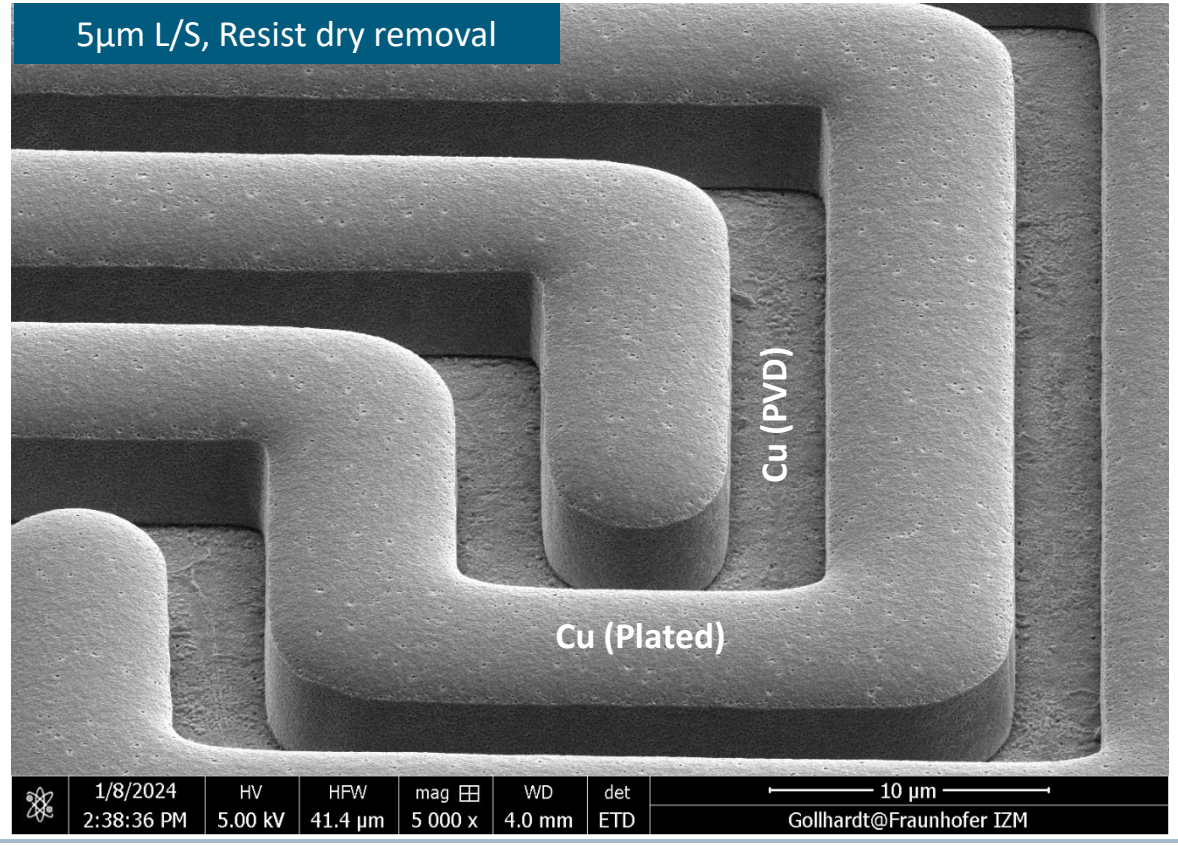
Resist removal after cu deposition

- Left: Wet chemically removed
- Right: Dry etched (Plasma) and cleaning

5µm L/S, Resist wet removal



5µm L/S, Resist dry removal

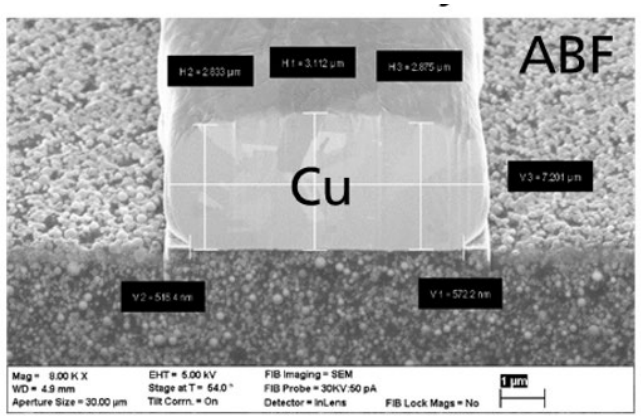


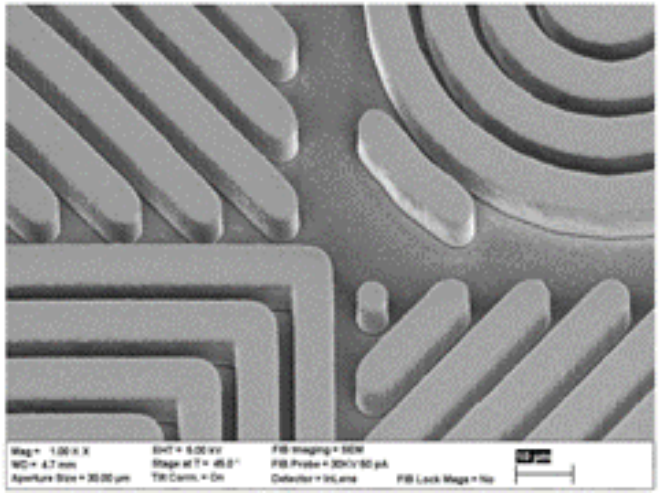
Advanced Semi Additive (aSAP) - RDL Process

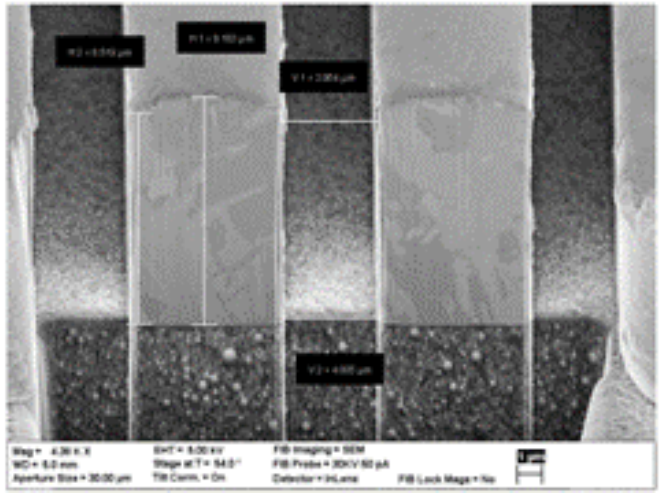
Horizontal - Seed etch

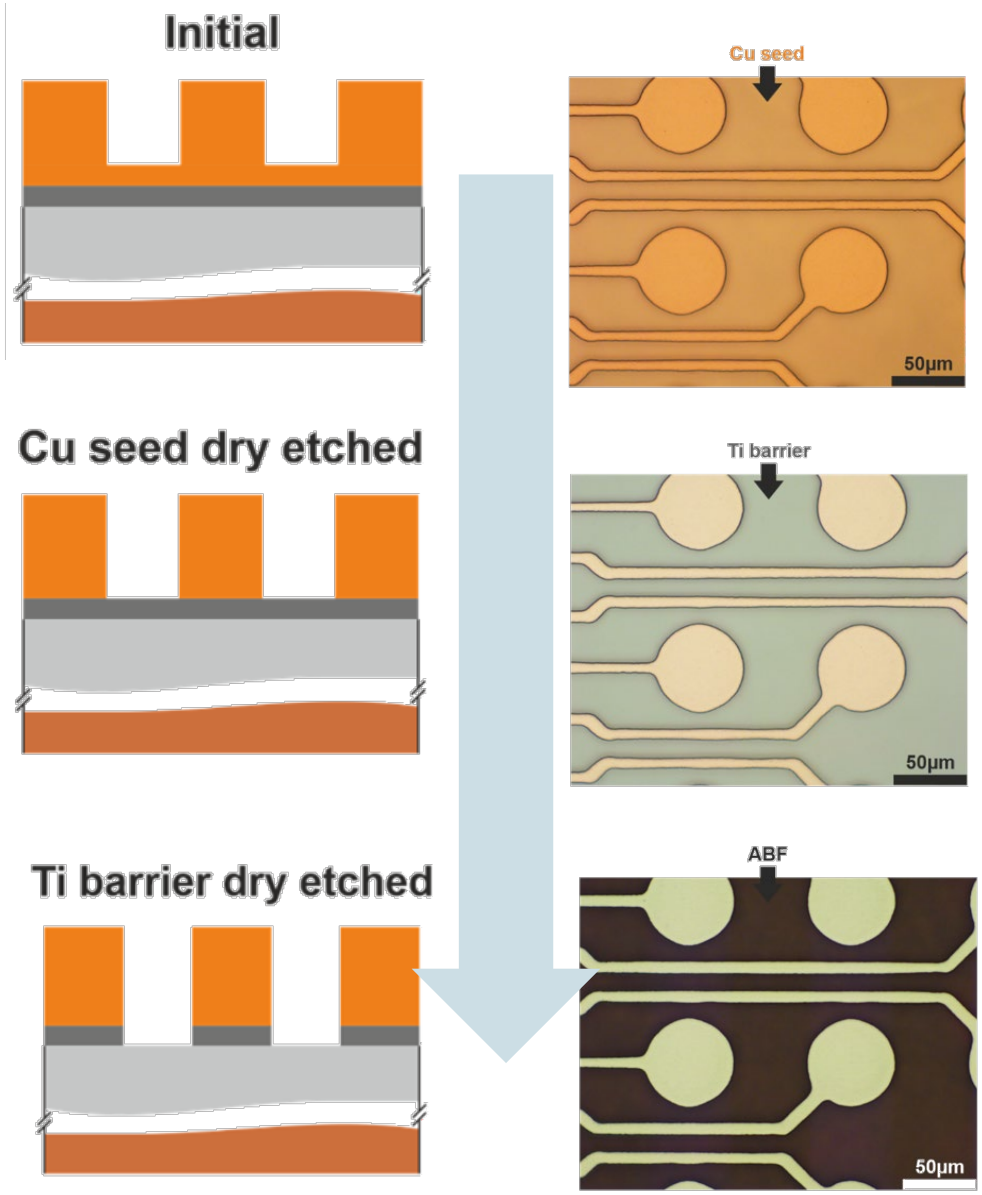
Cu and Ti differential etching

- Wet chemical methods limits minimum line width and space due to under etching of plated copper
- Structures below 5µm require minimum under etching
- Dry etching with almost anisotropic process could be an alternative









03

Process Control / Electrical Testing

Process Control - Electrical Testing

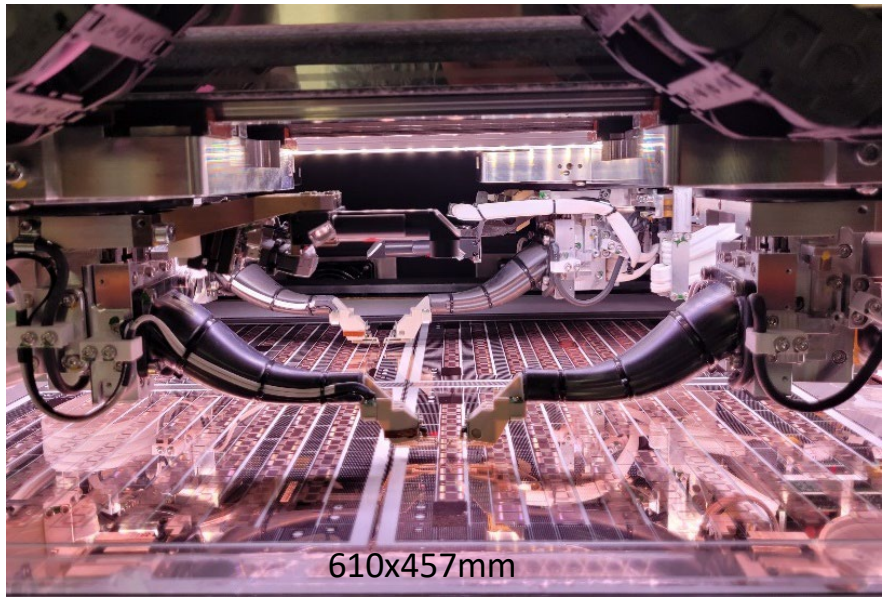
Equipment

A9 and A9+ (cleanroom):

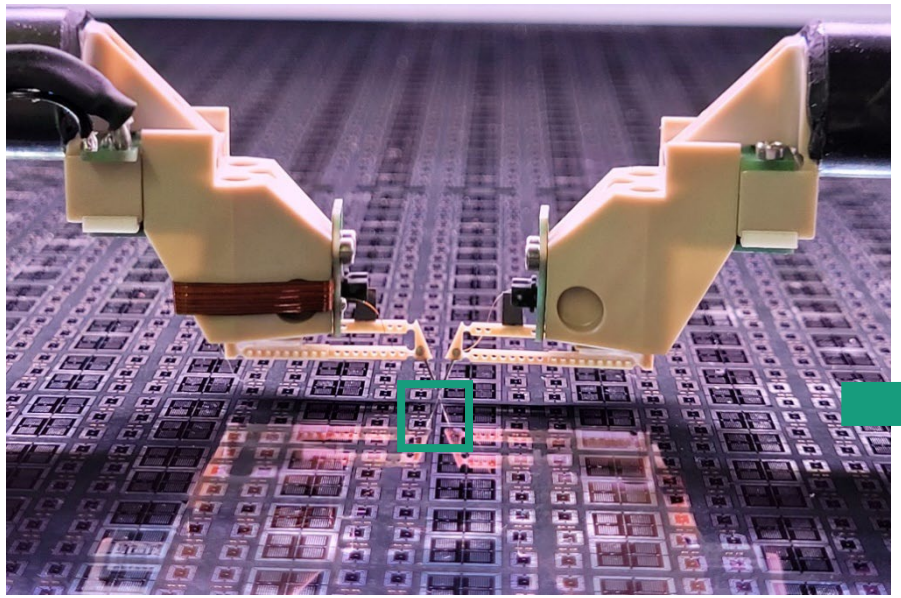
- Automated Inner layer Test
- 8 Probes: 4 Top, 4 Bottom
- Min Board Size: 10x10mm
- Max Board Size: 640x535mm

- Specs:
  - Camera 3µm/pixel
  - Smallest Pitch: 50µm
  - Smallest Pad: **25µm**
  - R: 25µΩ… 200MΩ
  - C: 30fF …100µF
  - L: 25µH…10mH

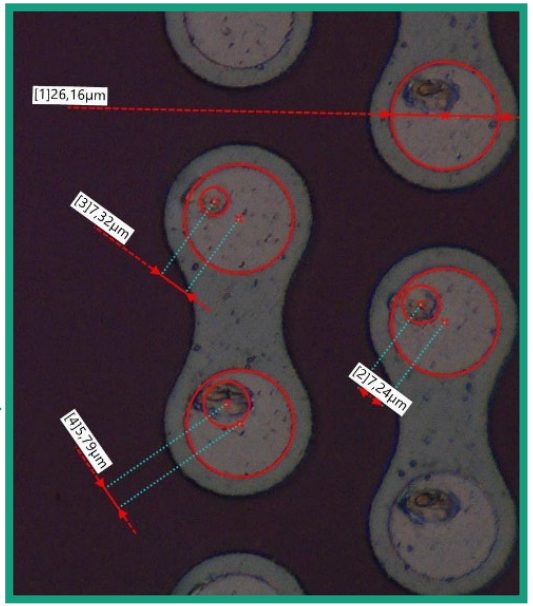
- Top Probes on Glass IC



- Testing on EMC-Panel, Chip First [PLC2]



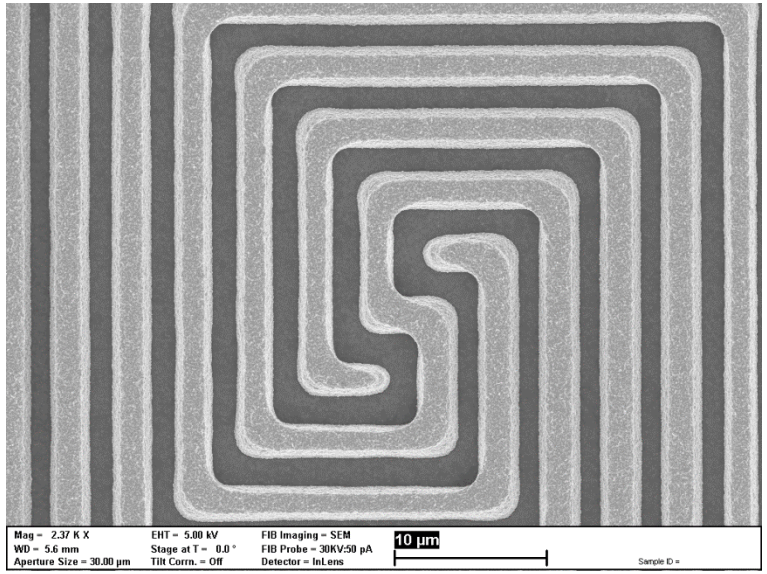
- Probemarks on **25µm** Pad



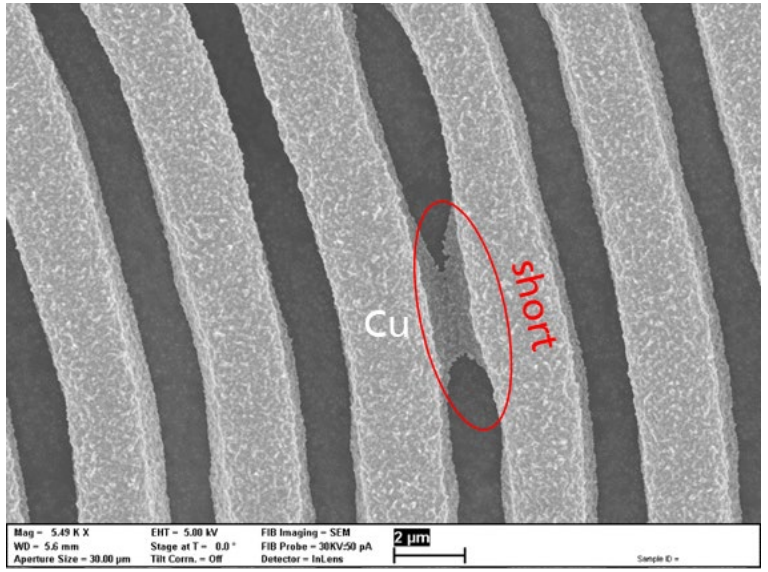
Process Control - Electrical Testing

Yield evaluation of RDL structures

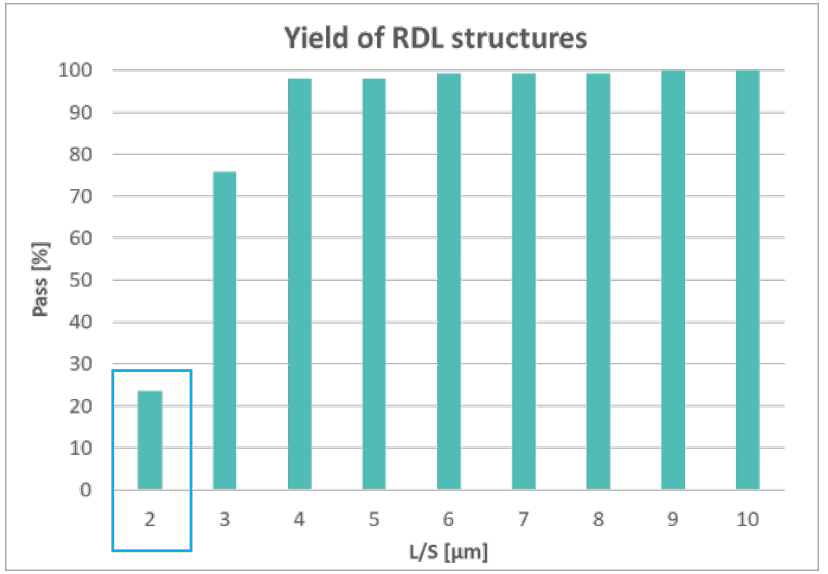
- Test structures: Coils 1,44 mm²
- Testing of open and short
- Main failure: Shorts
- Analysis of potential failures in complete process chain



Test structure 2µm L/S



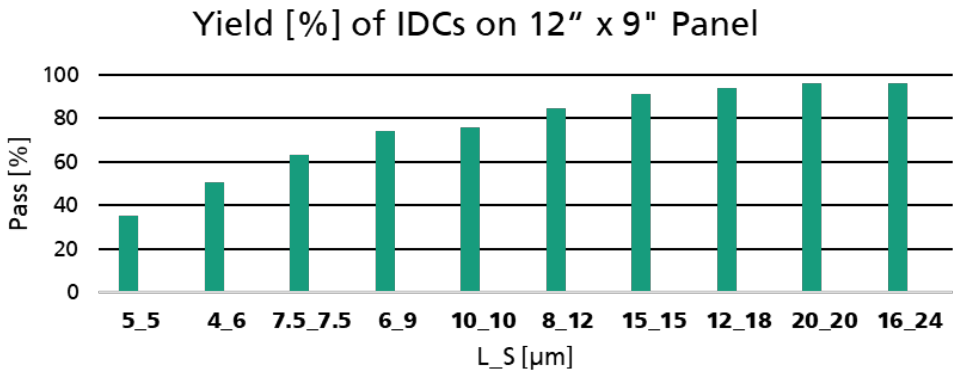
Typical failure



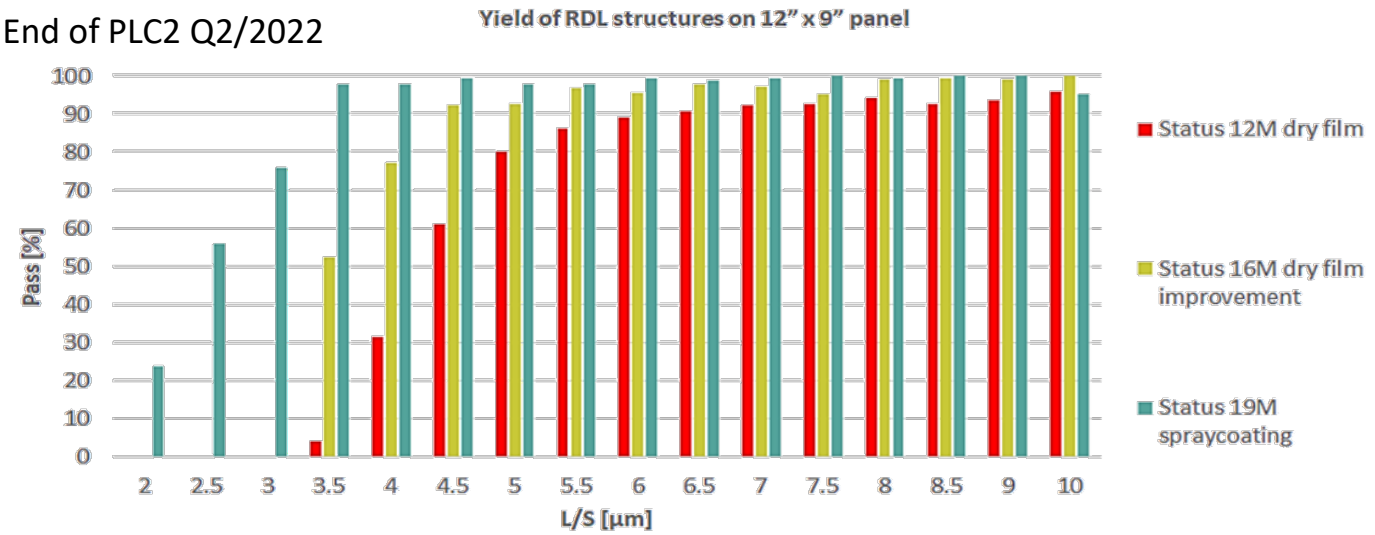
Process Control - Electrical Testing

Electrical testing & yield of RDL structures

Start of PLC2 Q1/2020 (dry film only)



End of PLC2 Q2/2022



Method

Example from Panel-Level Consortium 2:

- Flying-Probe testing of IDCs (4200 x 380 µm²) on 303mm panel
- Improved Fine Line test vehicle within PLC2
- Flying-Probe testing of spiral and rectangular coils (580x580µm²) with 468 coils per L/S resolution 10 to 2µm L/S

Results

- ≈ 35% yield for IDCs of 5µm L/S structures at the start of PLC2
- SAP optimization based on failure classification & root analysis was performed
- First 2µm L/S structures achieved @ 24%
- Yield improvement: 3.5µm L/S - 52% to 98%

04

Outlook & Summary

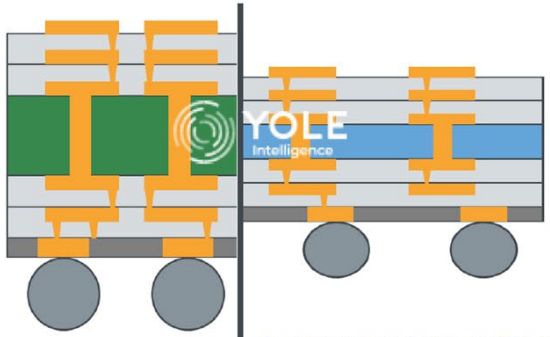
Outlook

Glass core - Motivation

GLASS CORE VS. ORGANIC SUBSTRATES

Organic Core substrate

- >10/10µm L/S.
- Organic Core substrates are currently in HVM at a lower cost than GCS.
- The warpage issues of larger organic substrates are the main obstacle.
- The processing temperature is lower than GCS due to the polymeric nature of the core.



Glass Core substrate

- Current <5/5 L/S and an enabler of <2/2 L/S in the next few years.
- GCS tolerates higher temperatures and offers 50% less pattern distortion
- From a lithographical point of view, GCS has a better DoF* due to the ultra-low flatness.
- GCS has a higher interconnect density (up to 10x compared to OCS)

- Dielectric constant of organic substrates varies between 4 and 6.
- Loss tangent of organic substrates is around 0.02, which is higher than GCS's 0.005.
- Organic substrates have lower thermal conductivity than GCS : 0.2 – 0.5 < ~ 1.5 W/mK.
- The CTE of organic substrate is higher: ~17 vs. 3 – 8 ppm/°C of GCS.
- Organic substrates target a broader range of markets (most in low to mid-end applications).

- Less warpage issues as the mechanical properties of GCS allow ultra-large form-factor packages (up to 240×240)
- Large-size substrates allow high assembly yields.
- In terms of design rules, GCS provides increased flexibility for signal routing and power delivery.
- In terms of power delivery, GCS allows high-speed signaling at ultra-low power
- GCS's dimensional stability is critical to achieving precise alignment between layers in interconnect overlays with very tight tolerances.
- Filled TGV with a high aspect ratio from (1:10 to 1:50)
- Glass core thickness can reach 1mm for applications such as AI and data center
- GCS-related R&D initiatives have been very active in the last few years.

*Depth of Focus

YOLE Intelligence

Status of the Advanced IC Substrate Industry 2023 | Report | www.yolegroup.com | 41

Benefits of glass compared to organic core

- Dimensional accuracy during RDL build-up (temperature and moisture cycles)
- Overlay accuracy (layer-to-layer registration)
- Warpage of glass core with multi-layer RDL
- Warpage of glass-based modules during assembly

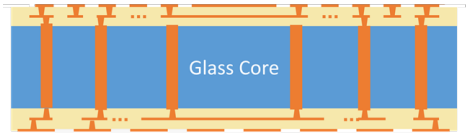
Challenges for glass core

- Glass type, thickness, CTE and modulus
- TGV density, geometry
- TGV seeding, Cu filling degree
- Cost of glass core compared to organic

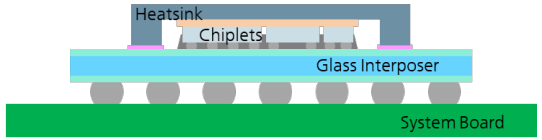
Source: Yole Status of the Advanced Substrate Industry 2023

Outlook

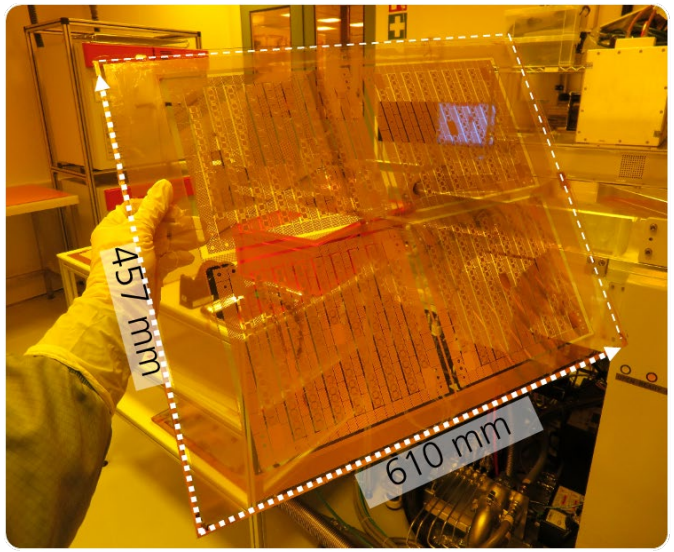
Advantages of Glass Core Substrate Technology

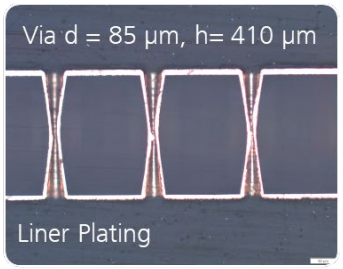


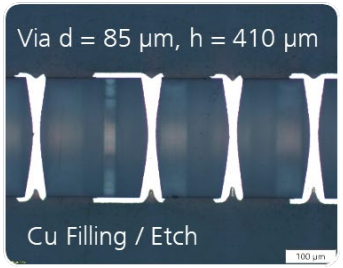
Glass core interposer



Chiplet module







	Pros	Cons
Organic Core Substrates	▪ Established technology ▪ Large production formats ➔ High productivity, low cost ➔ Large modules	• Unstable geometries & warpage ➔ Roadblock below 5 µm L/S for multi-layer RDL ➔ Yield problem
Glass Core Substrates	▪ Large production format ▪ Geometric stability & planarity ➔ High stability during processing ➔ Scalability for high wiring densities	• Brittleness of glass ➔ Handling is challenging ▪ Stiffness of glass ➔ Hardly any compensation of CTE Differences between si and PCB

Summary

1. Successful demonstration of process technology for high-density organic substrates
2. Use of aSAP process flow, with different process options for vertical and horizontal interconnects
3. Advantages and disadvantages of the different via technologies were determined
   RDL processing was optimized and alternative process option implemented
4. Routines for process control and testing have been introduced to assess the quality and yield of the entire technology chain
5. Glass core substrates offer an excellent opportunity in terms of outstanding dimensional stability. Initial approaches for this technology are already in place

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Thank you for your attention!

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