Reliable Direct Bonded Heterogeneous Integration (DBHi) for AI Hardware

Divya Taneja, Katherine Pilger, Alexis Jacques-Fortin, Maxime Godard, Isabel de Sousa
IBM Infrastructure , Bromont

Sayuri Kohara, Chinami Marushima, Takahito Watanabe, Akihiro Horibe
IBM Research, Tokyo

Joseph Ross
IBM Research, Albany

Thomas Wassick
IBM Infrastructure, East Fishkill

Outline

- Introduction to Heterogenous Integration
  - Si bridge technology
- DBHI architecture
  - Bond and Assembly Development
  - 75µm pitch
    - Reliability results for Standard and Surface DBHI
    - FA results
  - 30µm pitch
    - t(0) results
    - Reliability results for Standard DBHI
- Conclusion

Chiplet Technology (Heterogenous Integration)

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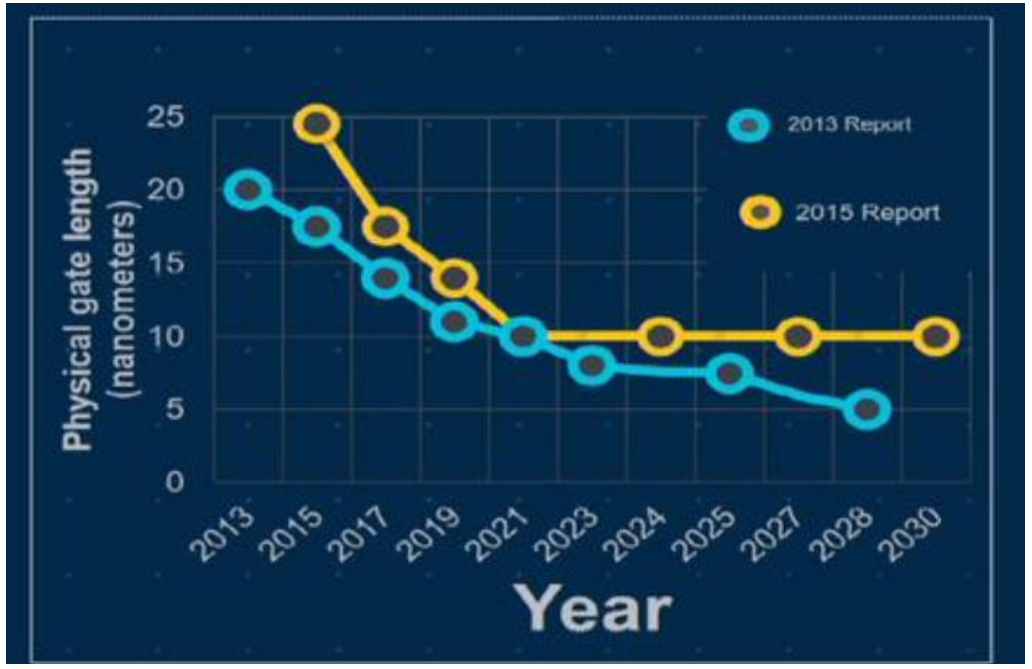
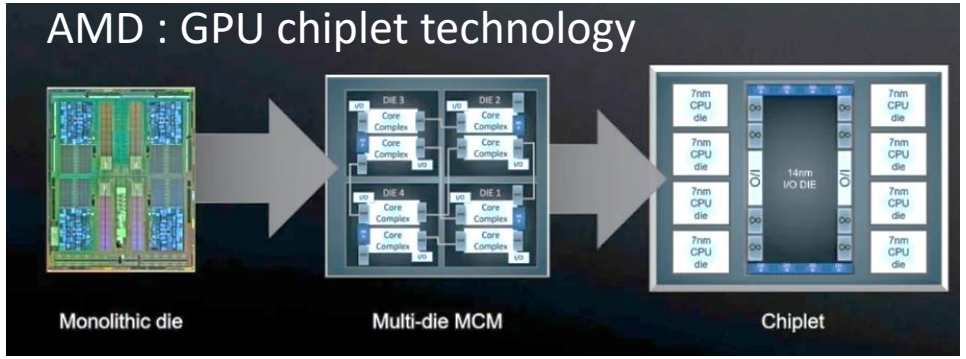
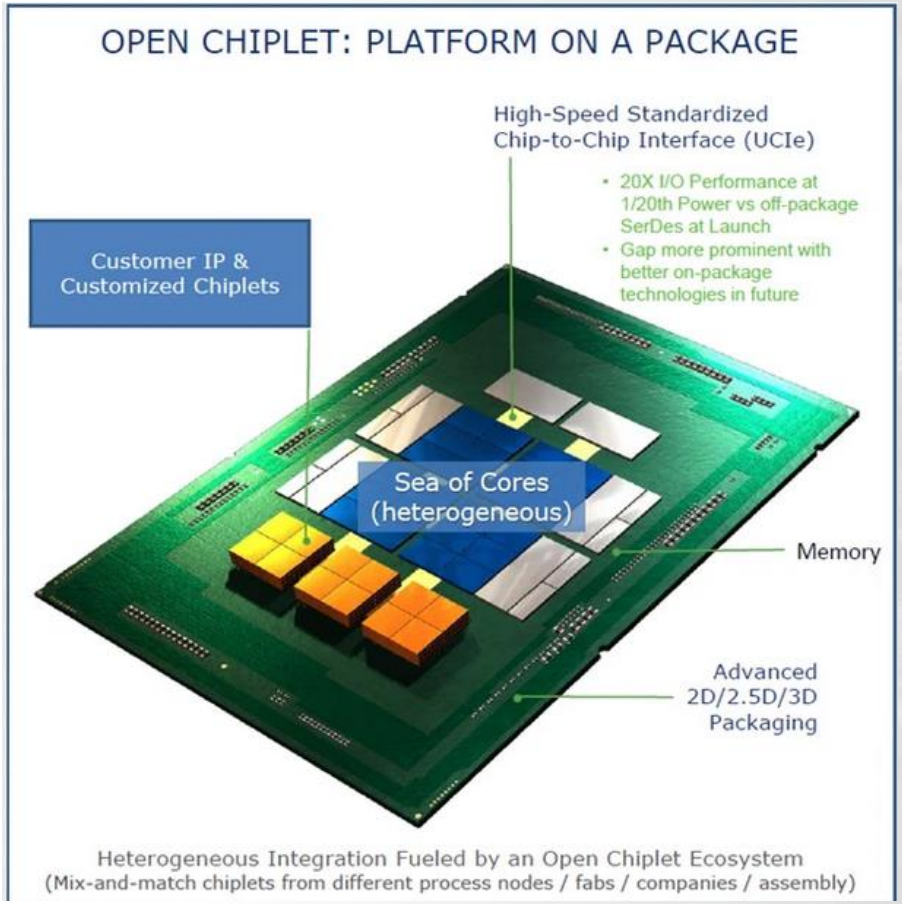




Ref : https://www.asset-intertech.com/wp-content/uploads/2020/12/Chiplet-Interconnect-Testing-Using-JTAG-Boundary-Scan-eBook.pdf



Ref : https://www.cnx-software.com/2022/03/03/ucie-universal-chiplet-interconnect-express-open-standard-for-chiplets-with-heterogeneous-chips/

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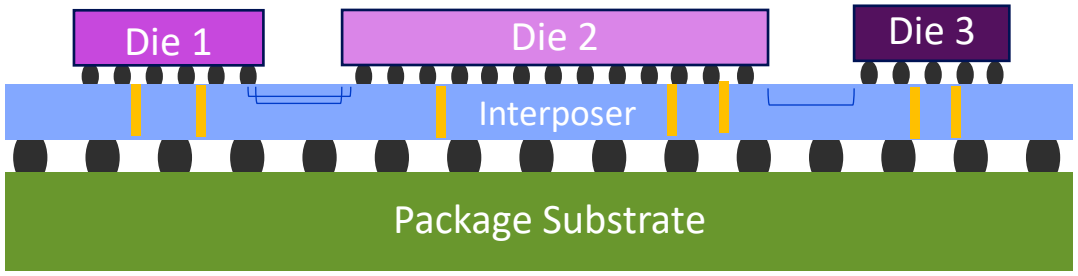
Solution for Chiplet Interconnects



Si Interposer

ADVANTAGES

- Easily adaptable in the Industry
- Finer line width line spacing (<2µm)

DISADVANTAGES

- Expensive technology
- lesser signal integrity due to Si

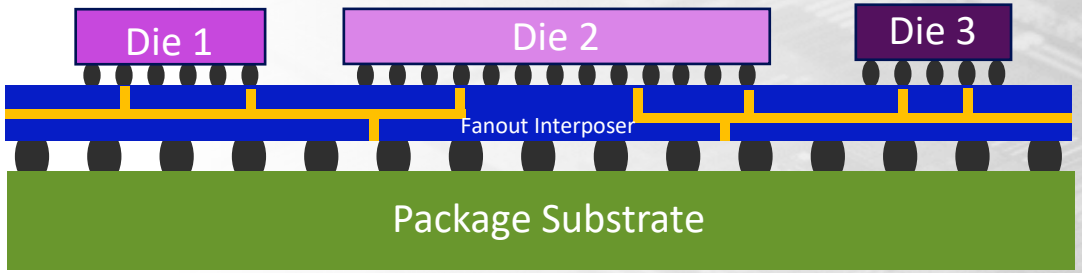
Fanout Interposer

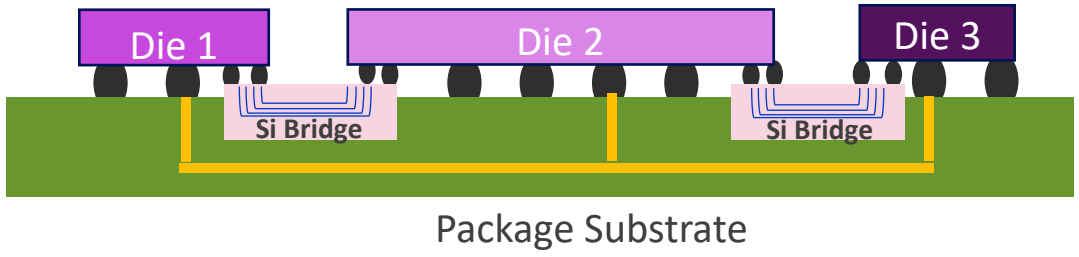
ADVANTAGES

- Lower cost than interposer
- Better Signal Integrity due to signal fanout

DISADVANTAGES

- Requires special processing capabilities
- Limitation with line width/spacing (>2µm)





Si Bridge

ADVANTAGES OVER SI INTERPOSER :

- Lower cost than Si interposer
- Better Signal Integrity due signal fan out within the package and Si die locally

ADVANTAGES OVER FANOUT INTERPOSER :

- Easily adaptable in industry
- Supports finer line width /spacing

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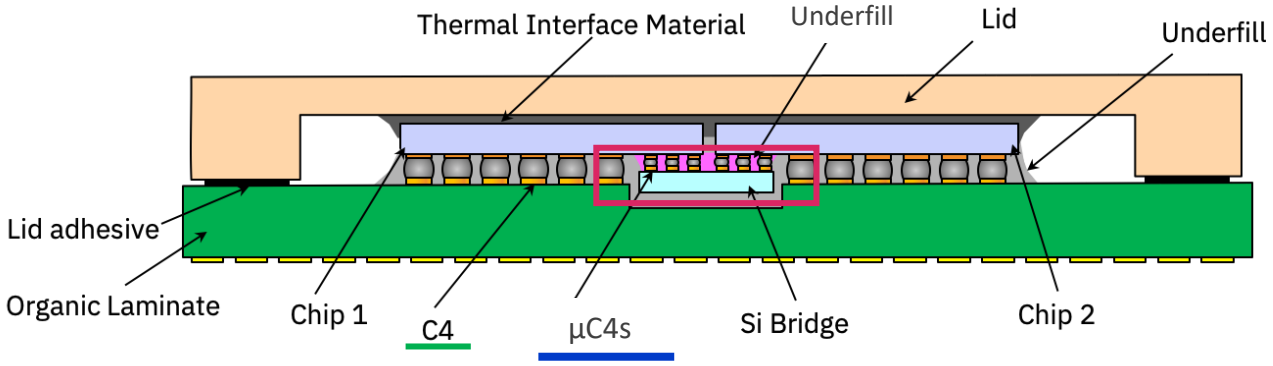
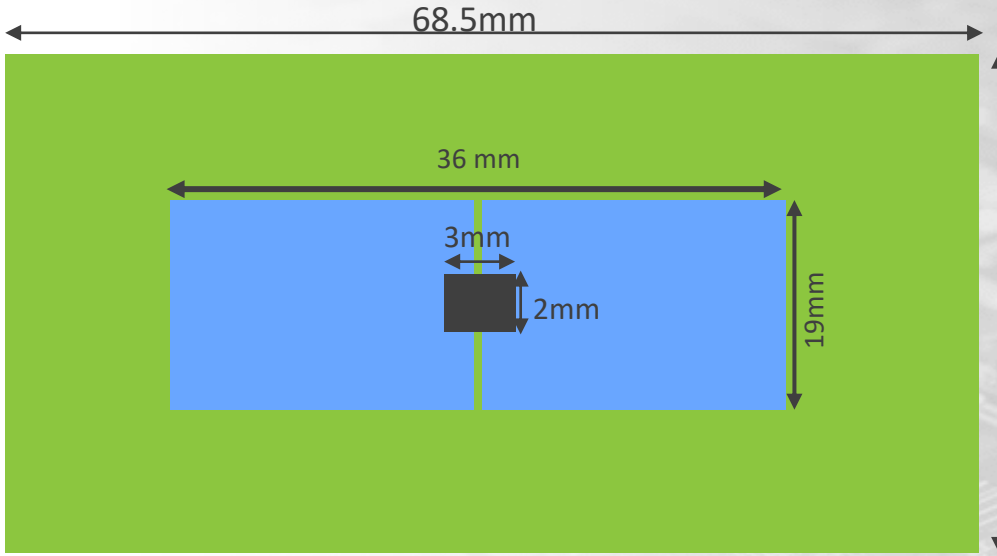
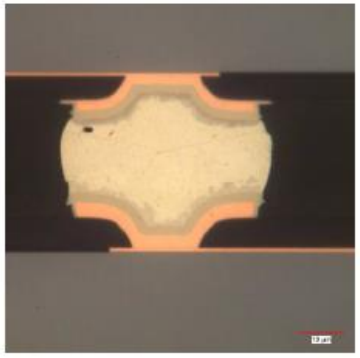
Introduction : DBHI

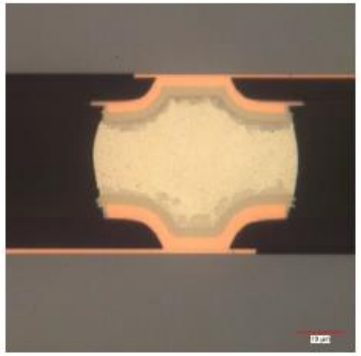


X-sectional View



Top View * Closer to 1 Reticule size





Advantages

- Power Efficiency (0.2pJ/bit)
- Bandwidth Density : <0.5TB/mm/s

DBHI Architectures

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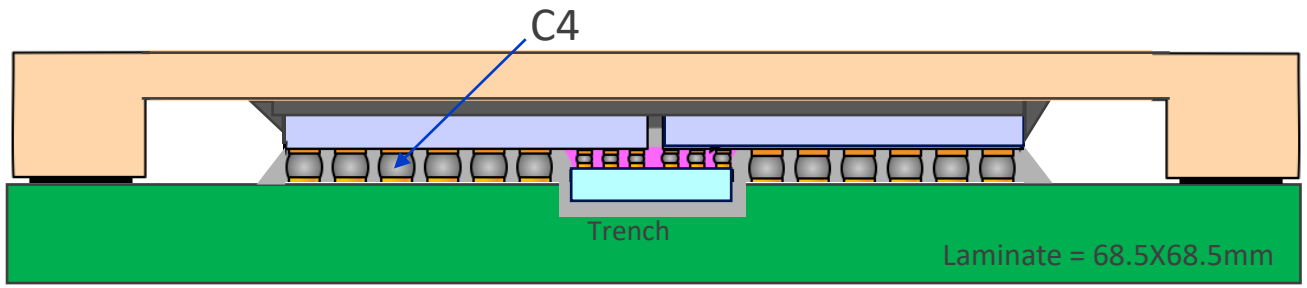
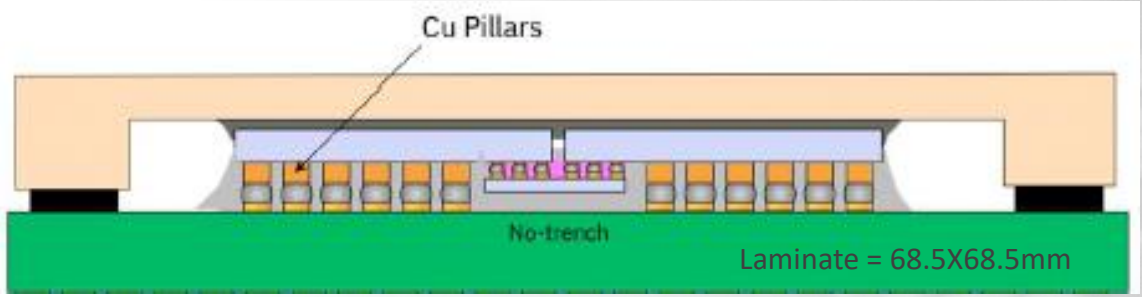
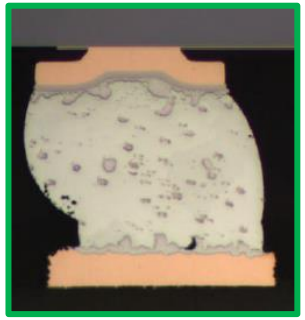
Standard DBHI

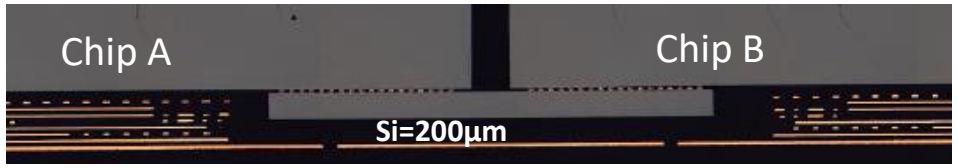


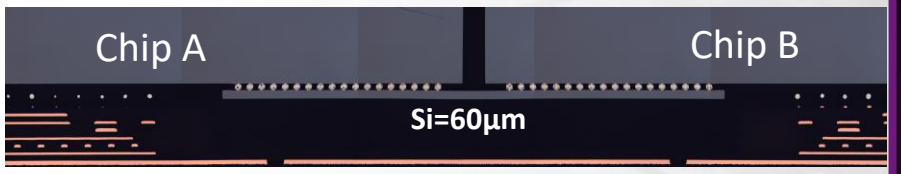
Surface DBHI





C4





Cu pillar

Advantages for Surface DBHI

- Performance : no keep out area below the Si bridge (Flexibility for Signal Routing)
- Process Development : No additional processing for laminate as in case of Standard DBHI

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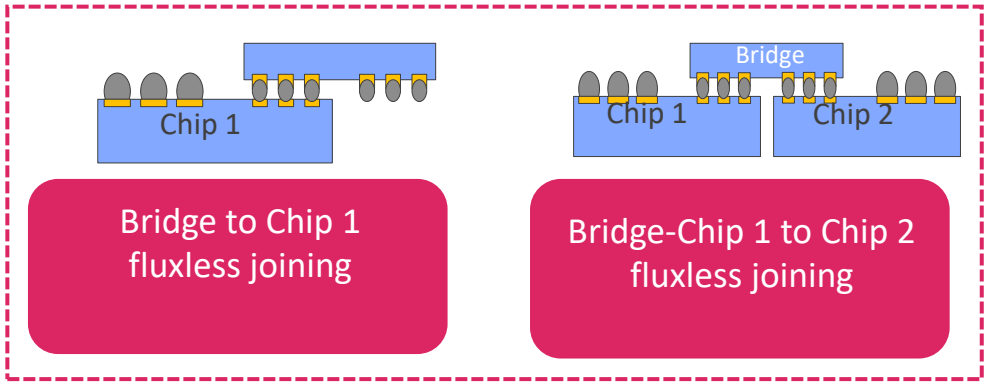
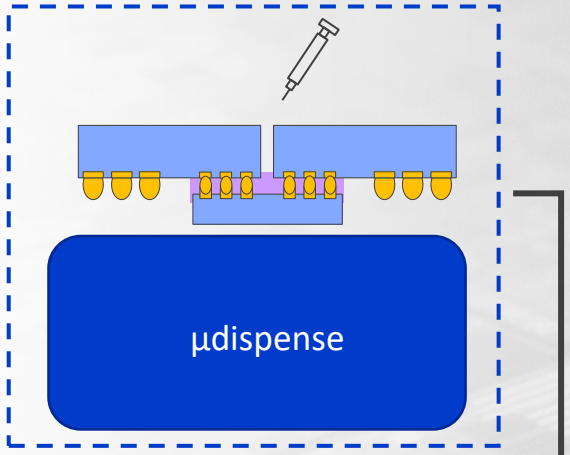
Bond and Assembly Process

1. Subassembly

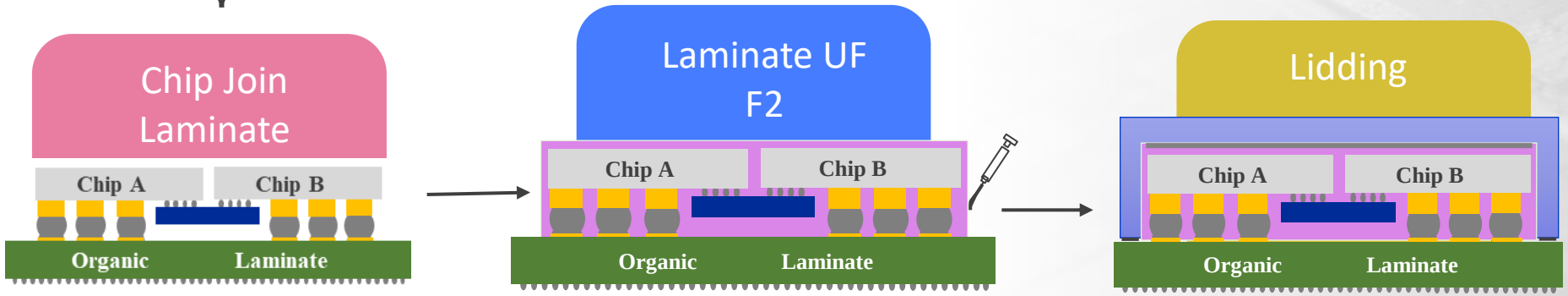
Challenge : Special fixturing to maintain alignment between all the chips in the assembly



Challenge : UF dispense through narrow gap



2. Subassembly to Laminate



Challenge : CTE mismatch between laminate and subassembly (Si)

Challenge : Filling UF within the cavity

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Reliability Results : Bridge Nets at 75µm pitch

Standard-DBHI (75µm pitch)									
Part no.	t(0)	250	500	750	1000	1250	1500	1750	2000
1*	1/29	1/29	1/29	1/29	1/29	1/29	1/29	1/29	1/29
2	0/29	0/29	0/29	0/29	0/29	0/29	0/29	0/29	0/29
3	0/29	0/29	0/29	0/29	0/29	0/29	0/29	0/29	0/29
4	0/29	0/29	0/29	0/29	0/29	0/29	0/29	0/29	0/29
5	0/29	0/29	0/29	0/29	0/29	0/29	0/29	0/29	0/29
Surface - DBHI (75µm pitch)									
1	0/29	0/29	0/29	0/29	0/29	0/29	0/29	0/29	0/29
2	0/29	0/29	0/29	0/29	0/29	0/29	0/29	0/29	0/29
3	0/29	0/29	0/29	0/29	0/29	0/29	0/29	0/29	0/29
4	0/29	0/29	0/29	0/29	0/29	0/29	0/29	0/29	0/29
5	0/29	0/29	0/29	0/29	0/29	0/29	0/29	0/29	0/29

*Tested over 20 parts per condition

DTC testing conditions :
-40°C/+125 ° C
JEDEC criteria for passing is 850 cycles

Standard DBHI

- t(0) yield issue
- 100% pass in extended DTC cycling

Surface DBHI

- 100% Yield
- 100% pass in extended DTC cycling

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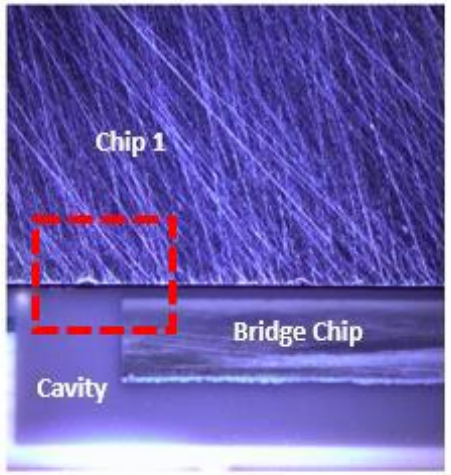
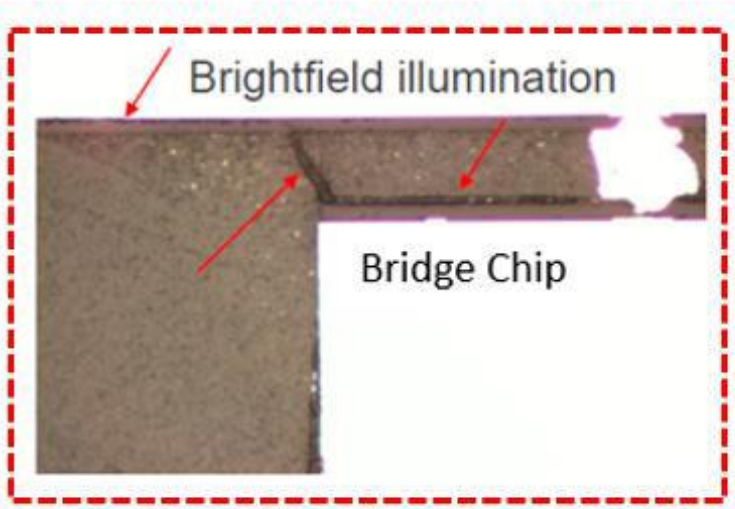
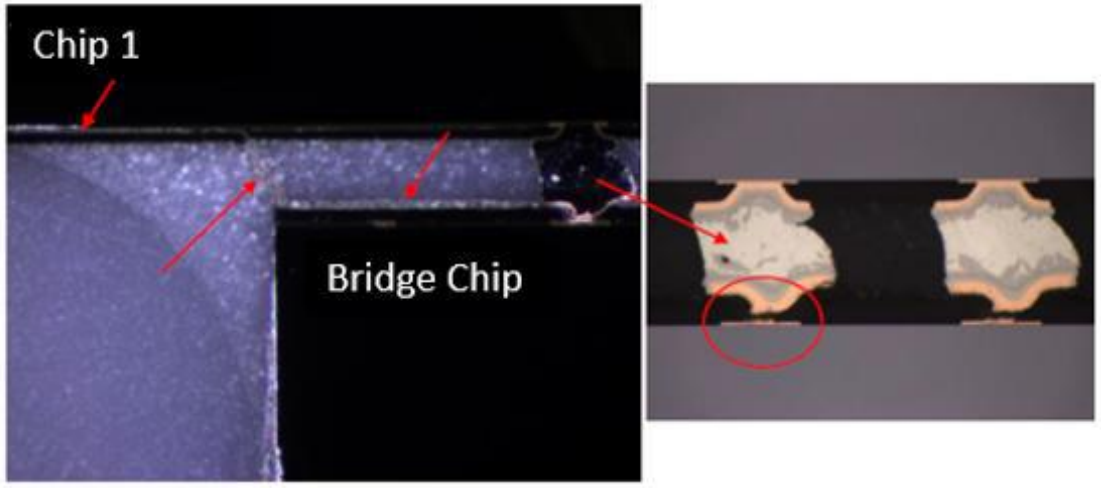
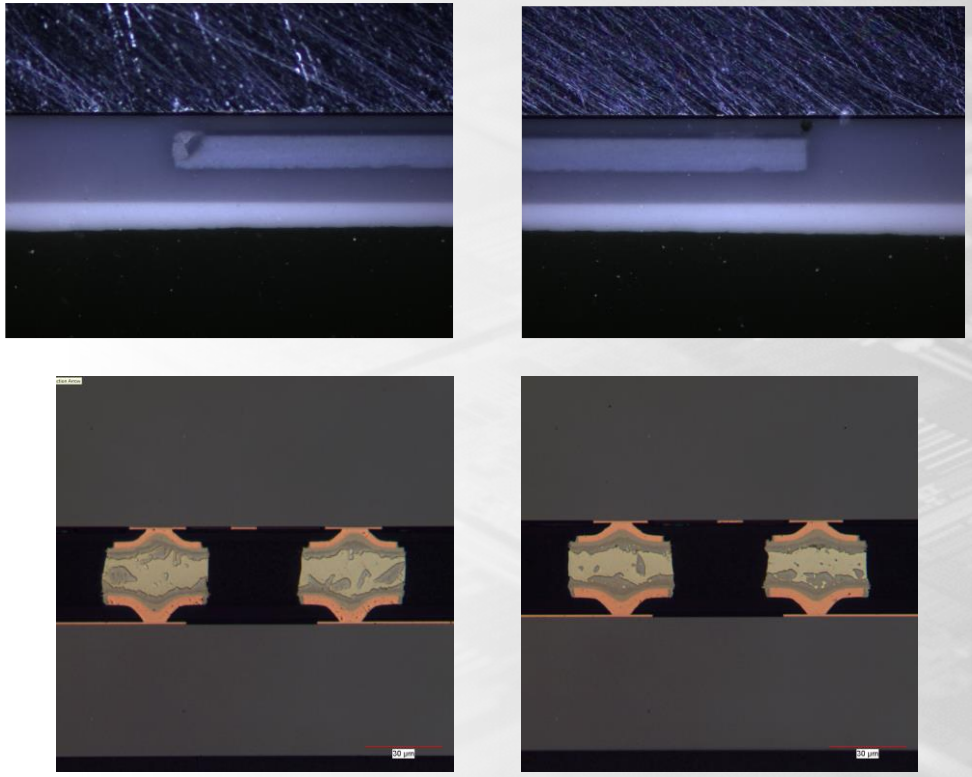
Analysis after extended DTC in bridge area





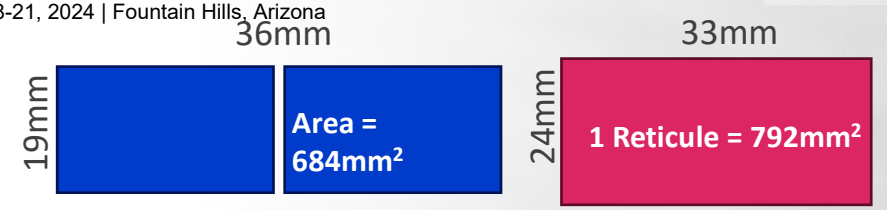


Standard DBHI : Failures are observed in UF that propagates to µC4 region within Bridge after >2000 DTC cycles



Surface DBHI : Failures are not observed electrical testing and in post analysis also. X-section after >2000 DTC cycles.

Physical Analysis in High DNP area



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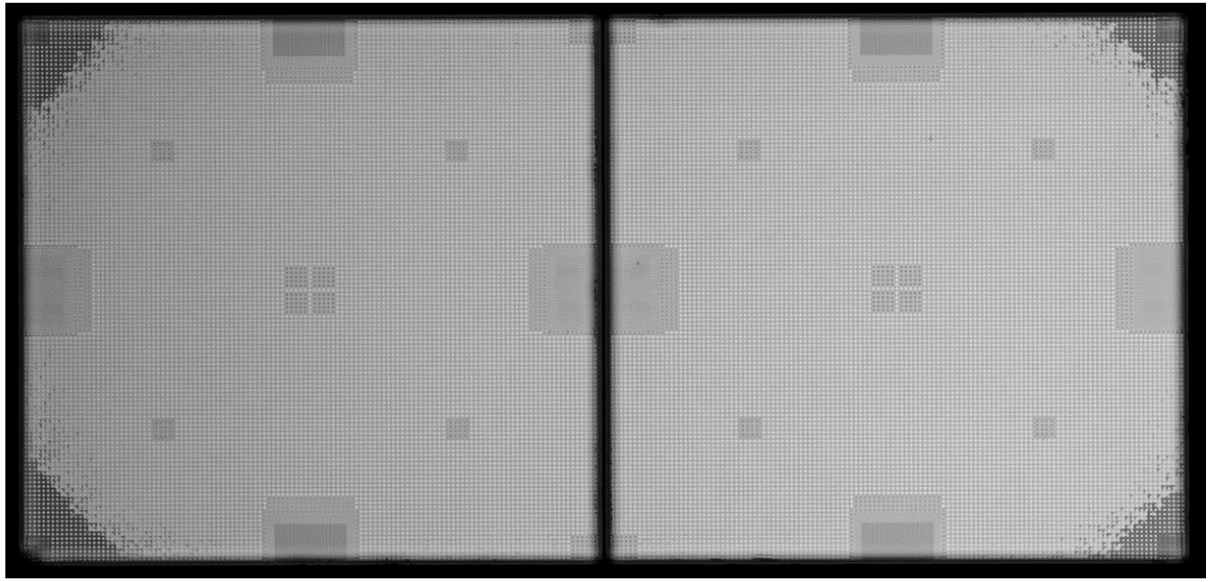
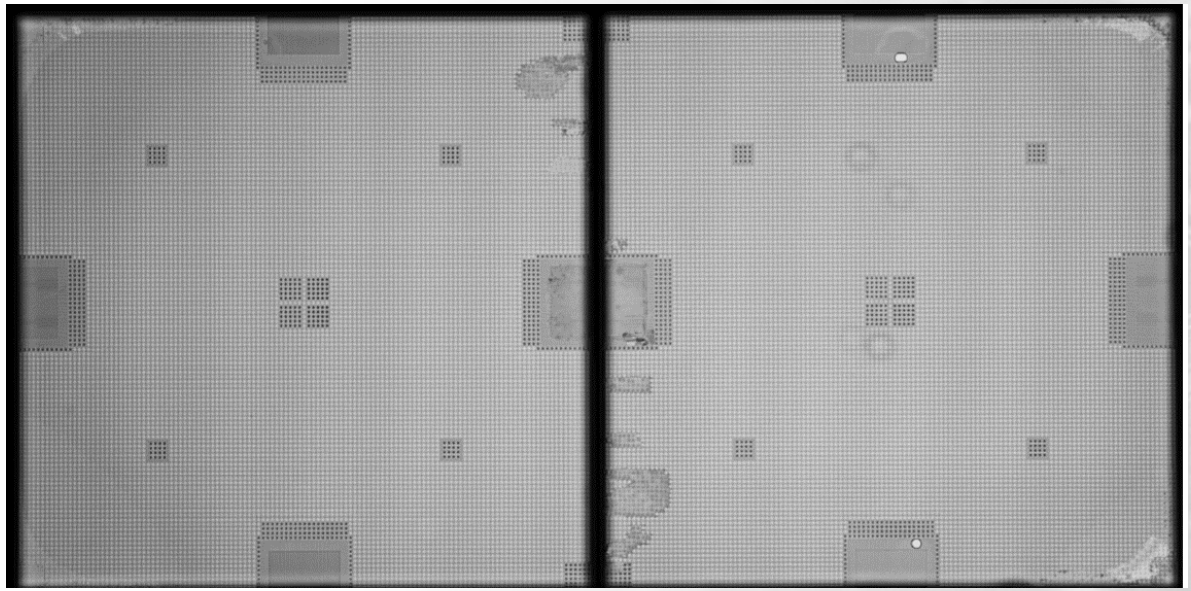
Scanning Acoustic Analysis after extended cycles of DTC



Standard DBHI



Surface DBHI

No stiffener is used

Surface DBHI shows lesser impact of stress at chip corners than Standard DBHI

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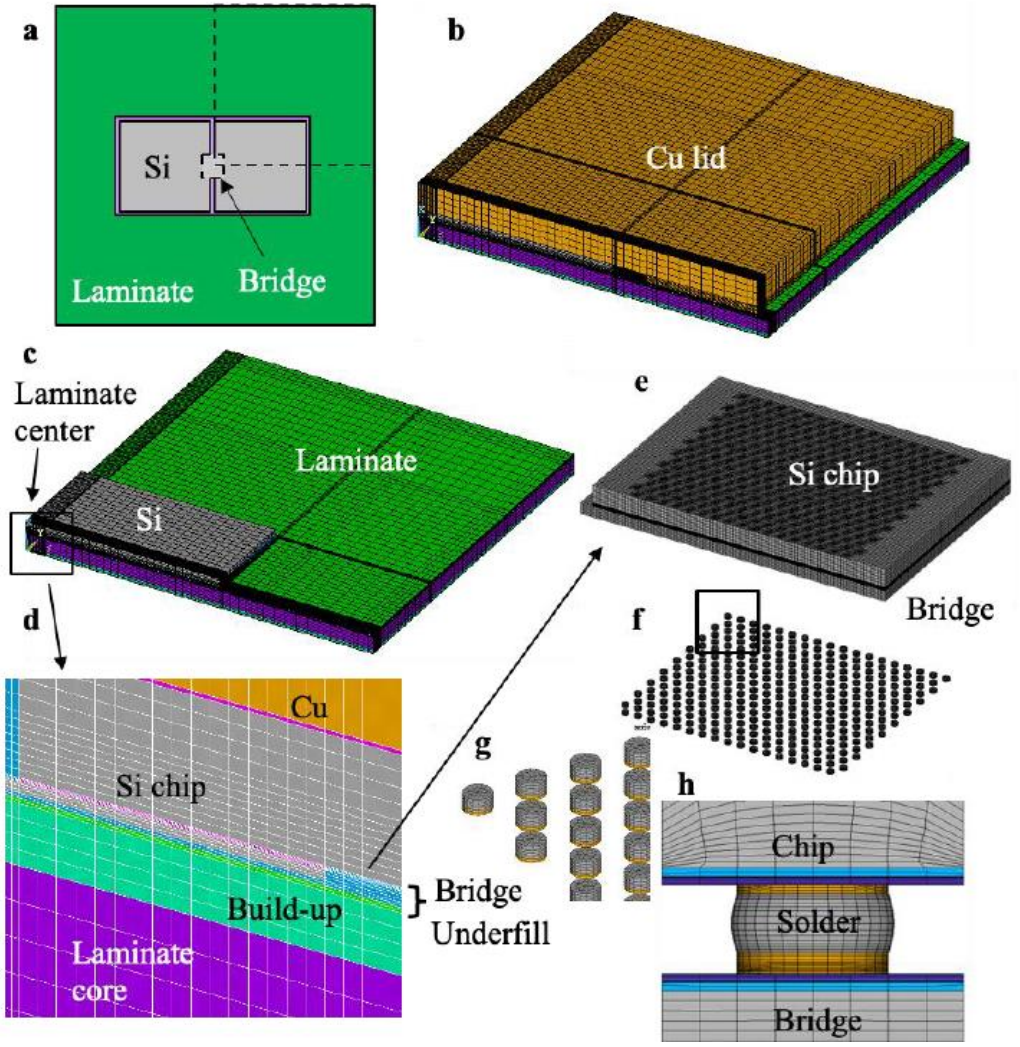
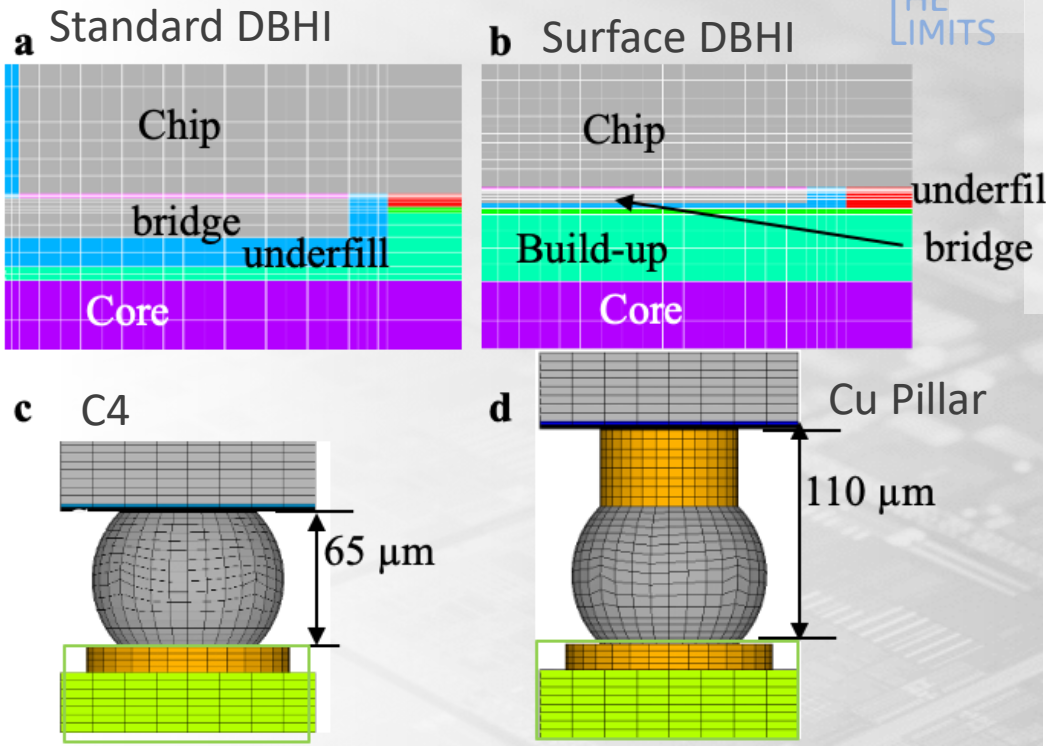
Finite Element Model for DBHi package





	Standard DBHI	Surface DBHI
UF Stress	X	0.42X
C4 Stress	Y	0.6Y
µC4 Strain	Z	0.8Z

Stresses are lesser in Surface DBHI than Standard DBHi, which explains the Extended DTC cycling results

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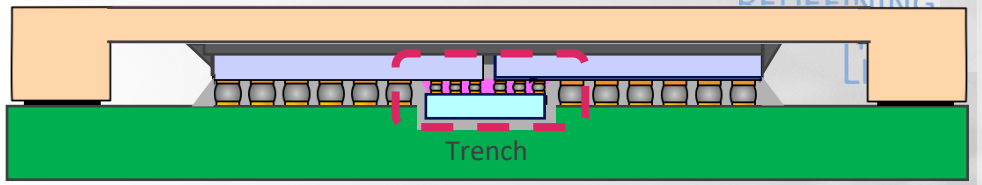
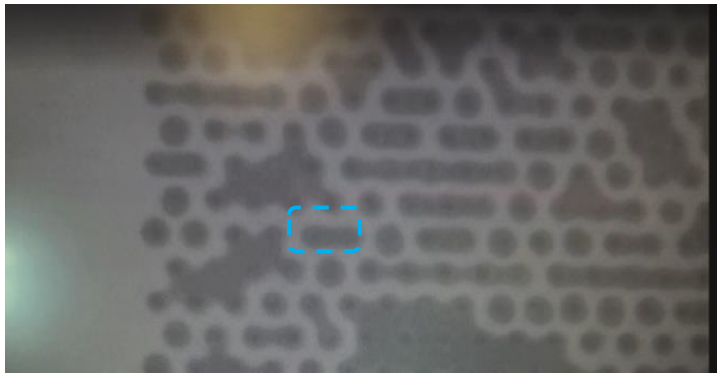
Finer pitch at Bridge region – 30µm

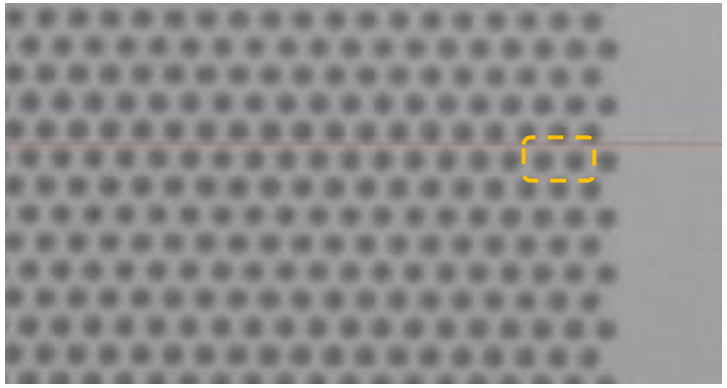


Main challenges for very fine pitch subassembly : Solder height to diameter ratio

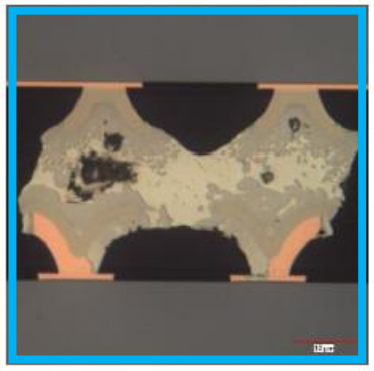
Non-optimized solder volume

X-RAY of Subassembly

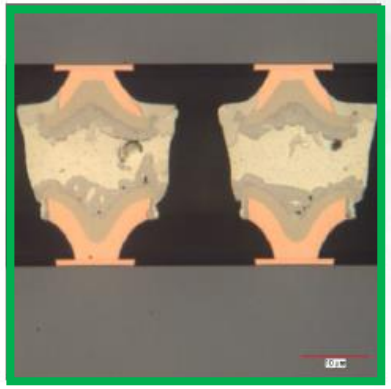


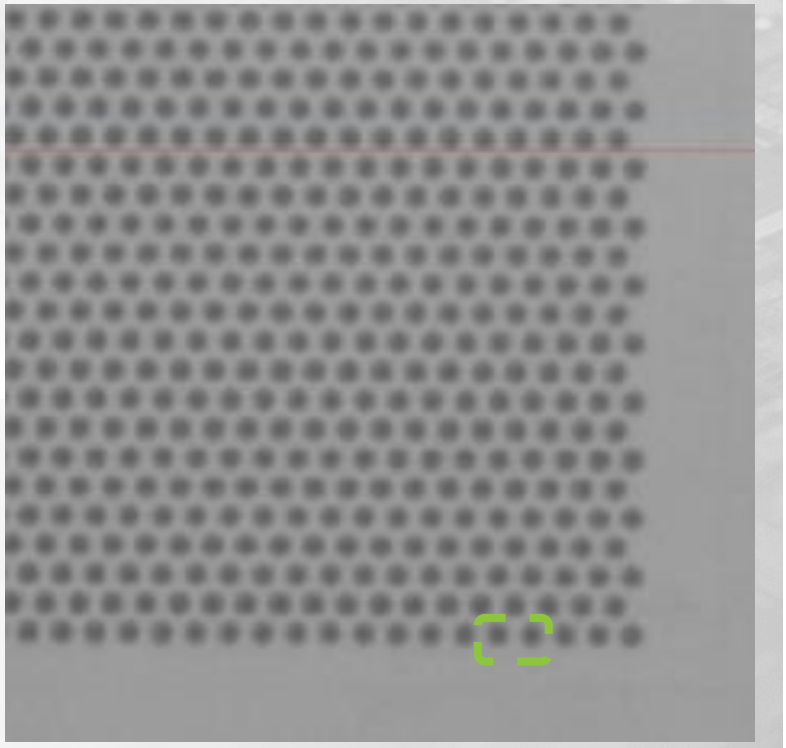


X--section



Optimized solder volume





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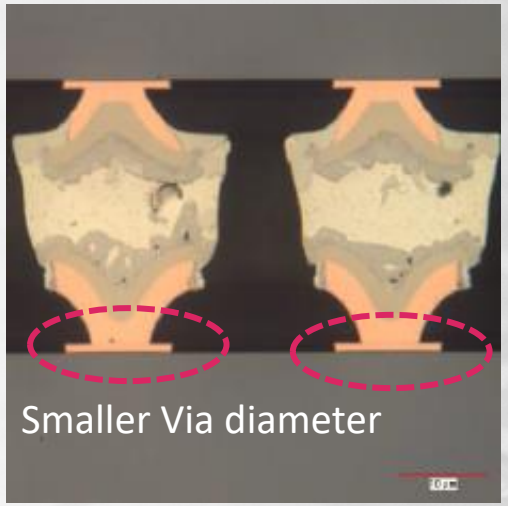
Results for 30µm pitch



Standard DBHI – 30µm pitch					
Part no.	t(0)	250 cycles	500 cycles	750 cycles	1000 cycles
1	0/29	1/29	1/29	2/29	2/29
2	0/29	1/29	2/29	2/29	2/29
3	0/29	1/29	4/29	4/29	5/29
4	0/29	0/29	0/29	0/29	0/29
5	0/29	0/29	0/29	0/29	0/29

- **100% Yield of the process**
- **Decent Reliability (DTC) results, but room for improvement**

Reliability can be further improved:

•Using Surface DBHI architecture (as seen in case of 75µm pitch)

•By increasing via diameter thus changing BLM structure

Conclusions

DBHi Architecture with 75µm pitch Bridge Region

- Successfully demonstrated Bond and Assembly Process
- Reliability testing demonstrated robust bridge region interconnects for both Surface and Standard DBHI w.r.t. JEDEC criteria
- Surface DBHI architecture is robust as shown by extended DTC cycling (>2000 cycles) and explained by Finite element modelling

DBHI Architecture with 30µm pitch Bridge Region :

- Successfully demonstrated Bond and assembly process with 100% yield
- DTC results (500 cycles) looks promising

Future Work:

- 30µm pitch bridge reliability analysis with Surface DBHI architecture and modified BLM
- To extend DBHI architecture to multiple chiplet integration
- For some applications (& in accordance with UCIe), bridge needs power supply.
  - Solution : Bridge with TSVs where bridge is connected to the laminate as well

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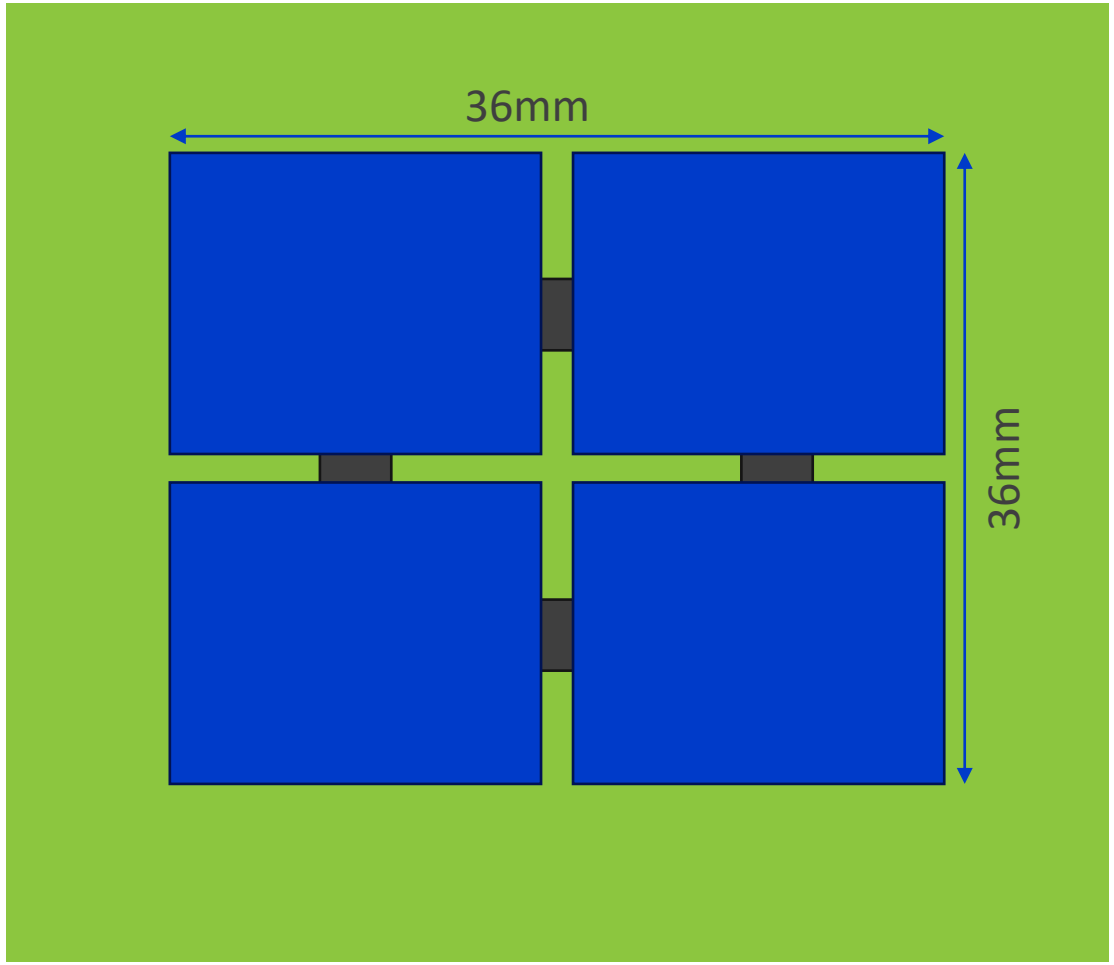
Upcoming Presentation on DBHI



Work on Multiple Chip DBHI will be presented in ECTC 2024 by Akihiro Horibe

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Special Acknowledgements

Claudia C. B. Pulido, Serge Martel, Anthony Buissoneault, Rock Cabana, Amelie Rachine and Genevieve Beaulieu
IBM Bromont
Frank Libsch, *IBM Research*

Thanks for your Attention

IBM