Advanced Packaging

Enabling the Future of Moore's Law

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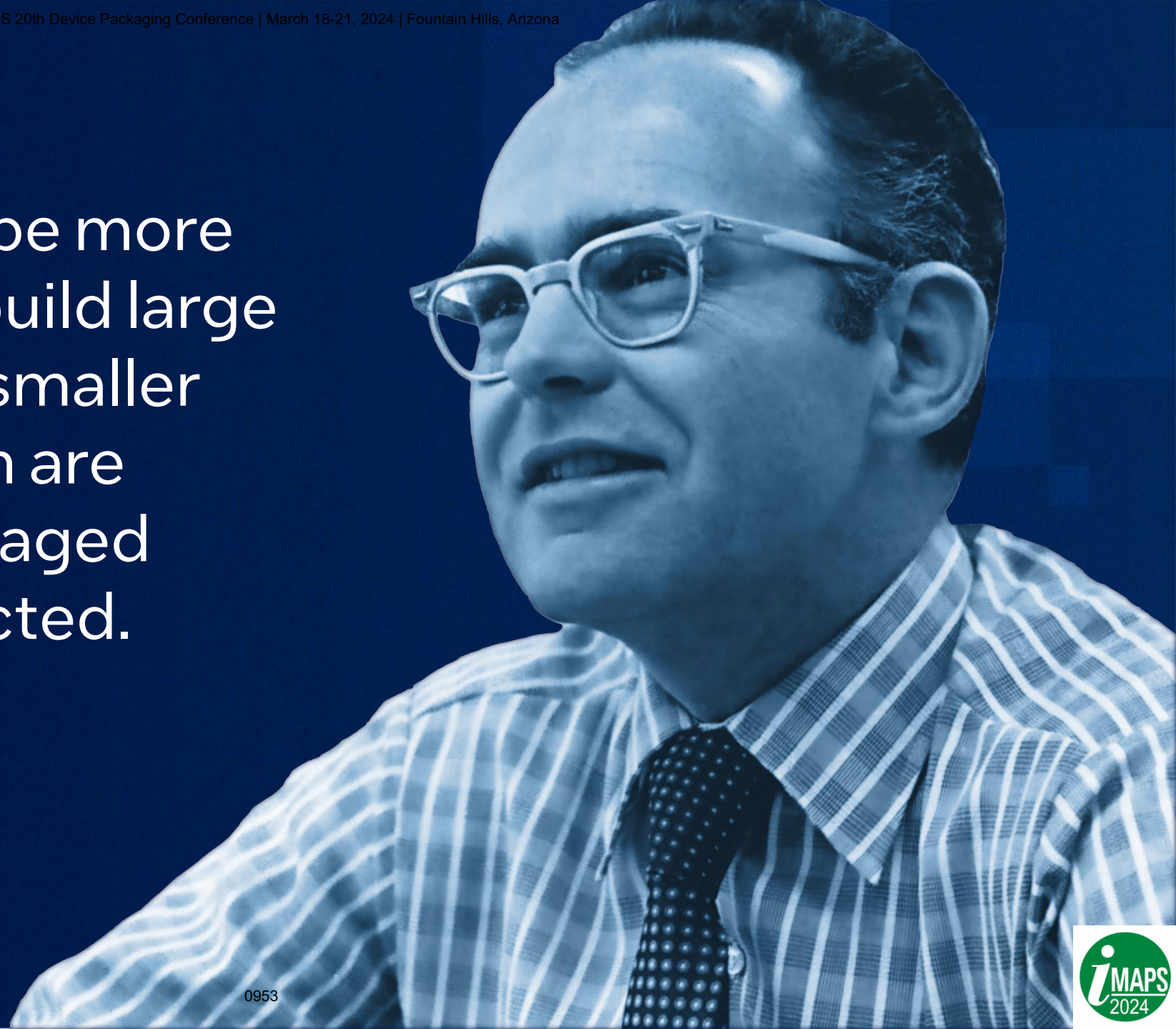
Executive Summary

- Industry is trending towards more complex integration schemes to address cost and scalability challenges
- The era of 3D integration and advanced packaging is upon us, but the ecosystem is not ready
  - There are fundamental design, manufacturing, and enabling challenges that must be addressed
- Metrology, physical debug, and manufacturing test are underserved and need more focus and investment from industry and academic partners
  - “if you can’t test it, you don’t have a product”

"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected.

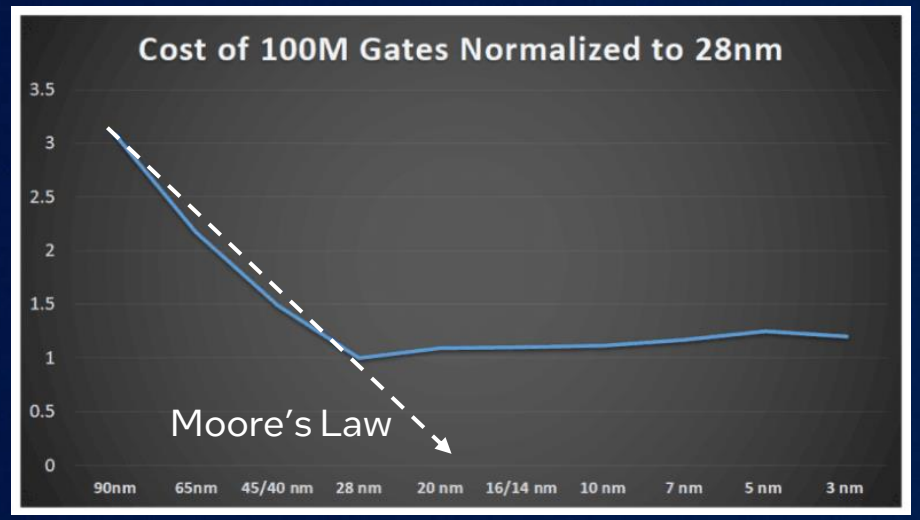
Gordon Moore
Electronics, 1965

Image credit - betanews



Technology Drivers

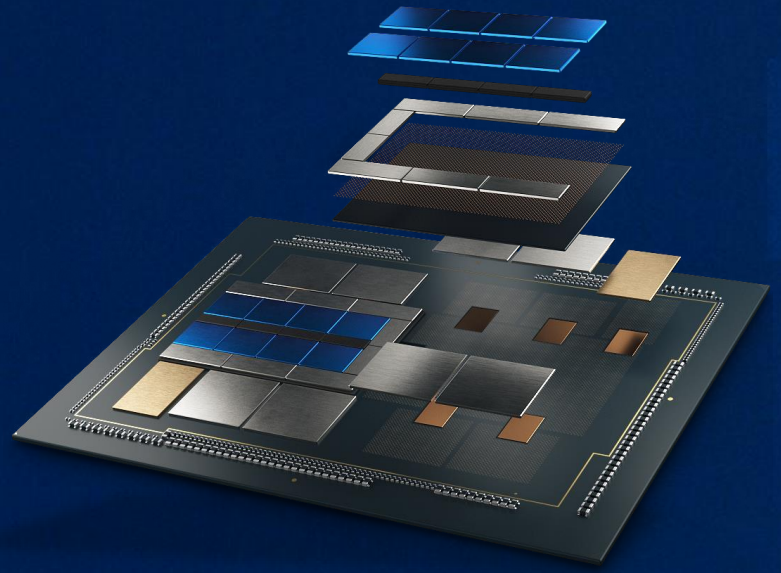
COST



Source: Google, IEDM23, SC1.6

Higher wafer cost drives disaggregation

PERFORMANCE/SCALING



Need for complex sizes that exceed the reticle limit

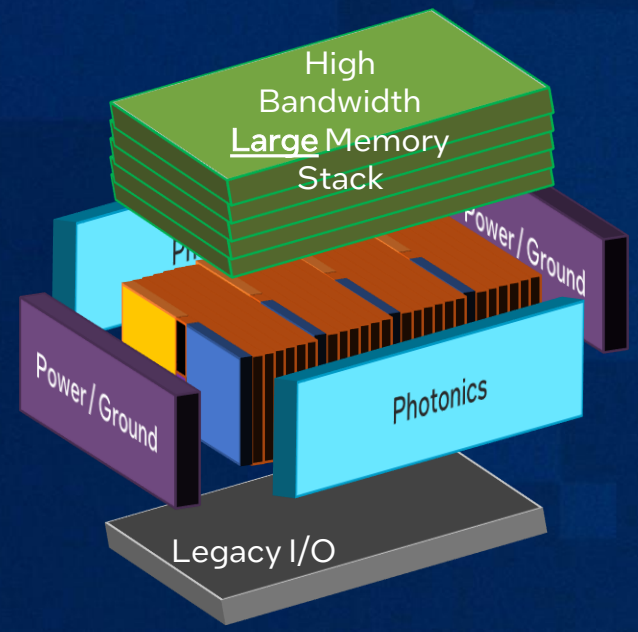
Advanced packaging is required to re-aggregate chiplets and build complexes larger than the reticle limit

Evolution of Advanced Packaging

Package main function:
provide power and signaling from motherboard to die

Added package value:
high density interconnects that enable larger die complexes from multiple process nodes

Evolution of 3D Packaging



Memory

Logic

Logic

Logic

3D today
"planar"

3D future
"cube"

3D stacking will evolve to enable more complex and integrated devices

Key Challenges: Power Delivery & Thermals

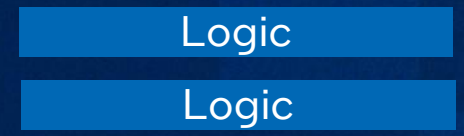
"low-power memory on top of high-power logic"

+Direct power delivery to logic die
-High-power logic die is thermally blocked

"high-power logic on top of low-power memory"

-Degraded power delivery to logic die
+Direct thermal access to high-power logic die

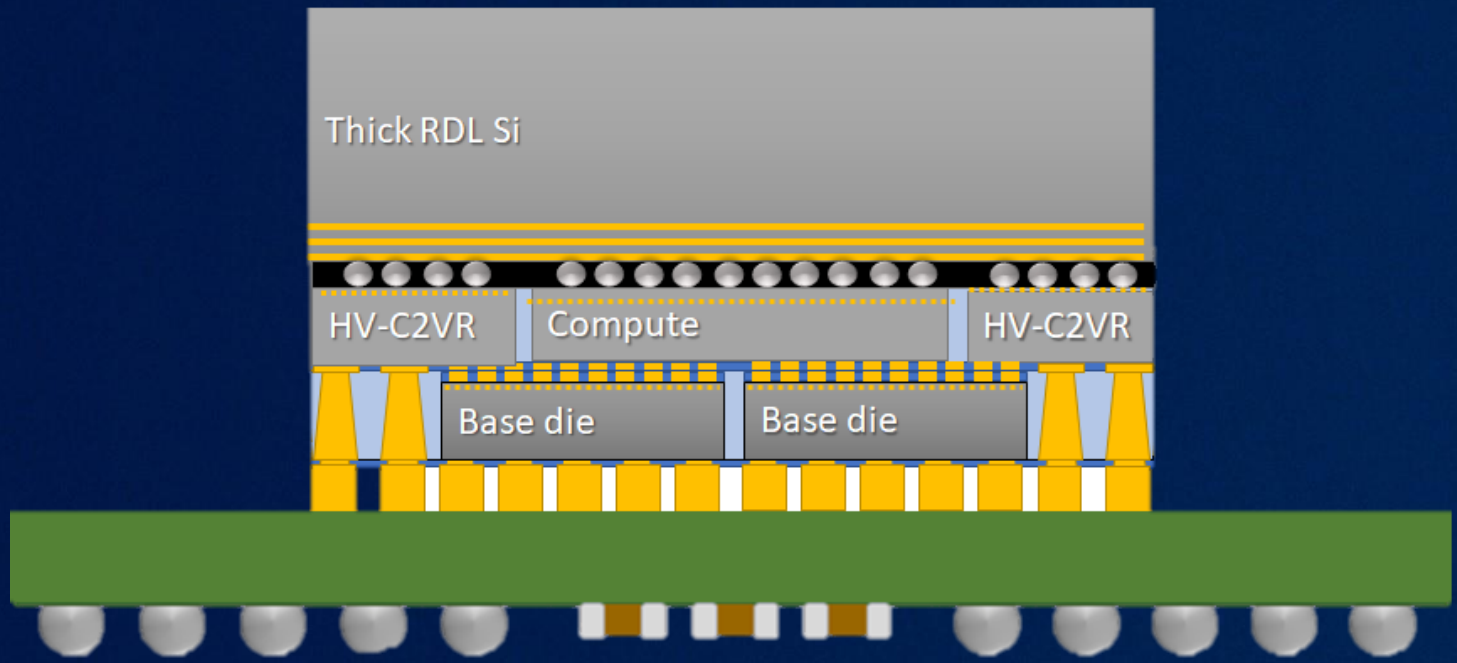
"high-power logic on top of high-power logic"



-Degraded power delivery to top die
-High-power bottom die is thermally blocked

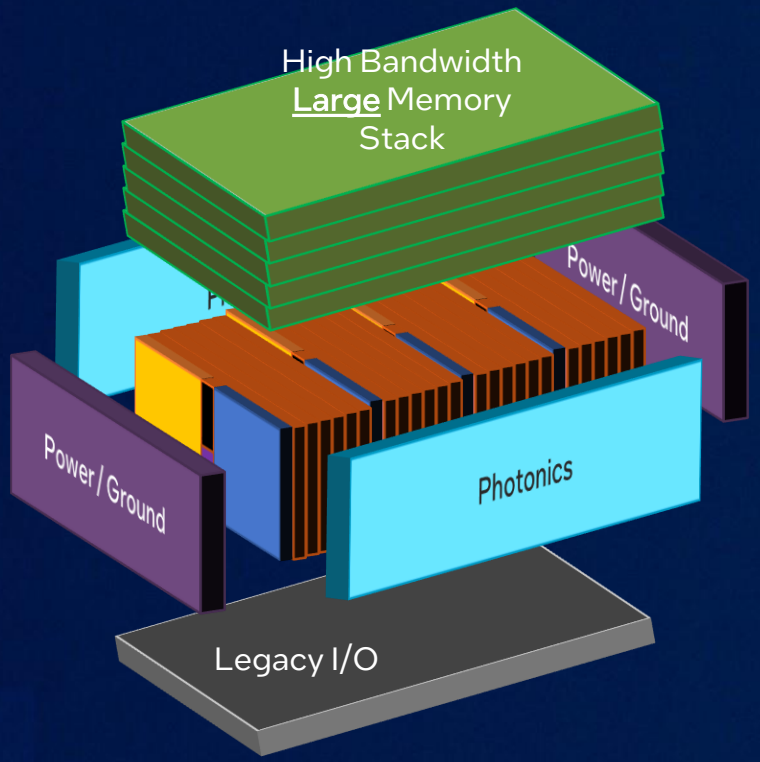
Innovations needed in power delivery and thermals to extract maximum value out of 3D stacking

Key Challenges: Power Delivery & Thermals



Topside power delivery may be a solution path, but adds cost and complexity

Key Challenges: Process & Design

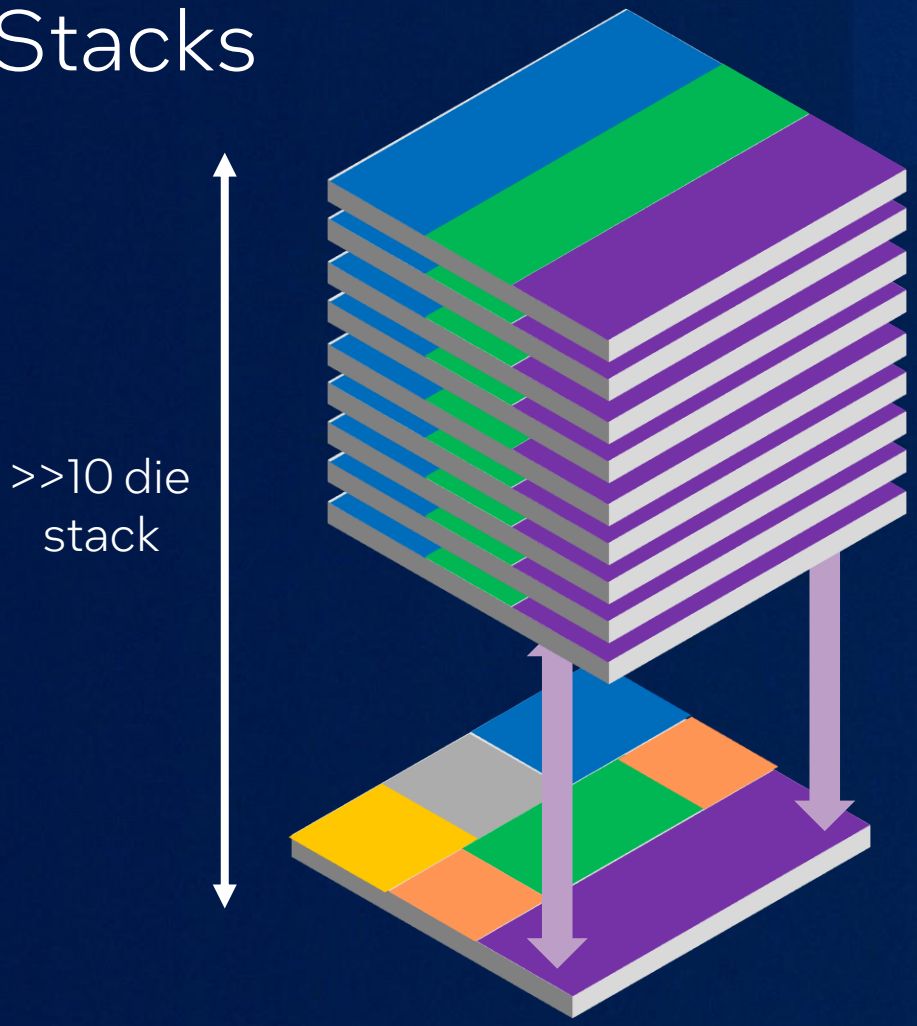


Manufacturing:
- Die/stack rotation
- Edge polish & attach
- Z-height
- Physical debug

Design:
- Die rotation & die edge egress
- Non-planar libraries
- Power delivery & thermals

New manufacturing tools & processes along with new design tools and methodologies are needed to enable “cube” architectures

Trends: Super Stacks

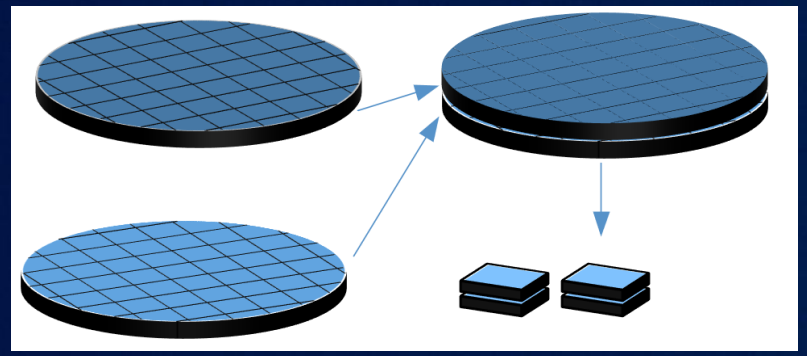


Chiplets composed of different functional blocks such as cores, memory, and IO

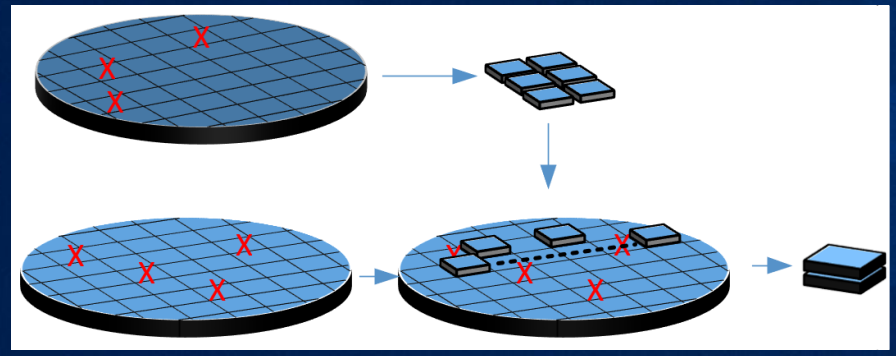
Super Stacks being proposed as a path to achieve best-in-class size, weight, power, and cost

Key Challenges: Super Stacks

Wafer-to-Wafer (W2W)



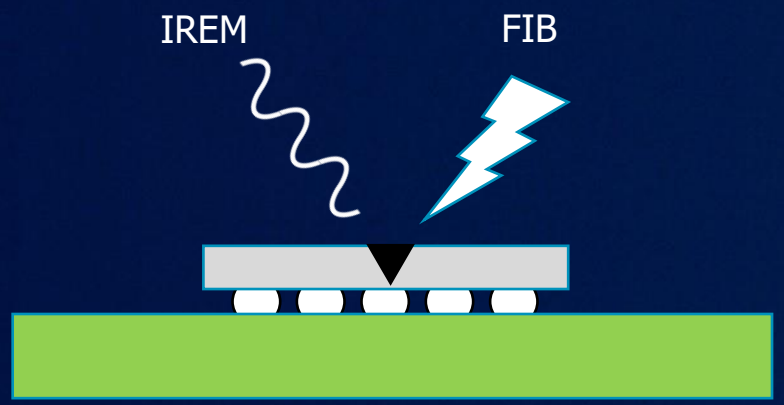
Chip-to-Wafer (C2W)



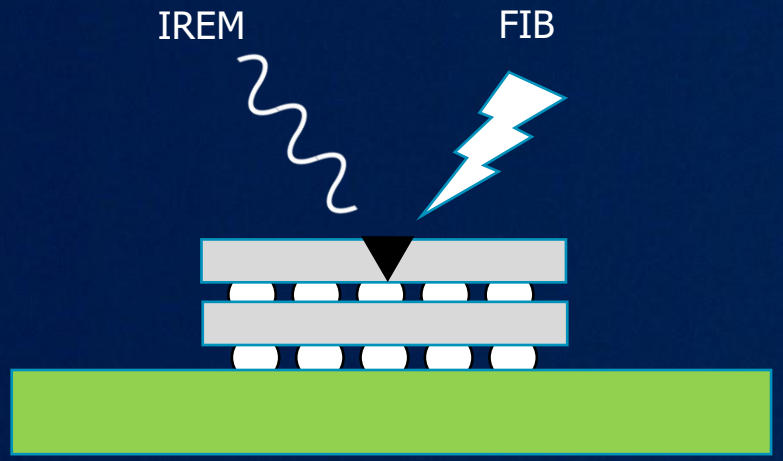
More mature, faster throughput	Less mature, slower throughput
Currently finer pitch	Currently coarser pitch with roadmap to finer pitch
Stacked die must be the same size	No limitations on stacked die relative sizes
Random pairing of die	Intelligent pairing of die
Cumulative yield issue (all die must work)	No cumulative yield (all die are tested before attach)

New tools and flows needed to enable economically viable Super Stacks

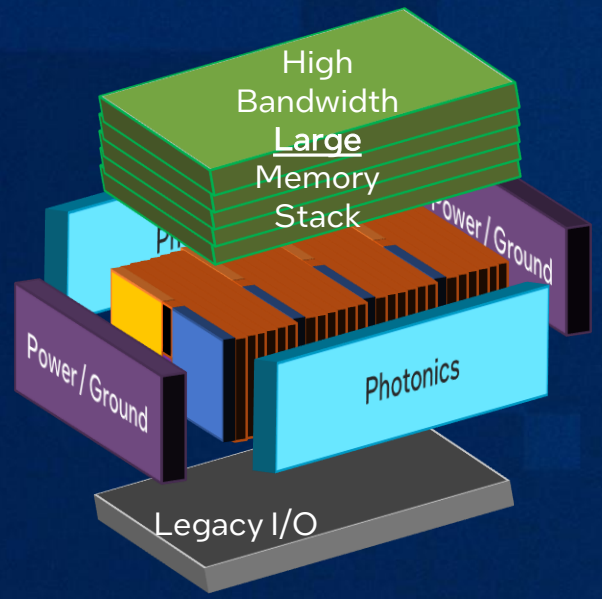
Key Challenges: Physical Debug



All transistors are **accessible**



Bottom die transistors are blocked by the top die and are **inaccessible**



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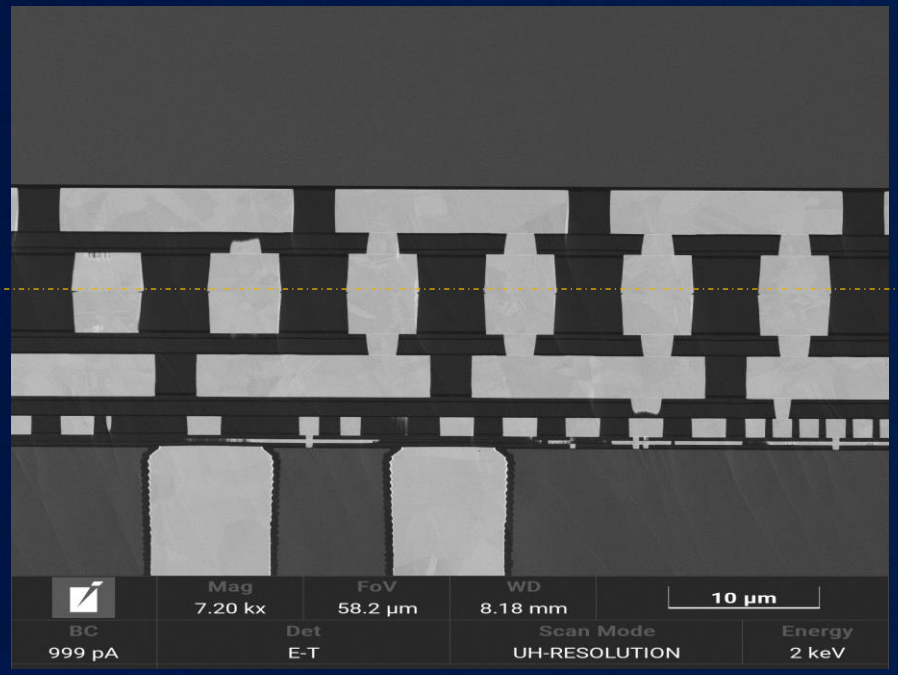
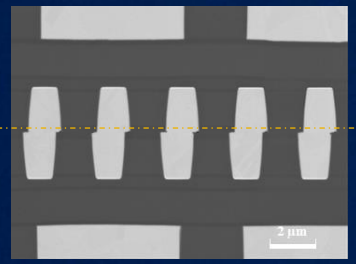
Need new physical debug techniques to enable more complex stacking strategies

Trends: Pitch Scaling

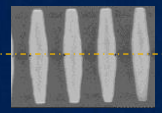
9 um pitch



3 um pitch



1 um pitch



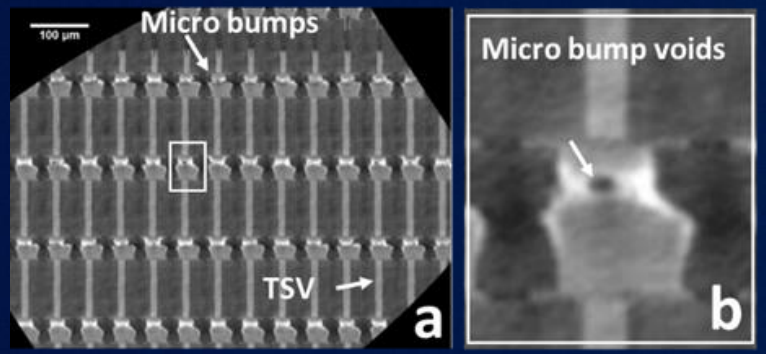
0.4 um pitch

time

Cu-Cu hybrid bonding enables aggressive pitch scaling to ≤1 um

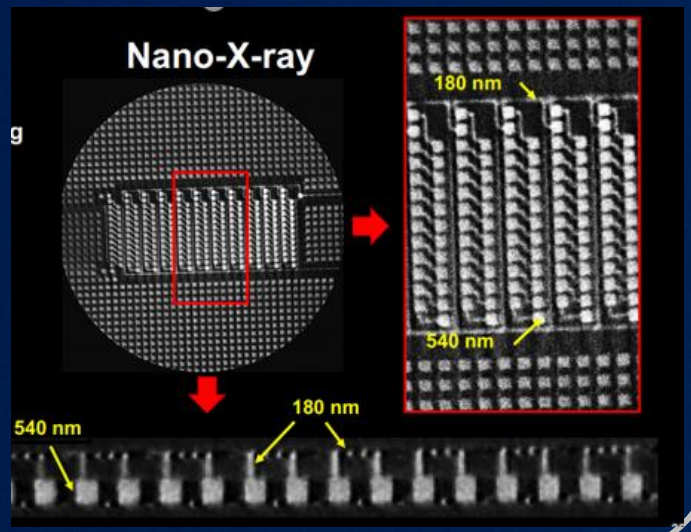
Key Challenges: Defect Detection

Typical 3D X-ray for interconnect defects; no sample prep is needed



Cheryl Hartfield et. al. DOI: 10.1109/IPFA.2018.8452551

Nano 3D X-ray with <1um res.; sample preparation is needed

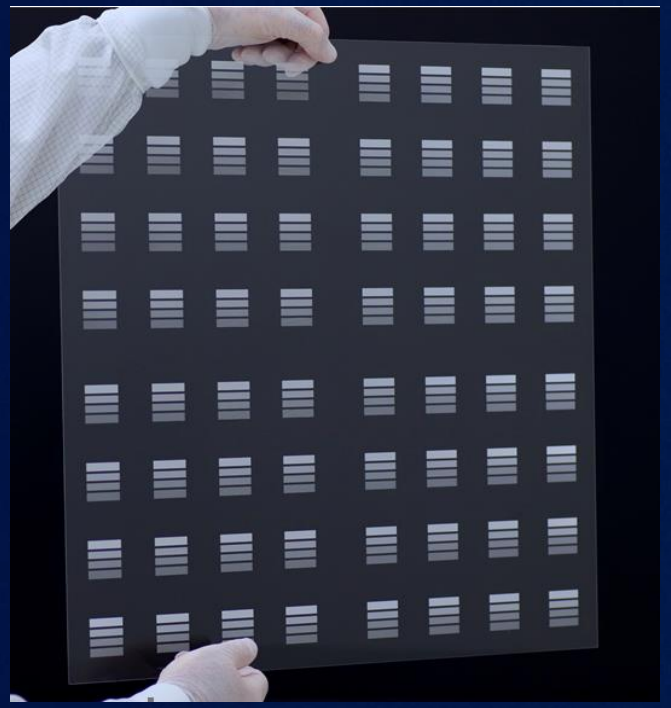


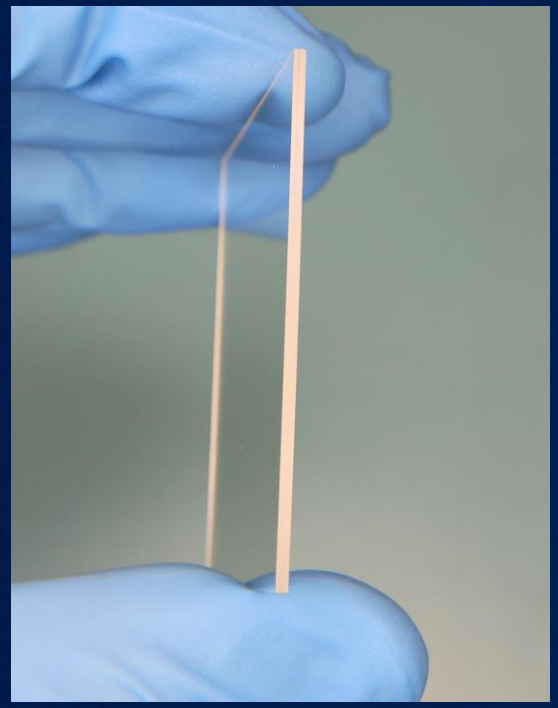
Christian Schmidt, Lorenz Lechner, Ingrid DeWolf, Soon-Wook Kim, Eric Beyn ECTC 2018

Sample prep and long scanning time needed to reach high resolution for fine pitch features will slow down yield learnings and impact time to market

Need innovations in imaging and FA methods to quickly and non-destructively catch sub-micron defects buried under multiple interfaces

Trends: Glass Substrates

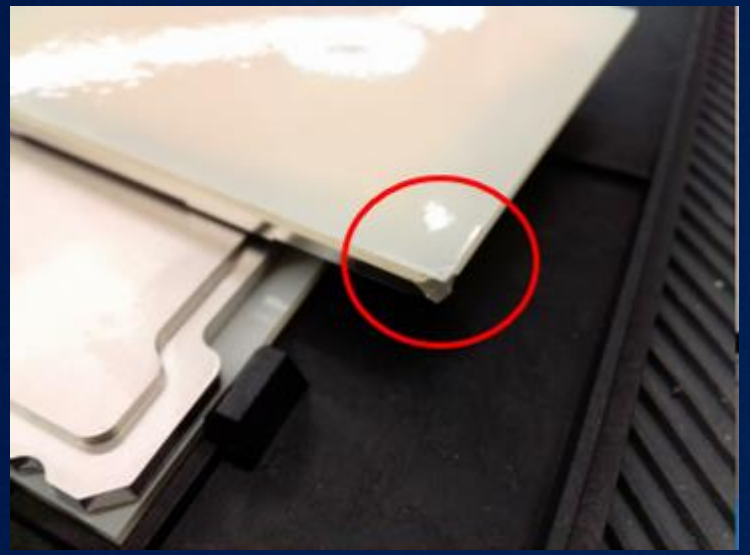




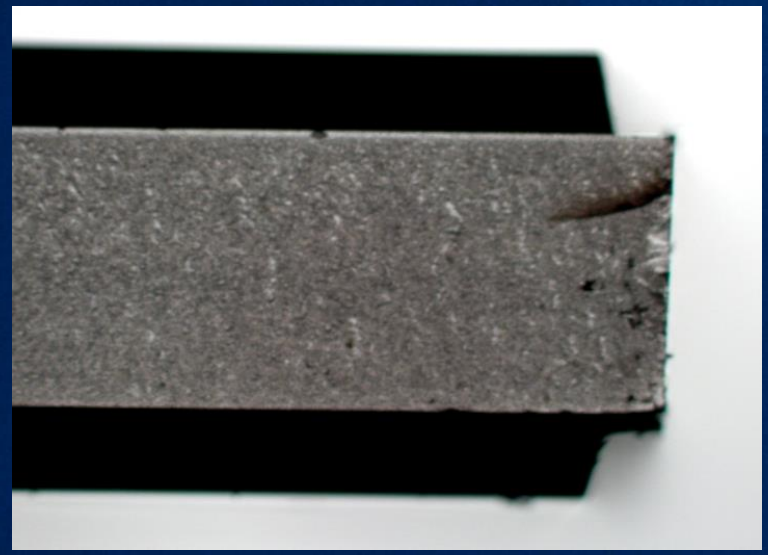
Glass offers improved material properties resulting in better dimensional stability and ability to scale

Key Challenges: Process & Metrology

Edge defects due to singulation



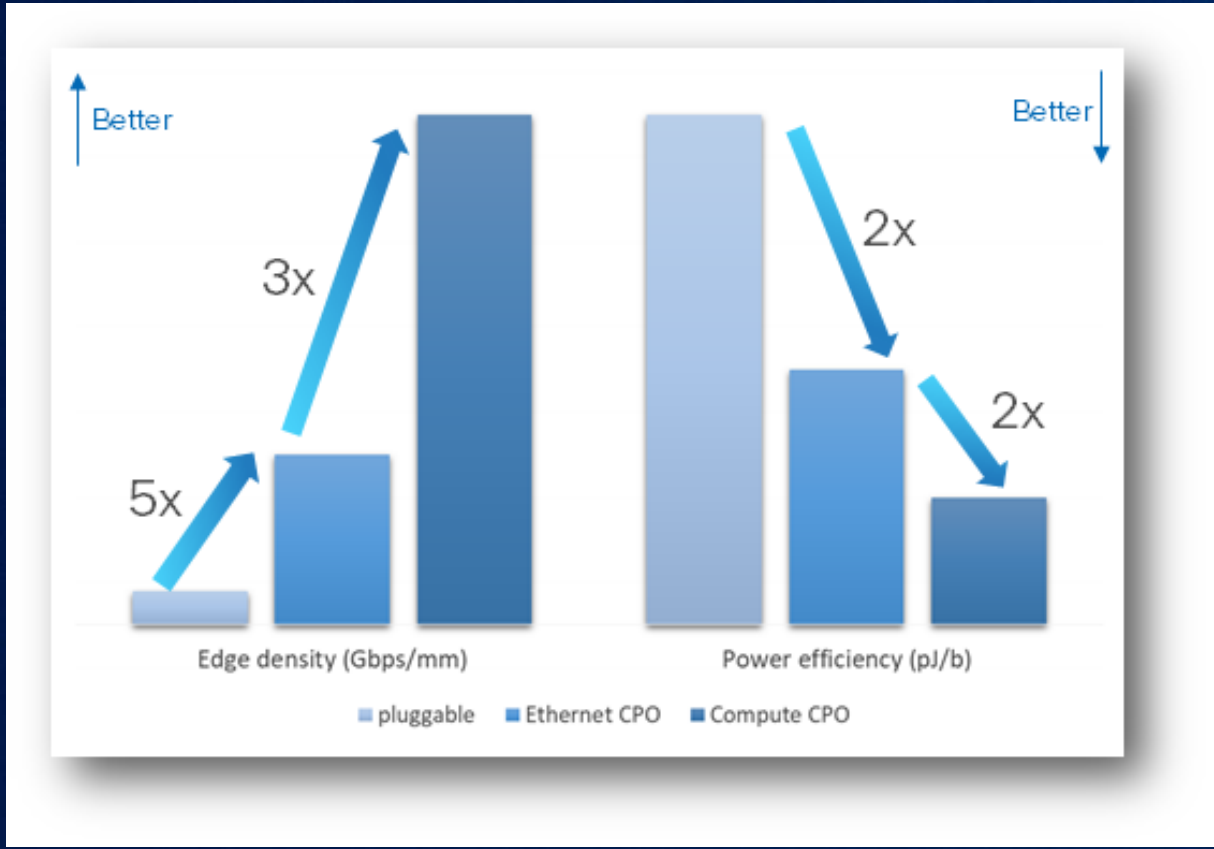
Corner chipping due to material handling



Cracks that can become gross fails if undetected

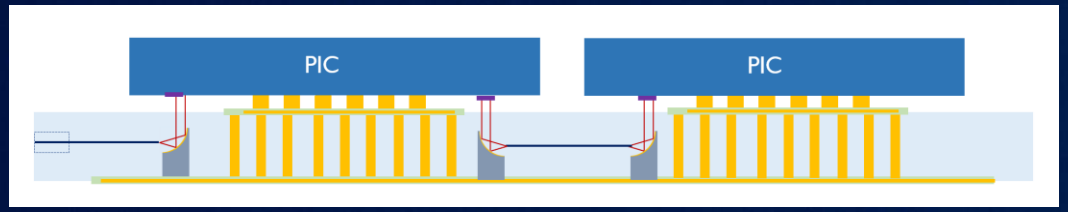
New processing techniques, material handling, and in-line metrologies required to enable manufacturing of glass substrates

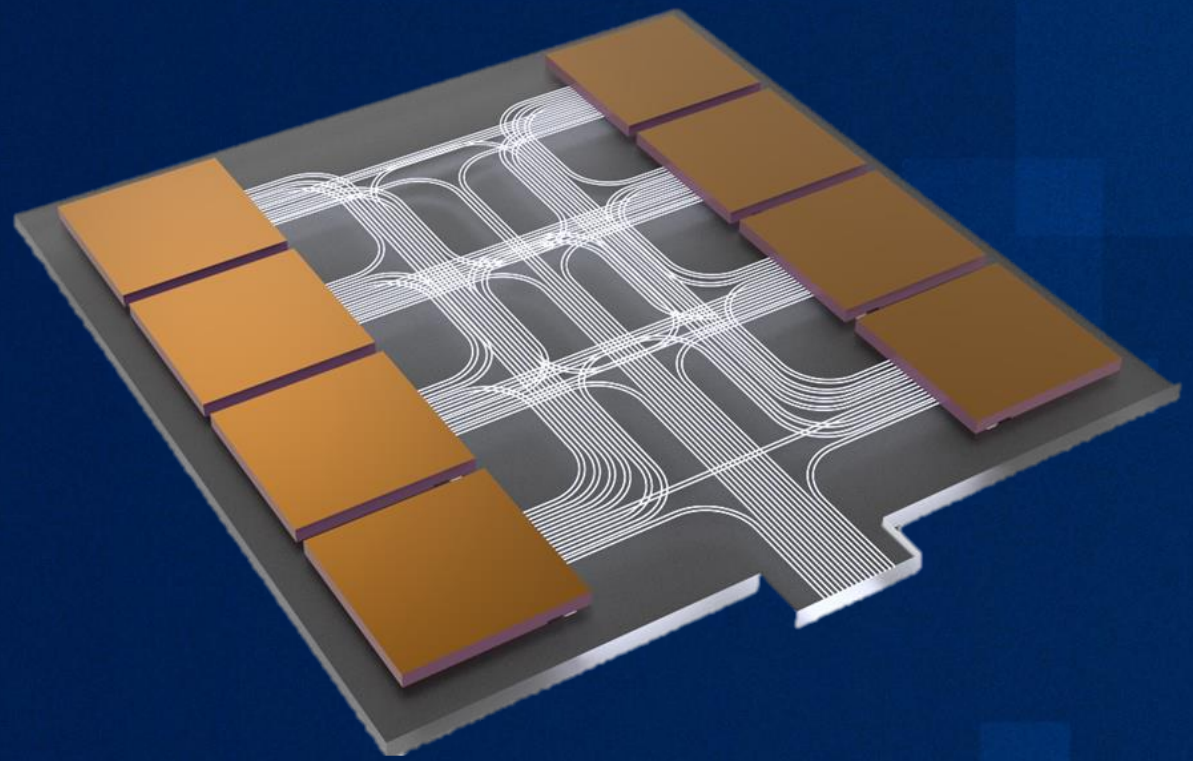
Trends: Co-Packaged Optics



Co-packaged Optics will grow bandwidth/socket and improve IO power efficiency

Key Challenges: Optical Integration in Glass Substrates



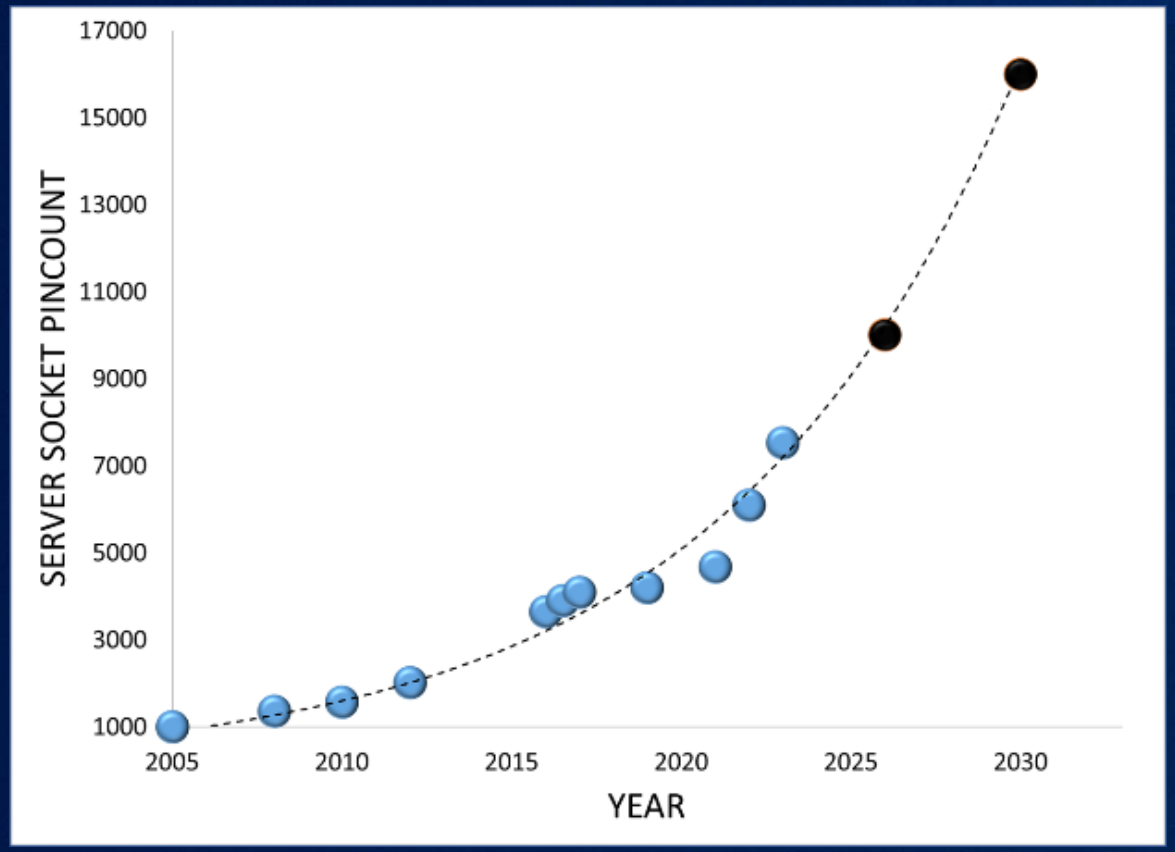


Key building blocks:

- *Lower propagation loss waveguides*
- *Programmable waveguide mesh*
- *EDA tool for electrical/optical design*
- *Faster waveguide writing*
- *Better/faster waveguide metrology*

Full optical integration in glass substrates for chip-to-chip communication in large-scale systems

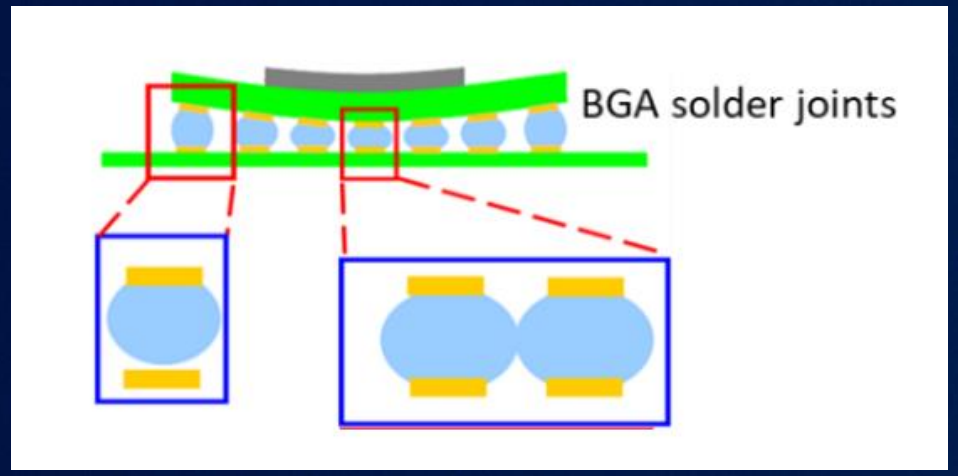
Trends: Larger Substrates with Higher Pincounts



Larger complexes drive larger packages which leads to an exponential increase in pincount

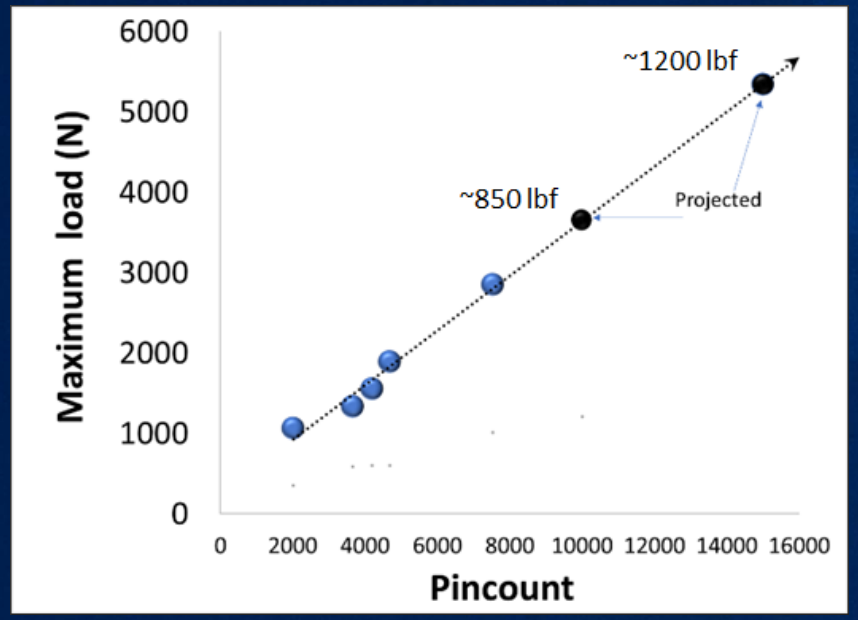
Challenges: Board Attach

Ball Grid Array (BGA)



Larger packages result in higher warpage which lead to a less reliable surface mount process

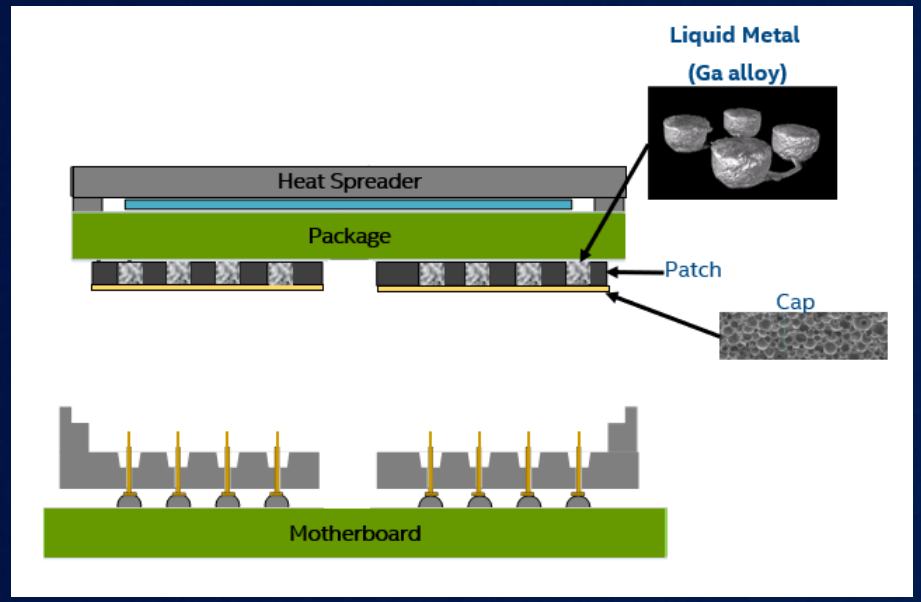
Land Grid Array (LGA)

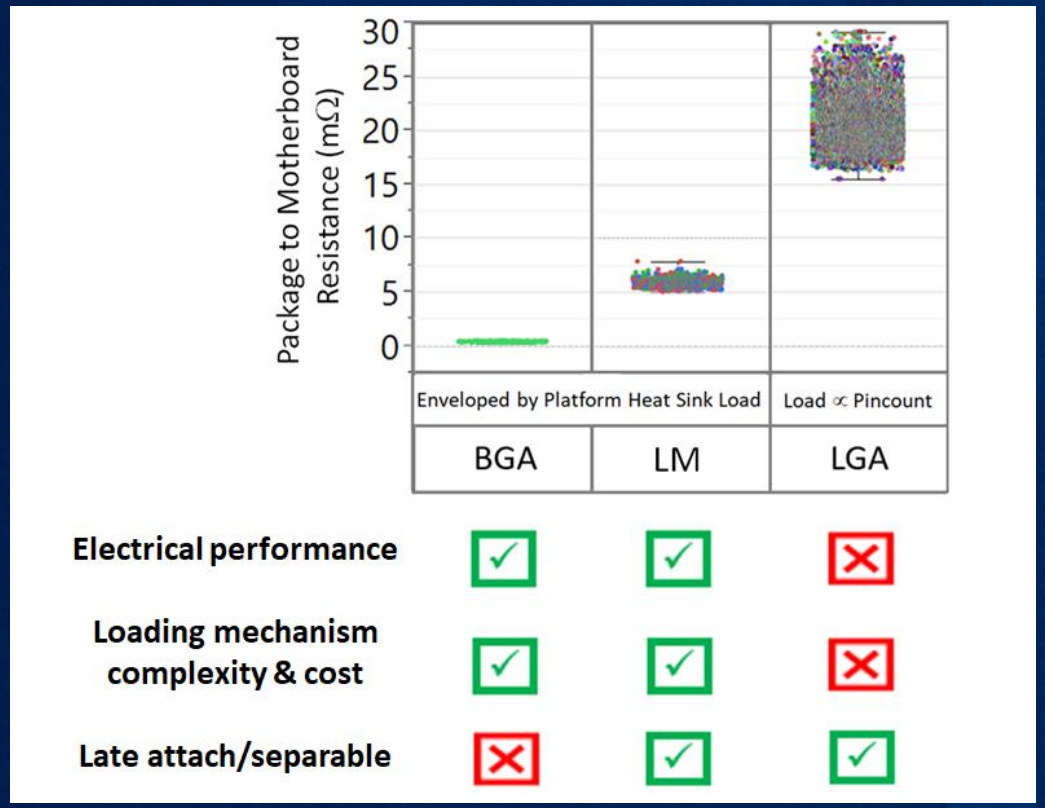


As pin count grows, the total sustained load required by the socket grows linearly

Larger packages with higher pincount challenge both BGA and LGA solutions

Challenges: Board Attach



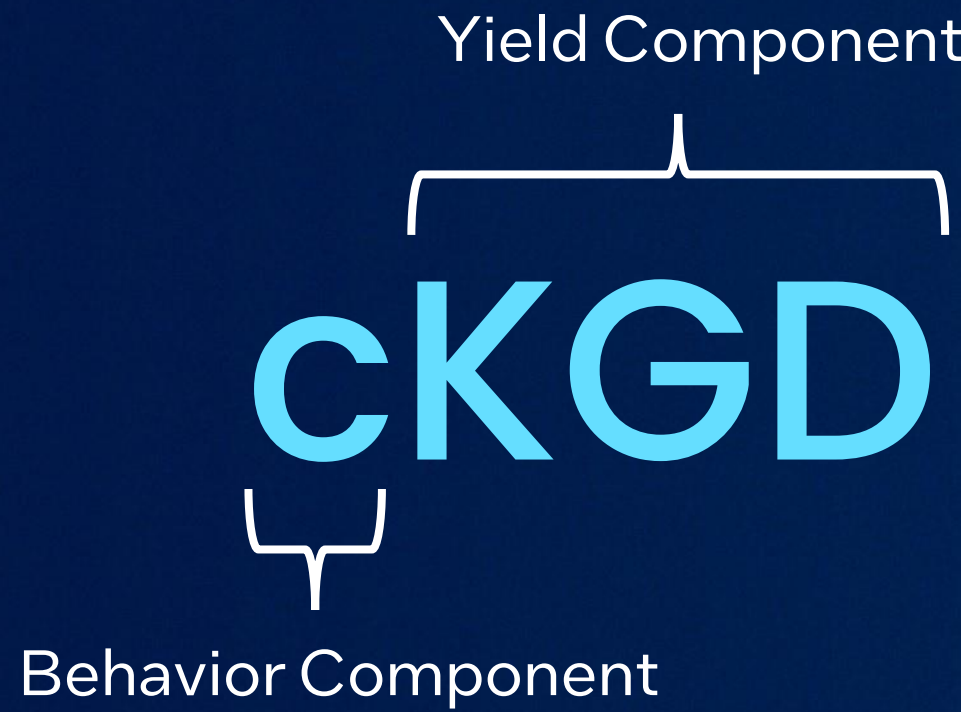


Liquid metal (LM) offers a ~zero load interconnect that has the goodness of BGA and the flexibility of LGA, but requires significant ecosystem maturation

Key Challenges: Test

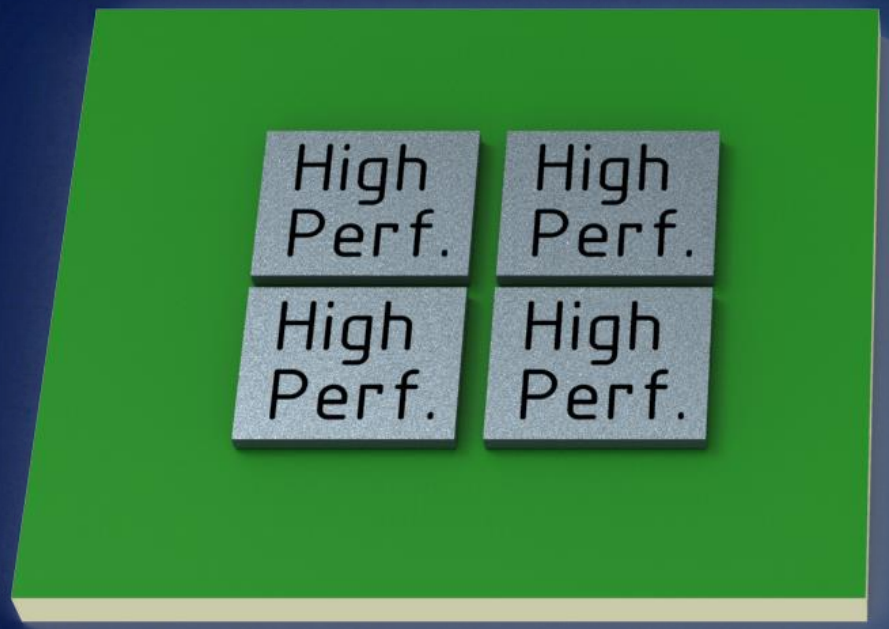
Characterized Known-Good-Die (cKGD) out of wafer test is critical to making 3DIC economically viable

What is cKGD?

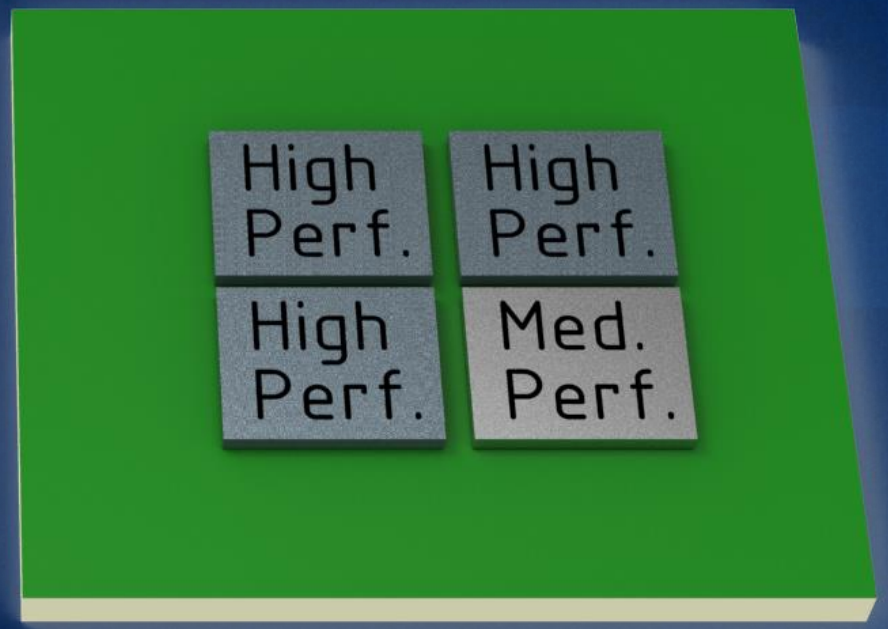


Wafer test needs to not only catch defects, but also provide an accurate assessment of device behavior for optimal die pairing decisions

Importance of Characterization



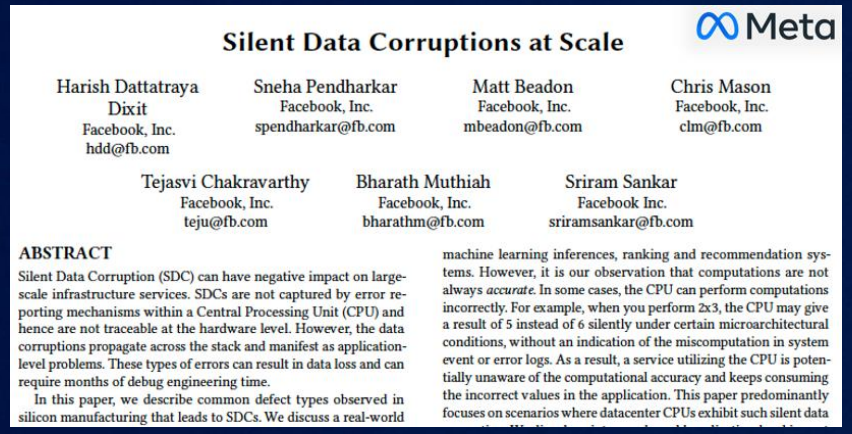
Shipped as high performing part



Shipped as medium performing part

Characterization of device behavior/performance and intelligent pairing is needed to maximize performance

cKGD Challenges



Meta

Silent Data Corruptions at Scale

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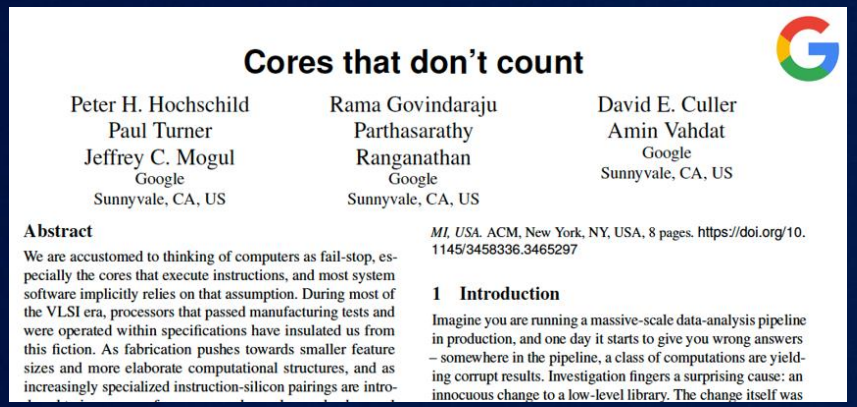
ABSTRACT

Silent Data Corruption (SDC) can have negative impact on large-scale infrastructure services. SDCs are not captured by error reporting mechanisms within a Central Processing Unit (CPU) and hence are not traceable at the hardware level. However, the data corruptions propagate across the stack and manifest as application-level problems. These types of errors can result in data loss and can require months of debug engineering time.

In this paper, we describe common defect types observed in silicon manufacturing that leads to SDCs. We discuss a real-world machine learning inferences, ranking and recommendation systems. However, it is our observation that computations are not always *accurate*. In some cases, the CPU can perform computations incorrectly. For example, when you perform 2x3, the CPU may give a result of 5 instead of 6 silently under certain microarchitectural conditions, without an indication of the miscomputation in system event or error logs. As a result, a service utilizing the CPU is potentially unaware of the computational accuracy and keeps consuming the incorrect values in the application. This paper predominantly focuses on scenarios where datacenter CPUs exhibit such silent data



Cores that don't count

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Abstract

We are accustomed to thinking of computers as fail-stop, especially the cores that execute instructions, and most system software implicitly relies on that assumption. During most of the VLSI era, processors that passed manufacturing tests and were operated within specifications have insulated us from this fiction. As fabrication pushes towards smaller feature sizes and more elaborate computational structures, and as increasingly specialized instruction-silicon pairings are intro-

MI, USA. ACM, New York, NY, USA, 8 pages. https://doi.org/10.1145/3458336.3465297

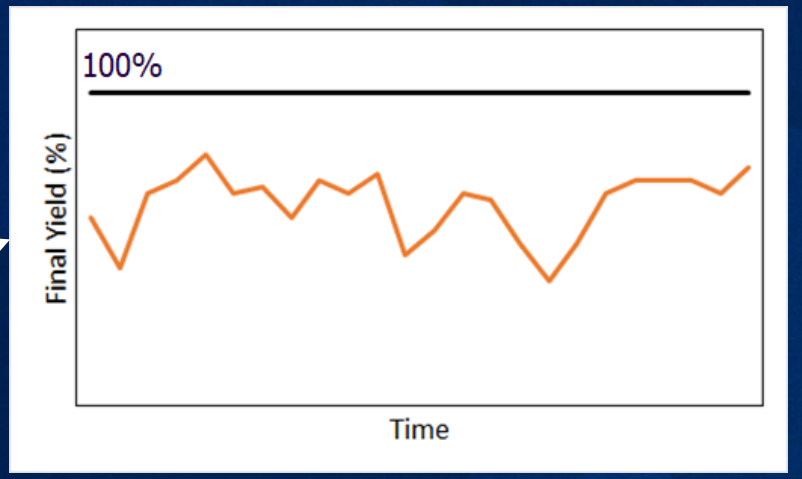
1 Introduction

Imagine you are running a massive-scale data-analysis pipeline in production, and one day it starts to give you wrong answers – somewhere in the pipeline, a class of computations are yielding corrupt results. Investigation fingers a surprising cause: an innocuous change to a low-level library. The change itself was

Even package level test has challenges catching all defects due to differences in the test vs use environment

cKGD

Typical final yield for a 3DIC



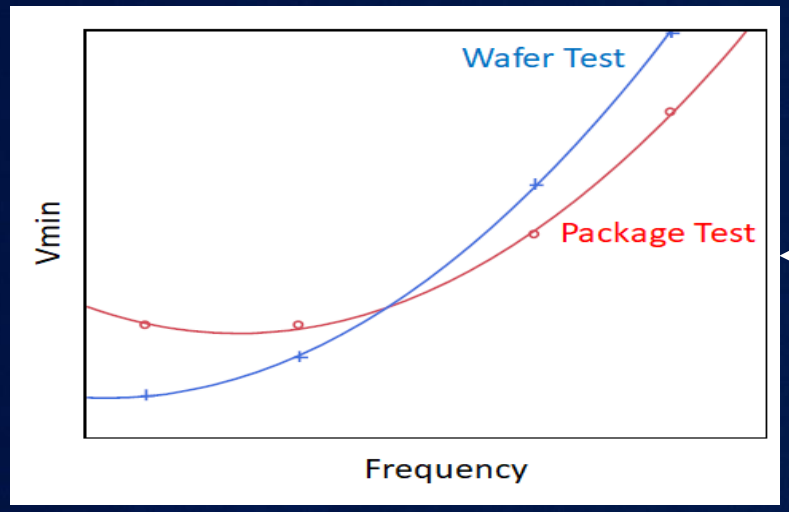
Despite best efforts to produce KGD out of wafer test, there are still a significant number of defects that are being caught at package test

Defects are getting harder to catch and test methods and strategies are not keeping pace

cKGD Challenges

Typical final yield for a 3DIC

	Wafer Test	Package Test
Thermal	Cold/warm, passive cooling	Hot, active cooling
Electrical	No package, limited connectivity	Package, full connectivity
Mechanical	No package, flat die	Package, warped die

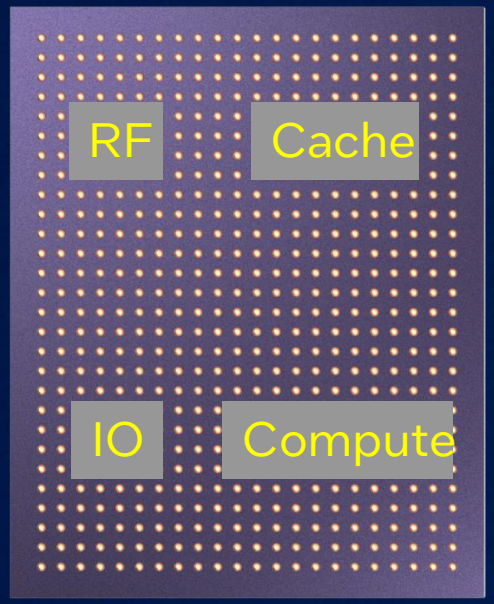


Device performance shifts due to differences in the wafer test vs backend test environment

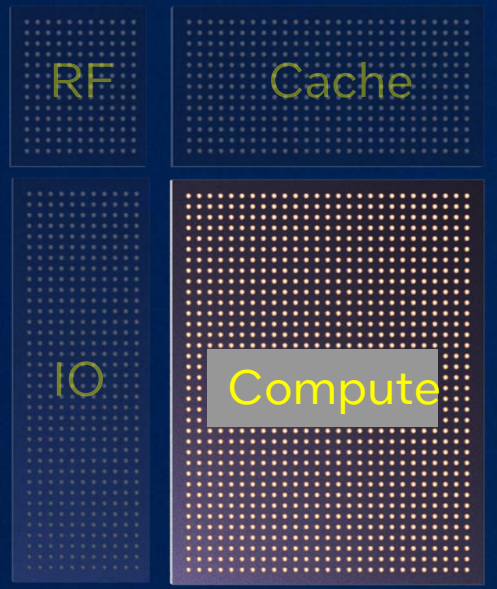
cKGD

Differences in wafer test vs backend test environment present challenges in properly characterizing chiplets

Characterization Challenges



All functional blocks are present during wafer test



Functional blocks are distributed and not present during wafer test

Need methods for effective testing and characterization of disaggregated chiplets that don't have all the functional blocks available during wafer test

Executive Summary

- Industry is trending towards more complex integration schemes to address cost and scalability challenges
- The era of 3D integration and advanced packaging is upon us, but the ecosystem is not ready
  - There are fundamental design, manufacturing, and enabling challenges that must be addressed
- Metrology, physical debug, and manufacturing test are underserved and need more focus and investment from industry and academic partners
  - “if you can’t test it, you don’t have a product”