Advanced Package Evaluation Platform through Collaboration

Hidenori Abe
Executive Officer, Electronics Business Headquarters
Resonac Corporation

Mar. 20, 2024

Today’s Presentation

RESONAC

1. Japan's Semiconductor Industrial Policy and Strategy
2. Corporate Introduction
3. Packaging Solution Center & Co-Creative R&D Platform and JOINT2 R&D Status
4. Overseas Strategy of Semiconductor Business
5. Carbon Neutrality and Supply Chain Management

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Global Government Funding to Semiconductor

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EU **$46Bn**
EU CHIPs Act
Global market share to double 20% by 2030
Intel, STM, Bosch…

Korea
K-semiconductor belt strategy
Samsung, SK Hynix…

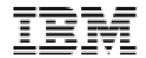
US **$50Bn**
CHIPs and Science Act
Intel, Micron, TSMC, Samsung…

China
Fund and Tax incentive
Global market share to 70% of domestic chip using rate by 2025
≥$74Bn

India
India Semiconductor Mission
Up to 50% co-funding

Japan

$27Bn ('21-23)
The investment of Japanese government

2nm Logic Manufacturing technology
Rapidus
Joint development partnership


KIOXIA
NAND Memory

DRAM Memory

Opening in February 2024

Logic

Substrate

Front-end process technology Platform

Cutting-edge Machine

Annealing
Cleaning

Nanoimprint

GAA-FET Common Pilot Line

EUB resist

from Japan's METI website
https://www.meti.go.jp/english/index.html

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Japan’s Strategy for the Semiconductor Industry

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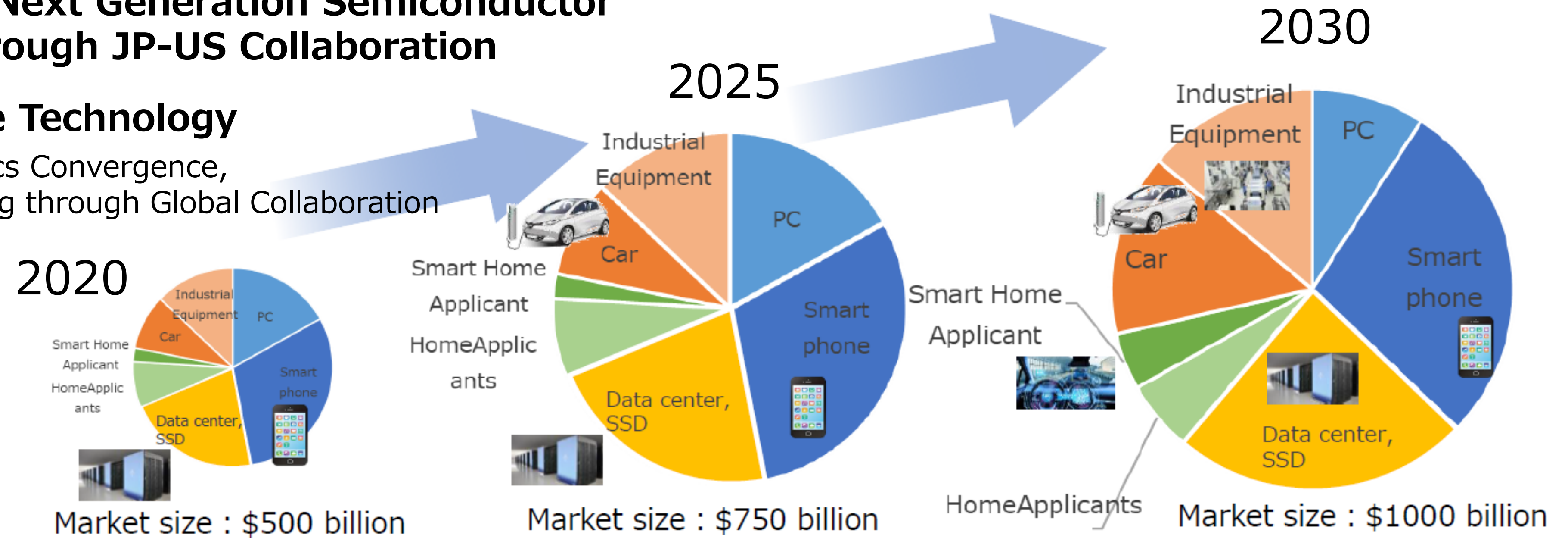
Step 1: Enhancement of Basic Production Capacity for IoT

Step 2: Realization of Next Generation Semiconductor Technology through JP-US Collaboration

Step 3: R&D for Future Technology

Photonics-Electronics Convergence,
Quantum Computing through Global Collaboration



Advanced semiconductor Strengthen their manufacturing bases	**Logic, DRAM, NAND** → TSMC/JASM, KIOXIA, MICRON
Economic Security Promotion Ensuring a stable supply of Key products	**MCU, Power IC, Analog IC, Si wafer, Substrate, SiC wafer** → RENESAS, IBIDEN, SHINKO, CANON, SUMCO, RESONAC, Sumitomo ···
Post-5G technology R&D and Manufacturing technology	**Beyond 2nm Logic, System design, Front-end process ...** → Rapidus, LSTC, TEL, SCREEN, CANON, JSR, NTT, Softbank ···

from Japan’s METI website

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Project Framework for Beyond 2nm Project in Japan

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Mass Production "Rapidus"

- Mass Production Design Function
- Mass Production Line@Rapidus
- Equipment/ materials

R&D Requirement

Commercialization

Open R&D "LSTC"

- R&D for Design Tech
- Pilot Line @Rapidus
- R&D for Equips/ Materials

LSTC: The Leading-edge Semiconductor Technology Center
Additional investment decided in February 2024

■ Oversea Collaboration

- Research Labs &Academia in Like-minded Countries : US NSTC, IBM, IMEC, etc

■ Domestic Collaboration

- Semicon User Companies
- Digital Design Labs
- Material & Machinery Companies

etc

JP Private Companies
Kioxia, Sony, SoftBank, Denso, Toyota, NEC, NTT, MUFG

JP Academia
JP National Research Rab

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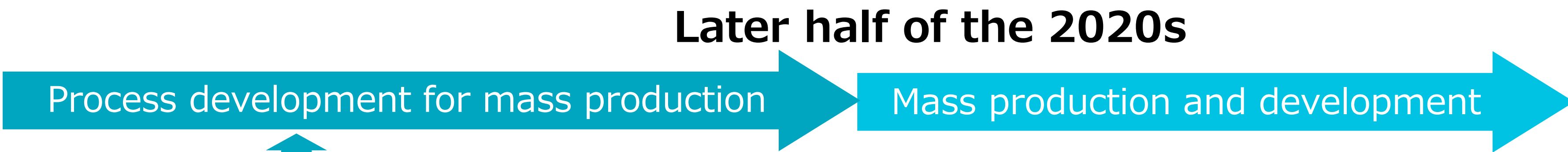
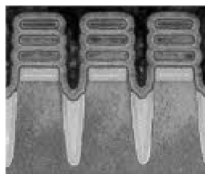


Gate All Around Nanosheet technology



Source: IBM website

EUV lithography equipment

Source: ASML website

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from Japan's METI website
https://www.meti.go.jp/english/index.html

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Subsidy for Back-end Process technology

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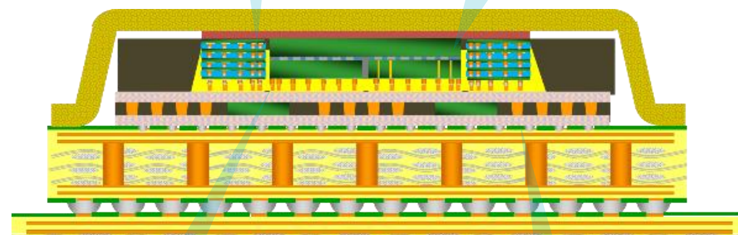
The investment includes not only Front-end process, but also **Back-end process technology** for next generation 2.xD/3D-PKG

Post-5G Technology

Technology development example

3D assemble (Memory on Logic)

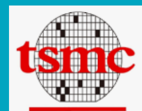
Chiplet technology



High density assemble

Low cost·High performance

Cutting-edge packaging technology



Supplier Materials Machine

3DIC Technology Research and Development

Direct bonding 3D-stack

Narrow pitch bonding

Hybrid bonding

Low temp. connection

CoW Direct bonding

Substrate

Fine pattern
High density

Materials

Materials evaluation platform

Fine bump
Fine pattern
Large flat substrate

EMC
Photo-materials
Resin for antenna

Assembly

Laser transfer

High performance large area 3.xD chiplet technology research and development

Selected on Dec. 2023

R&D subsidy selected theme related to Back-end Process in Japan

from Japan's METI website
https://www.meti.go.jp/english/index.html

METI Ministry of Economy, Trade and Industry

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January 2023: Resonac was born

Showa Denko

Showa Denko Materials
(Former Hitachi Chemical)

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Chemistry for Change

Resonate
共鳴する・響き渡る

Chemistryの「C」

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Company Consolidated Net Sales

Other 10%

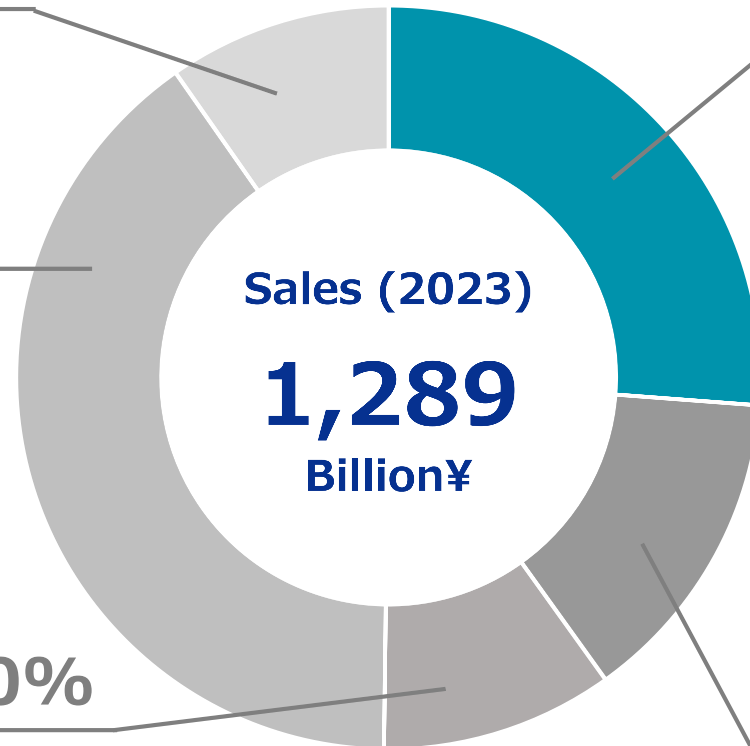
・Life science

Chemicals 40%

・Olefins and Derivatives
・Basic chemicals and Industrial gases
・Graphite electrodes

Innovation Enabling Materials 10%

・Functional chemicals
・Coating materials
・Ceramics
・Aluminium specialty components



Semiconductor and Electronic Materials 26% (338 Billion¥)

・High-purity gases and solvents
・CMP slurries
・Epoxy molding compounds
・Die bonding materials
・Copper clad laminate
・Photosensitive dry film
・Photosensitive solder resist
・Hard disc
・SiC epitaxial wafer
・Compound semiconductor

Mobility 14%

・Automobile products
・Lithium-ion battery materials

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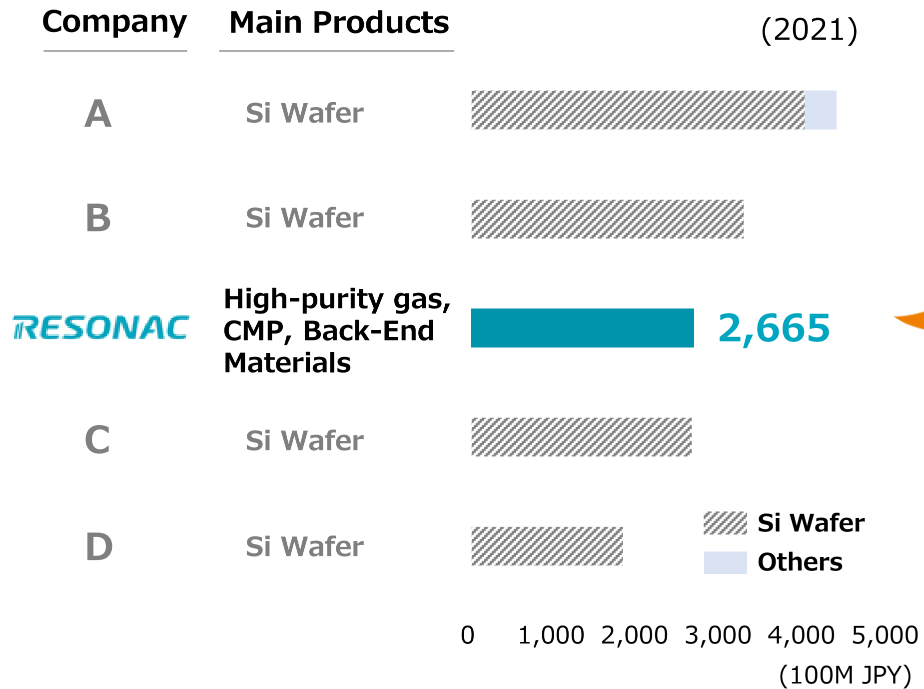
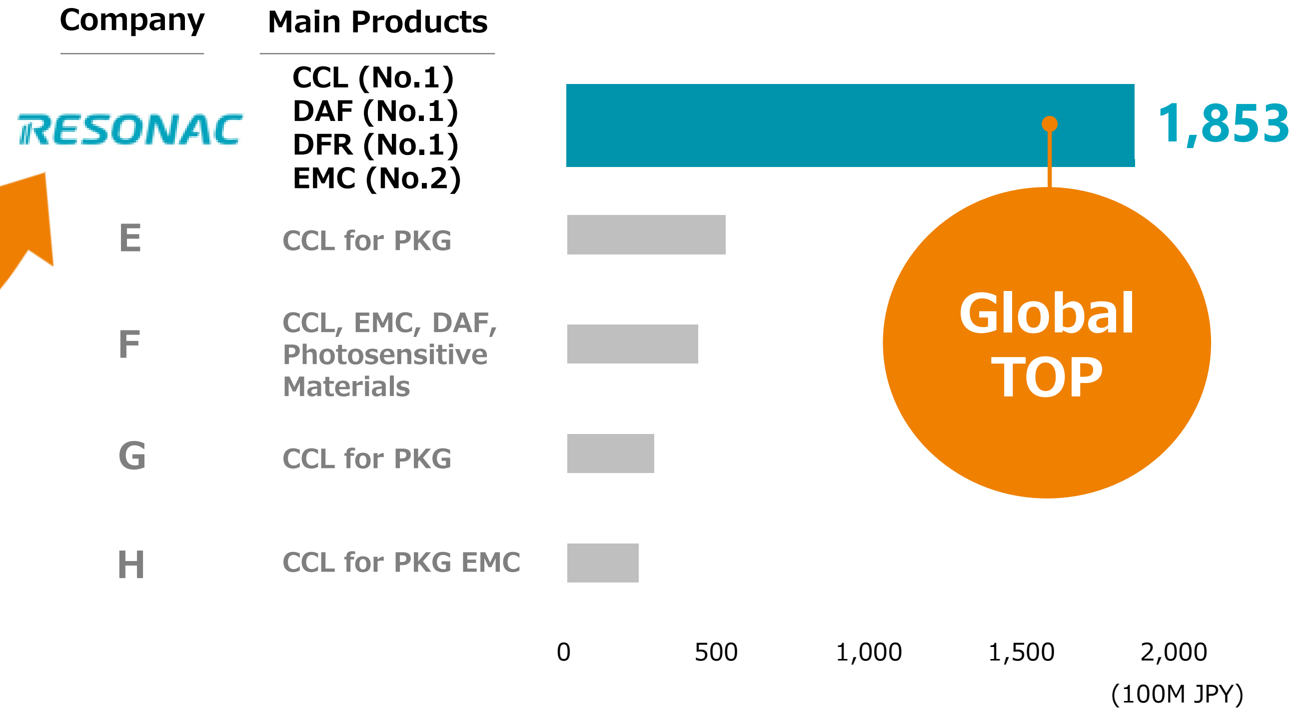
Top Company in Semiconductor Related Materials





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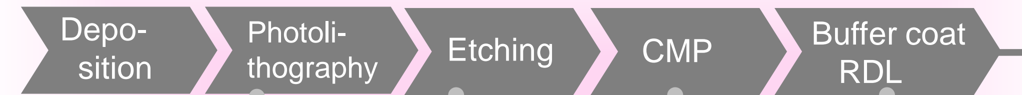
Resonac Materials Lineup for Semiconductor

Front-end Process

Wafer



High-purity Solvent

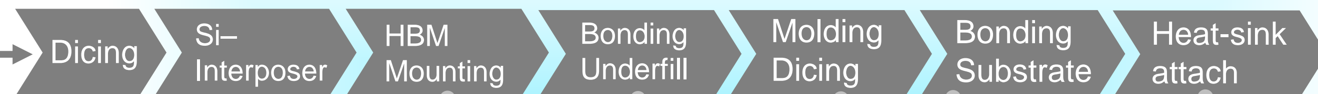
High-purity Gas
Global 1st
43%
for Etching

CMP Ceria Slurry
Global 1st
50%

PID
Global 1st
32%
*HDM

Back-end Process

Package



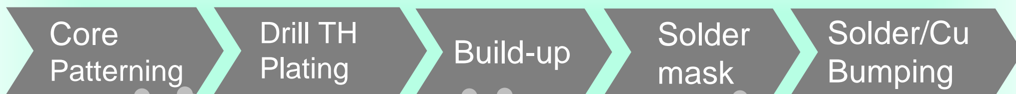
Die bonding film NCF
Global 1st
47%

CUF MUF
Global 2nd
19%

EMC
Global 2nd
19%

TIM
Sheet type
100%

Substrate manufacturing



Core material CCL
Global 1st
88% for PKG

Dry film resist
Global 1st
52%

Solder resist
Global 1st
85% for FC-BGA

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*1 Global market shares are based on data gathered by RESONAC
*2 HDM: HD Microsystems

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Technical Challenges for 2.xD/3D PKG

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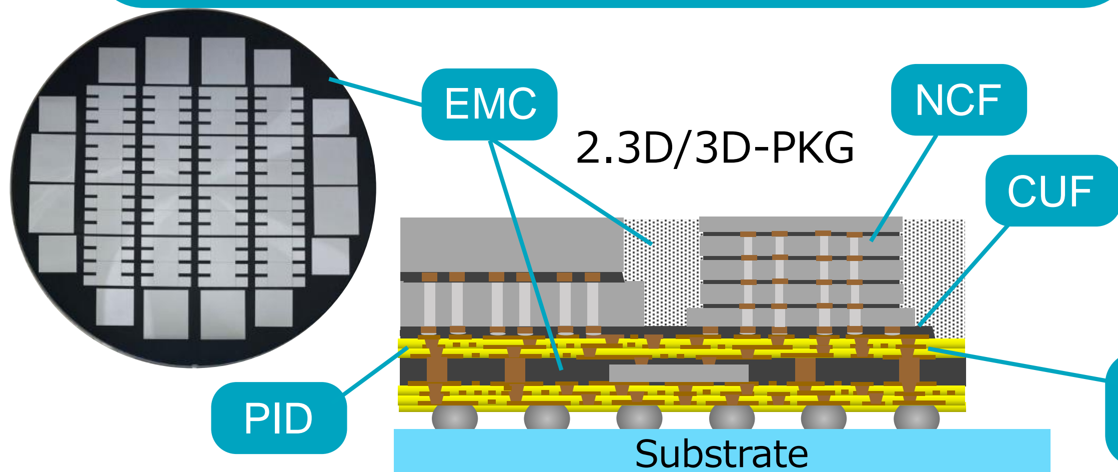
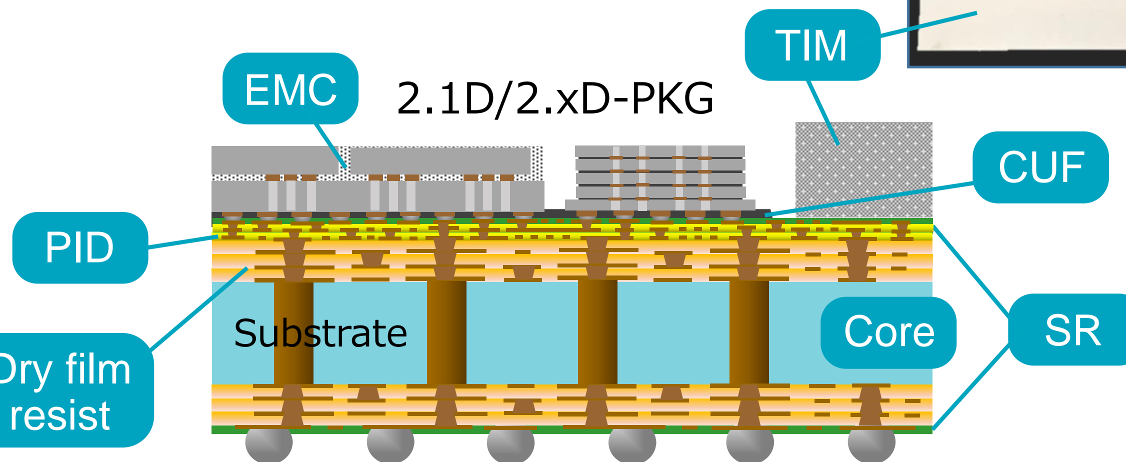
Assemble and Fine-pitch Bonding

- Micro solder/Cu bump formation
- Positioning accuracy
- Narrow gap filling / Bleed control and Voidless

Thermal solution

- High heat dissipation
- High thermal conductive materials

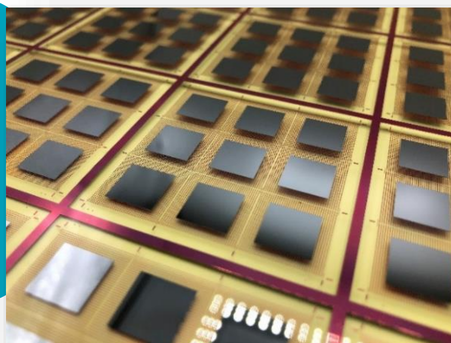




Continue to improve the performance of materials for the future PKG.

Organic interposer

- Fine RDL process
- Chip embedded molding
- Tall Cu pillar / Polishing EMC
- Low cost manufacturing (Panel level)



Fine-pitch Substrate

- Fine pattern formation (L/S≤2/2μm)
- Surface flatness (No undulation)
- No warpage
- Glass core technology

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New Materials Proposal for Back-end Process

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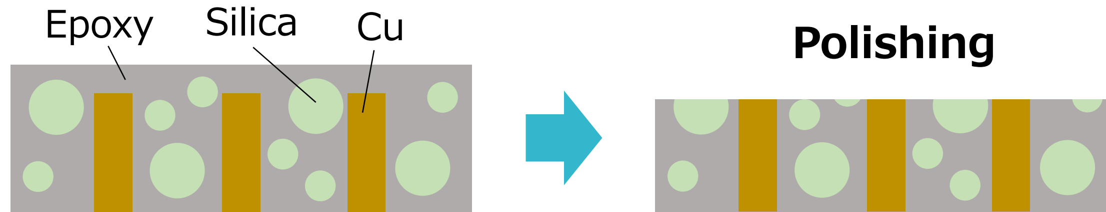
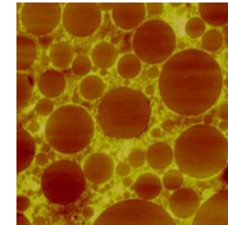
CMP for Polishing EMC and PID





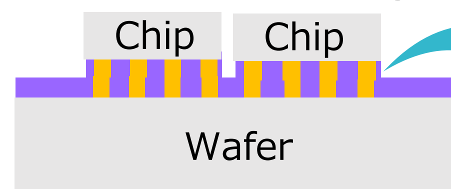
- ✓Cu/Silica/Epoxy selectivity
- ✓Filler drop prevention
- ✓Cu pillar topography
- ✓Anti Cu corrosion

2022 IEEE 72nd Electronic Components and Technology Conference (ECTC)

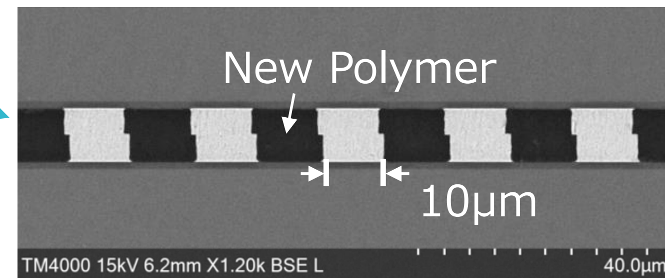
HS-8005
HS-CA315 series

New Polymer for Hybrid Bonding

Chip on Wafer

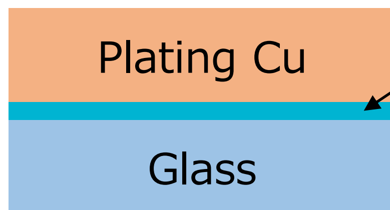


Low temp. pre-bonding (at 140°C)



LB-0100
LB-2000 series

Novel Primer for Glass Substrate



Primer

Peel strength
0.7 - 0.8 kN/m

"Cbla: Chemical Bonding Layer" improves adhesion between Cu and flat Glass without roughening process at low temp. and protects Glass.

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Why Co-Creation is so Important?

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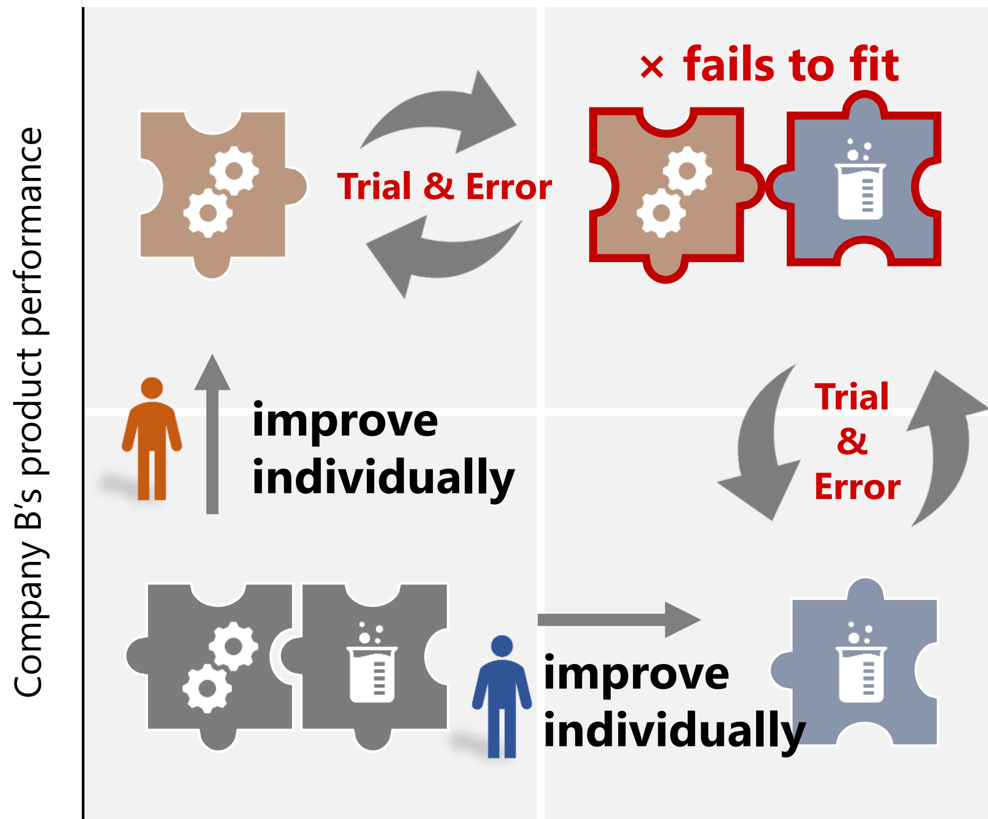
Individual approach



Partial optimization

Each company's limited information and capabilities require trial and error.

Co-Creation approach

Overall optimization

Improving together enables faster and better solution.

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Co-Creation in Advanced Packaging

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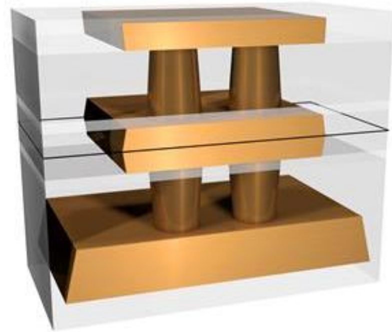
Examples of collaboration and integration in the Back-end equipment industry.

Hybrid Bonding Die to Die, Die to Wafer

2020



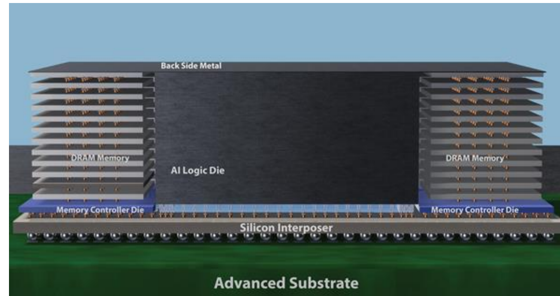
Etch, planarization, deposition, wafer cleaning, metrology, inspection, particle defect control

Die placement, interconnect, assembly solutions

https://ir.appliedmaterials.com/news-releases/news-release-details/applied-materials-and-be-semiconductor-industries-accelerate

Hybrid Bonding Wafer to Wafer

2021



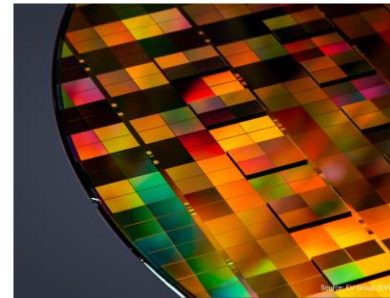
Deposition, planarization, implant, metrology, inspection

Wafer bonding, wafer pre-treatment and activation, alignment and bond overlay metrology

https://ir.appliedmaterials.com/news-releases/news-release-details/applied-materials-introduces-new-technologies-and-capabilities

Hybrid Bonding Die to Wafer

2021



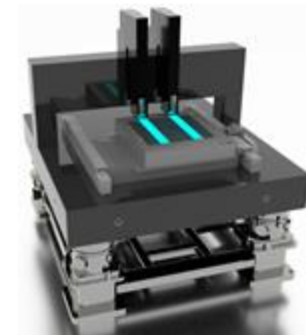
Die preparation (cleaning and activation) and wafer bonding capabilities

Precision die-bonding capabilities

https://www.evgroup.com/ja/company/news/detail/asm-pacific-technology-and-ev-group-join-forces-to-enable-industrys-first-ultra-precision-die-to-wafer-hybrid-bonding-solutions-for-3d-ic-heterogeneous-integration

Digital Lithography Technology Large panel

2023



Large panel processing

Lithography for packaging

https://ir.appliedmaterials.com/news-releases/news-release-details/breakthrough-digital-lithography-technology-applied-materials

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Effect of External Collaboration

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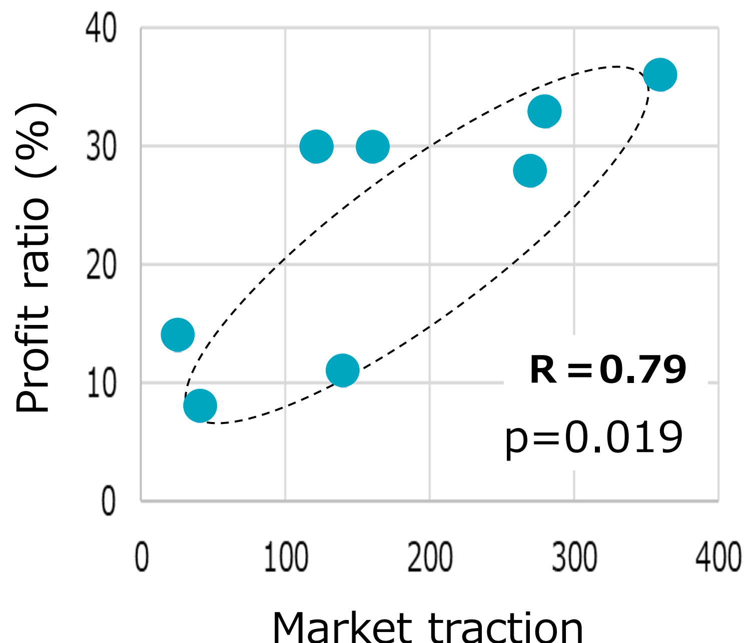
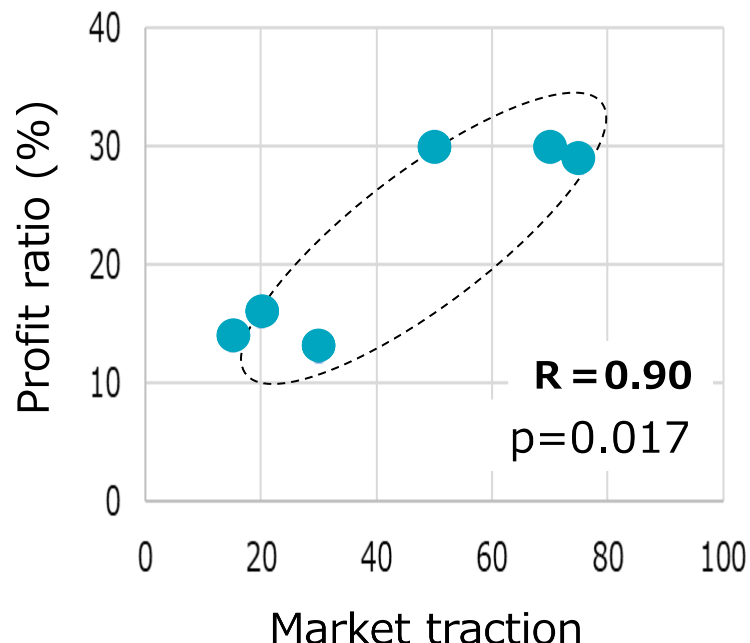
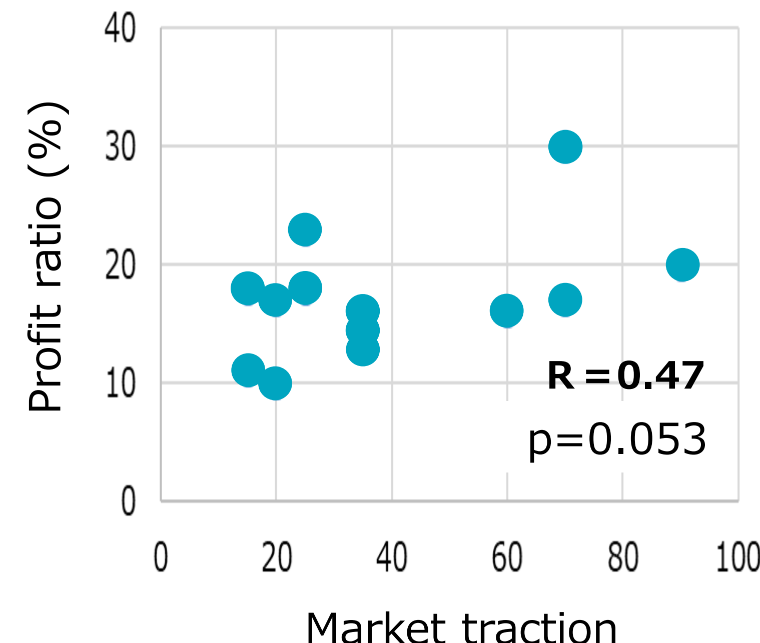
Front-end Process Equipment



Back-end Process Equipment



Back-end Process Materials & Substrates



Market traction＝“**Highest product share**”×“**The number of external collaboration**”

The correlation is weak for “Back-end Process Materials & Substrates” because of lower collaboration, suggesting the need for mergers, alliances and/or external collaboration.

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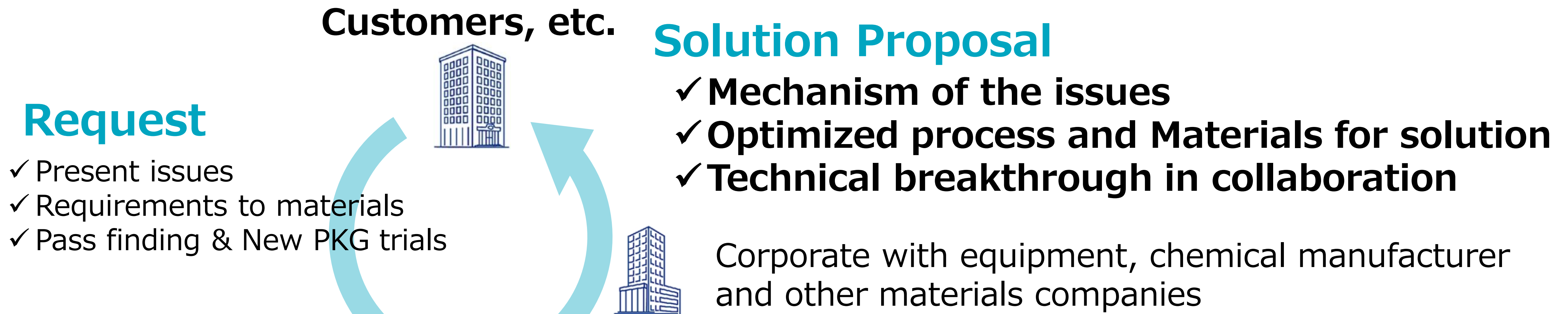
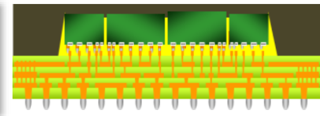
Packaging Solution Center (PSC)

Co-Creation site with customers and other companies to overcome various technical issues

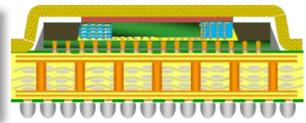


Located in Kawasaki-city, Kanagawa-pref. Japan

JOINT1 (2018-)
: FO-WLP & PLP



JOINT2 (2021-)
: 2.xD & 3D



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Function & Target of PSC

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TV Design

Modeling Simulation

Cu
L/S 2 µm
CUF
EMC
Chip
CUF
Area 2
Area 1
Area 3
Chip
Chip

TV Design/Modeling

Simulation

Substrate RDL Wiring

Assembly Packaging

L1: L/S = 2/2 µm
Wiring
Assembly
Flip chip bonder

Reliability Evaluation

Material Property

Thermal cycle test

Failure analysis

Evaluation results of Warpage

at 25℃
at 260℃

Ave. 215µm (Cry direction)
Ave. 81µm (Smile direction)

Simulation results of Warpage

at 25℃
at 260℃

221µm (Cry direction)
77µm (Smile direction)

2.xD/3D

FO-WLP/PLP

Memory
Logic
Logic
Memory

Memory

AiP/ RFFE

Transmission line simulation

Compatible with various types of PKG

3rd Floor Layout of PSC

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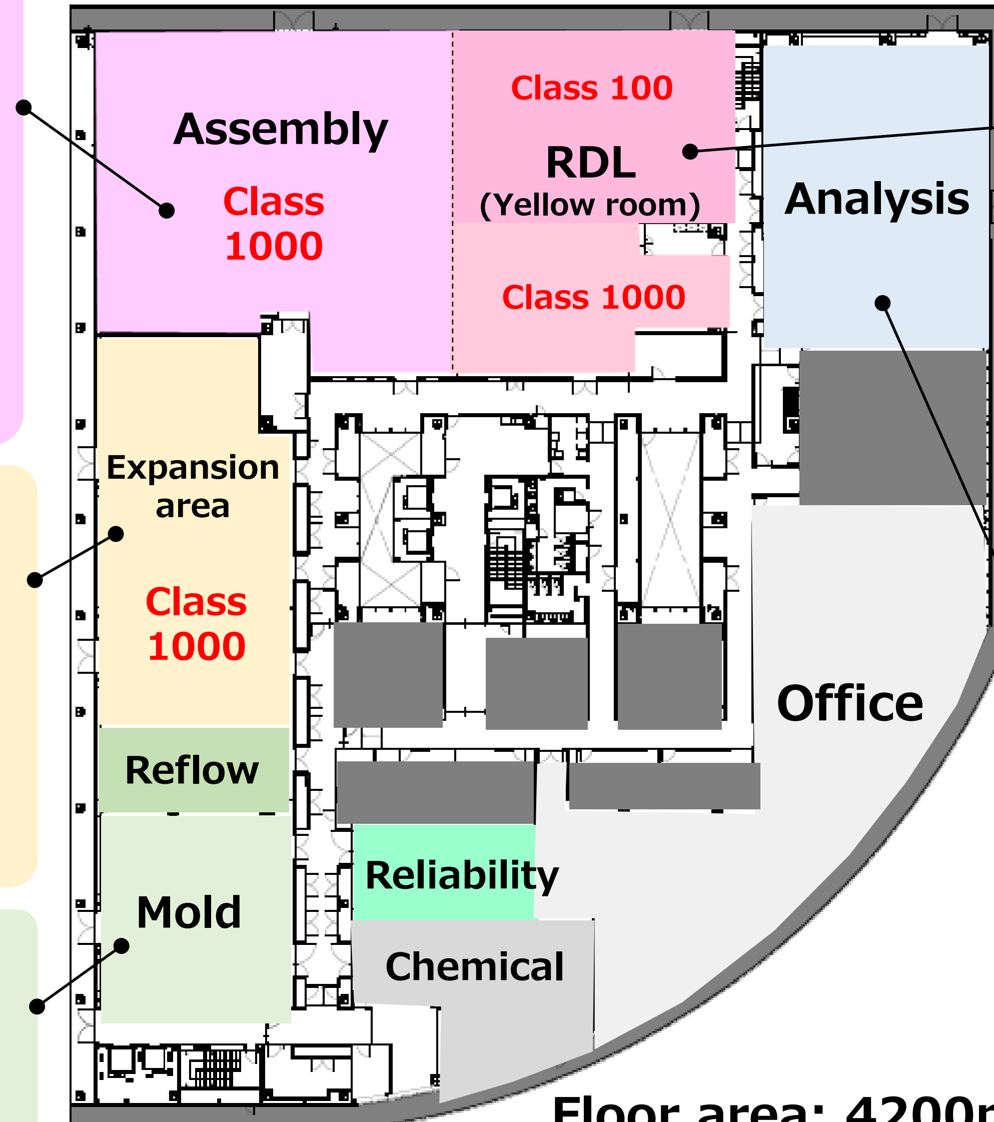
Assembly area
- ✓ Grinder
- ✓ Blade & Laser Dicer
- ✓ Die bonder
- ✓ CoC, CoW flip chip bonder
- ✓ Large die mounter
- ✓ Jet dispenser
- ✓ X-ray CT
- ✓ AOI

Expansion area
- ✓ C2W bonder
- ✓ Panel CMP
- ✓ Temporary bonder & debonder
- ✓ Compression molding
- ✓ Panel Grinder
- ✓ Panel Surface planer

Mold area
- ✓ Substrate Transfer
- ✓ Substrate Comp.
- ✓ Wafer Comp.
- ✓ Panel Comp.



Floor area: 4200m²
Clean room: 1450m²

RDL area
- ✓ Spin coater
- ✓ Slit coater
- ✓ Vacuum Dryer
- ✓ Stepper
- ✓ LDI exposure
- ✓ Developer
- ✓ Sputtering
- ✓ Plasma asher
- ✓ Vacuum Laminator
- ✓ Cu Plating

Analysis area
- ✓ FE-SEM-EDX
- ✓ FIB
- ✓ SAT
- ✓ 3D measurement
- ✓ Shadow moiré / DIC
- ✓ Probe tester
- ✓ Laser decapsulator
- ✓ Network analyzer
- ✓ AFM

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Be a Leader in Semiconductor Technology Innovation

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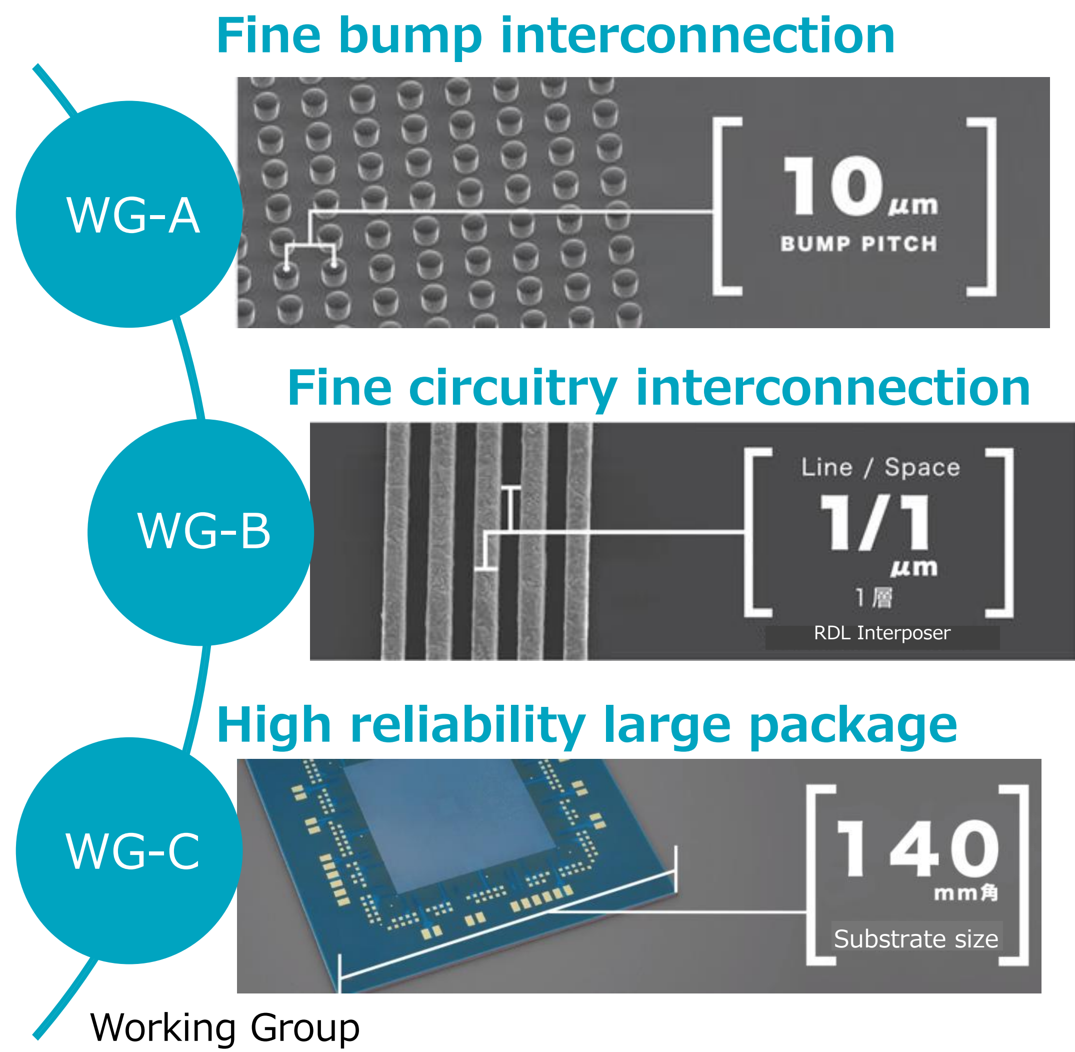
“Open innovation platform” evolve to “Consortiums with multiple company”

JOINT2 ADVANCED PACKAGE EVALUATION PLATFORM

RESONAC
AIMECHATEC
YAMAHA
YAMAHA ROBOTICS HOLDINGS CO., LTD.
Eat Well, Live Well.
AJINOMOTO
UYEMURA
tok
DNP
DISCO
JOINT2
SHINKO
Panasonic CONNECT
EBARA
MEC
NAMICS
ORC

Multiple working groups × Mutual utilization of technology and information



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WG-A. Fine Bump Interconnection

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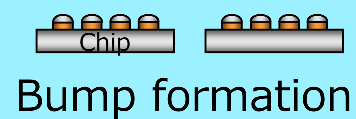
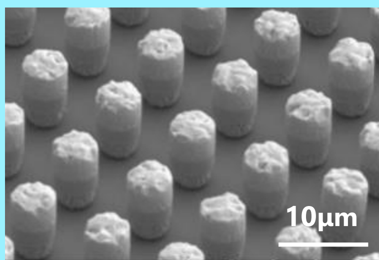
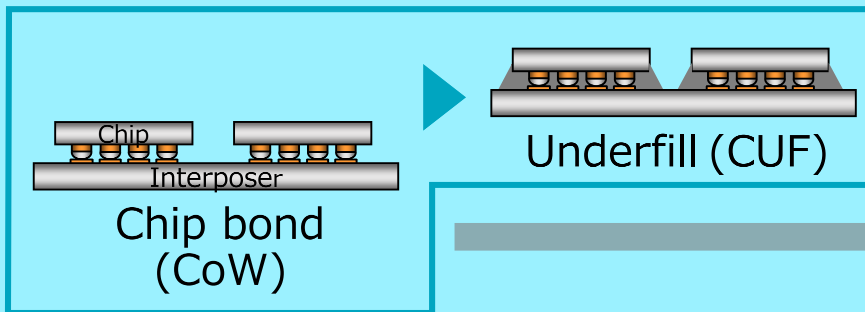
CoW Process

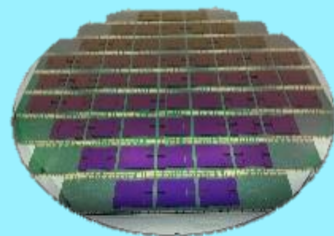


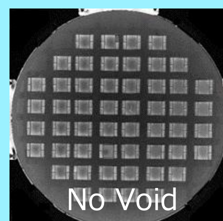
Bump formation



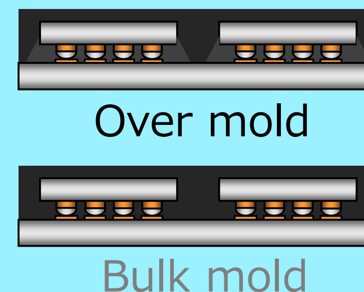
Cu Bump Φ5µm



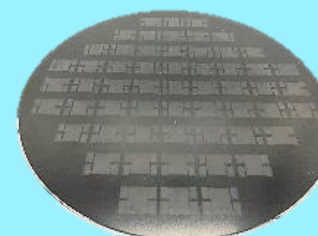


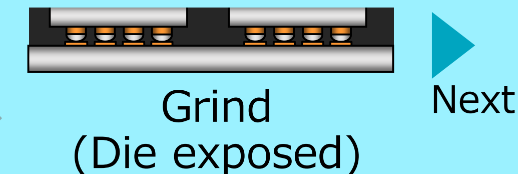


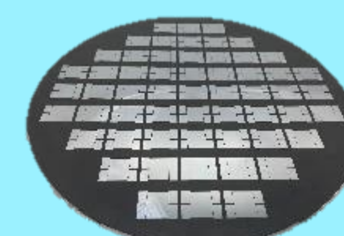
SAT image



Bulk mold

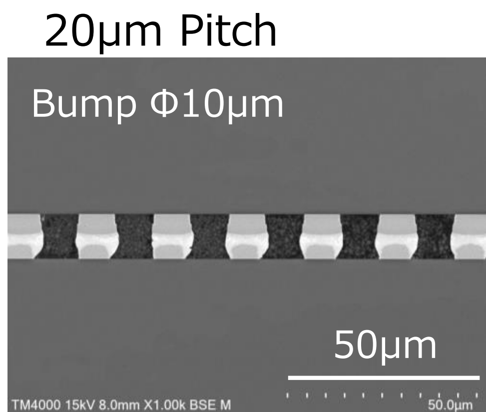




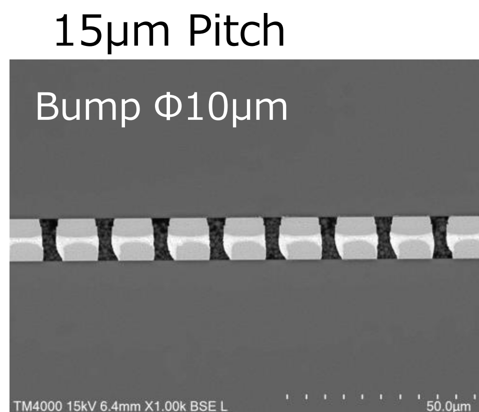


Excellent underfillability in narrow pitch and gap

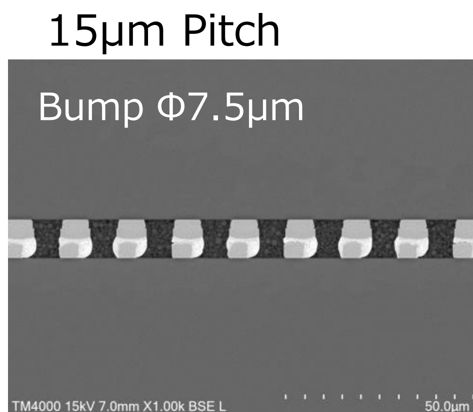
20µm Pitch



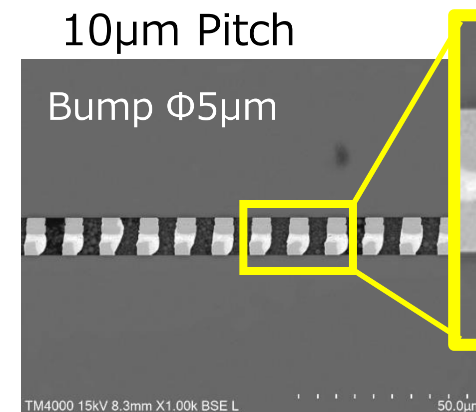
15µm Pitch

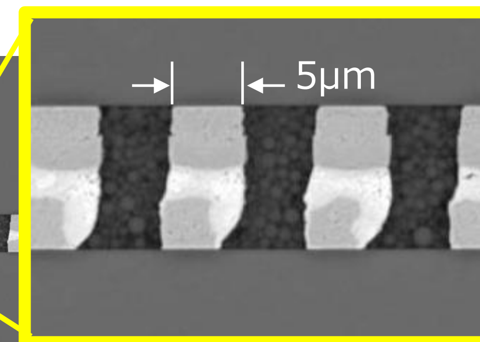


15µm Pitch



10µm Pitch





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WG-B. Fine Circuitry Interconnection

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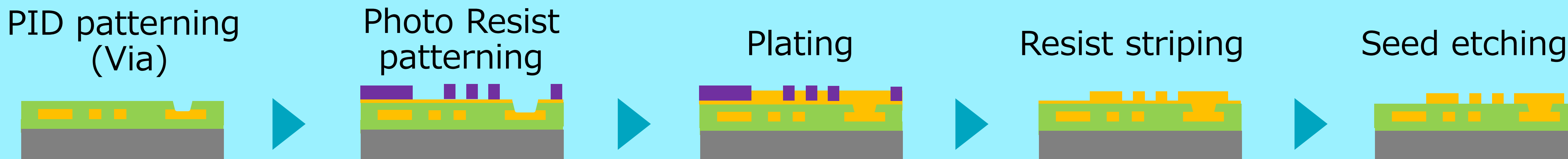
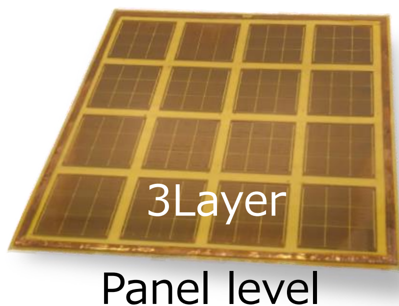
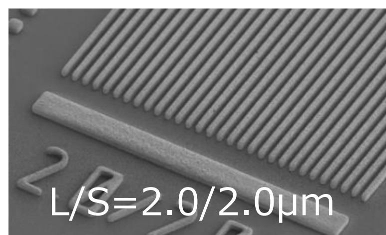
Semi-Additive Process (SAP)

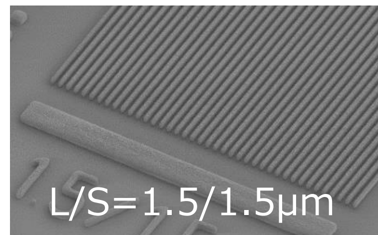


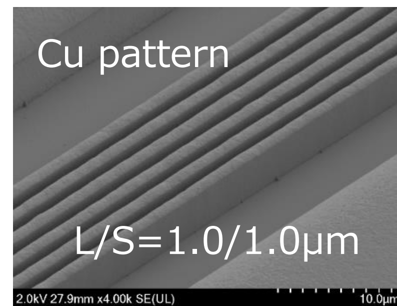


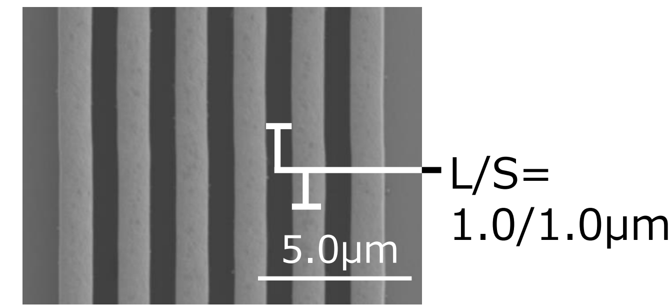
Panel level

Dry film resist (Photec RY-series)

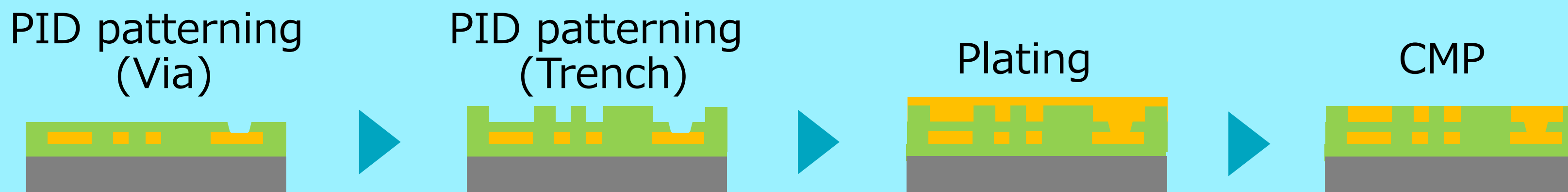








Damascene



L/S	1.6/1.6μm	1.3/1.3μm	1.0/1.0μm	0.8/0.8μm
PID pattern				
TCD	2.06μm	1.86μm	1.62μm	1.56μm
BCD	1.53μm	1.25μm	0.94μm	0.76μm

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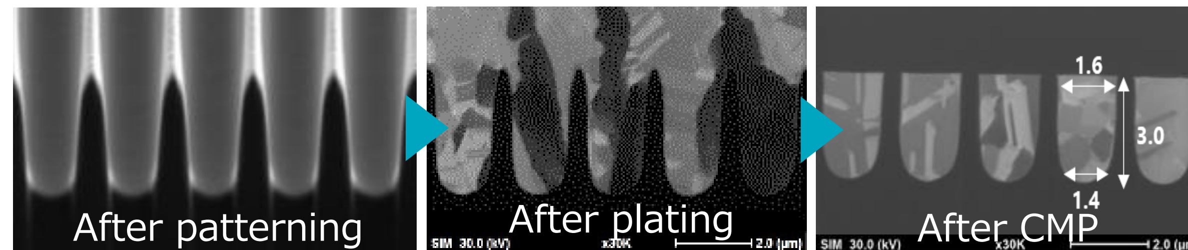
Plating → CMP (L/S=1.0/1.0μm)



PID for Damascene (Posi-type AR-series)

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WG-C. High Reliability Large Package

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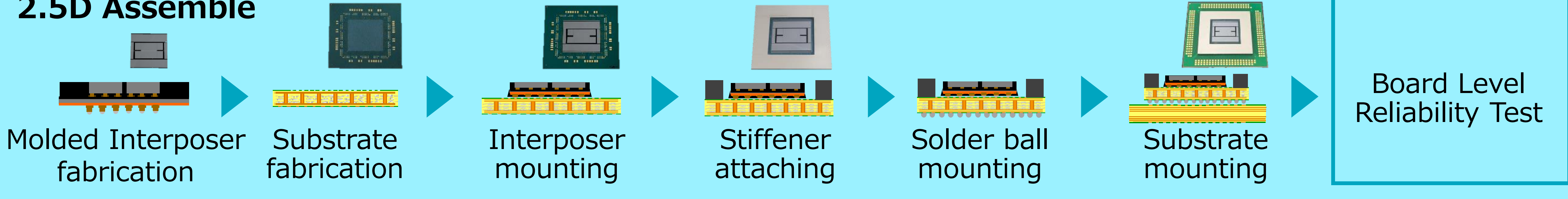
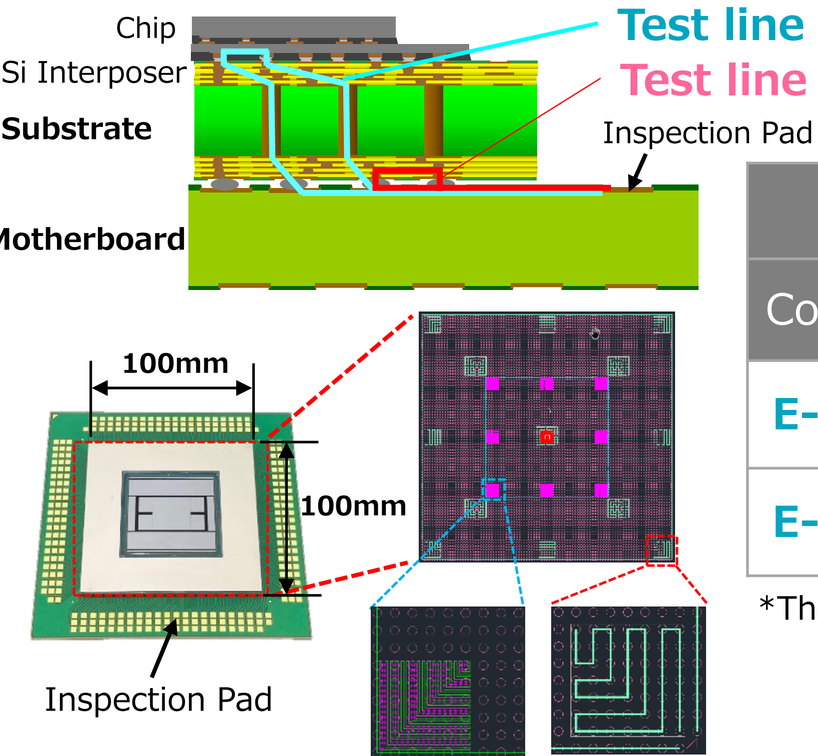


100x100mm PKG size Board Level Reliability (Thermal cycle test -55↔125℃)

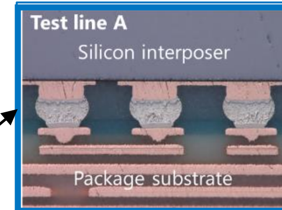


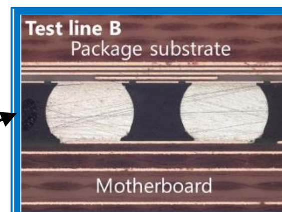
Test line A : Interposer – Substrate – Motherboard

Test line B : Substrate – Motherboard

Substrate		Motherboard		Result* 1000cyc		Result 2000cyc
Core material	CTE1 [ppm/℃]	Core material	CTE1 [ppm/℃]	Test line A	Test line B	
E-705G(LH)	6.9	E-705G(LH)	6.9	Pass	Pass	Pass
E-705G(LH)	6.9	Conventional	15.0	Pass	Pass	Fail

*The criteria was set at resistance change of 20% or less.





120x120mm and 140x140mm PKG size are ongoing.

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Today’s Presentation

RESONAC

1. Japan's Semiconductor Industrial Policy and Strategy
2. Corporate Introduction
3. Packaging Solution Center & Co-Creative R&D Platform and JOINT2 R&D Status
4. Overseas Strategy of Semiconductor Business
5. Carbon Neutrality and Supply Chain Management

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R&D Center in Silicon Valley, USA

RESONAC

Plans to establish a back-end R&D center in Silicon Valley, USA,
where GAFAM and semiconductor manufacturers are concentrated.

Start of preparation including consideration and investigation of equipment to be introduced.

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R&D Center in Silicon Valley, USA

RESONAC

Purpose

- ✓ **Co-Creation and concept validation** with concept leaders of advanced packaging, and materials and equipment manufacturers.
- ✓ **Development of human resources** that can **compete on the world stage**.

Plan

Year 2023

Planning, coordination and preparation

Install clean room and equipment.
Start test operation.

Year 2025

Full-scale operations begins.

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Our Challenge to Achieve Carbon Neutrality

Resonac sets 2030 target as **30% reduction of GHG emission** below 2013 levels & 2050 goal of Carbon neutrality.

Discussions with the industry

Semiconductor Climate Consortium
FOUNDING MEMBER

SEMI ANNOUNCES SEMICONDUCTOR CLIMATE CONSORTIUM FOUNDING MEMBERS

Source: November 1, 2022 SEMI announcement

Our Initiatives

- ✓ Reduction of CO_2 emissions at our own business sites
- ✓ **Study of low GWP gas solution** for semiconductor manufacturing process
- ✓ **Survey and proposal of contribution of CO_2 emissions** in semiconductor packaging process

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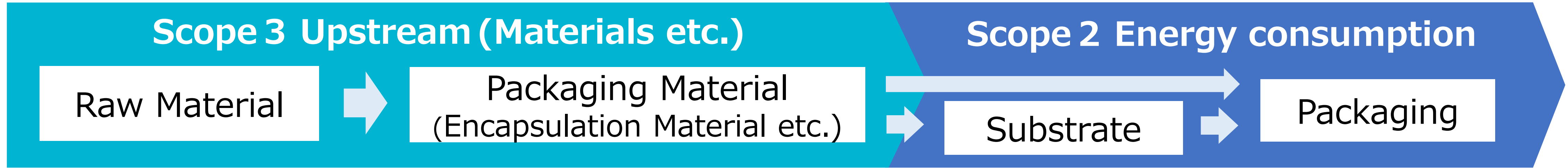
Estimation of GHG Emissions in Packaging Process



Total GHG emissions ($t\text{-}CO_2$/year)

2.5E+07
2.0E+07
1.5E+07
1.0E+07
5.0E+06
0.0E+00

■ Scope 2 Energy consumption
■ Scope 3 Upstream (Materials etc.)

Lead Frame (QFN) | BGA (WB/Memory etc. middle-small) | Lead Frame (SO) | Lead Frame (QFP) | FI-WLP | FC-CSP | BGA (FC/Logic etc. Large) | FO-WLP

Lower energy consumption (Scope 2) as an important means of reducing GHG emissions

Resonac is looking for partners to work on this topic together!

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SCM (Supply Chain Management) System

Resonac B site
Cloud
Supplier C
Supplier B
Supplier A
Coordination
FCST
Customer
Resonac A site

System Integration
- Sales
- Shipment Production
- Procurement

Digitization & Monitoring
- Customer data
- Order data
- CO2 emissions
- Product specification & Quality
- Product inventory
- Process conditions
- Worker labor conditions
- Raw materials ≒ tens of thousands
- Supplier data ≒ 500

Establishment of SCM System
✓ Early detection of supply chain risks due to market and social conditions
✓ Prompt response to customer needs and shorter lead times
✓ Disclosure of information on environmental impact
✓ Stable supply for products ; reduction of single supplier, alternative supplier research

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Summary

RESONAC

1. Resonac is Global No.1 semiconductor packaging material supplier.
2. Resonac offers advanced packaging materials through Packaging solution center evaluation.
3. Resonac has established JOINT2 with materials, substrate, and equipment companies, and currently considering to establish a new R&D center in Silicon Valley, USA.
4. Resonac is open to collaboration including 1on1 co-development with any partner.

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