

# Revitalizing Domestic Semiconductor Manufacturing: Challenges, Opportunities and Emerging Applications

Mark Litecky

SkyWater Technology



# Who is SkyWater Technology?



# We streamline the Concept-to-production journey.

Technology as a Service

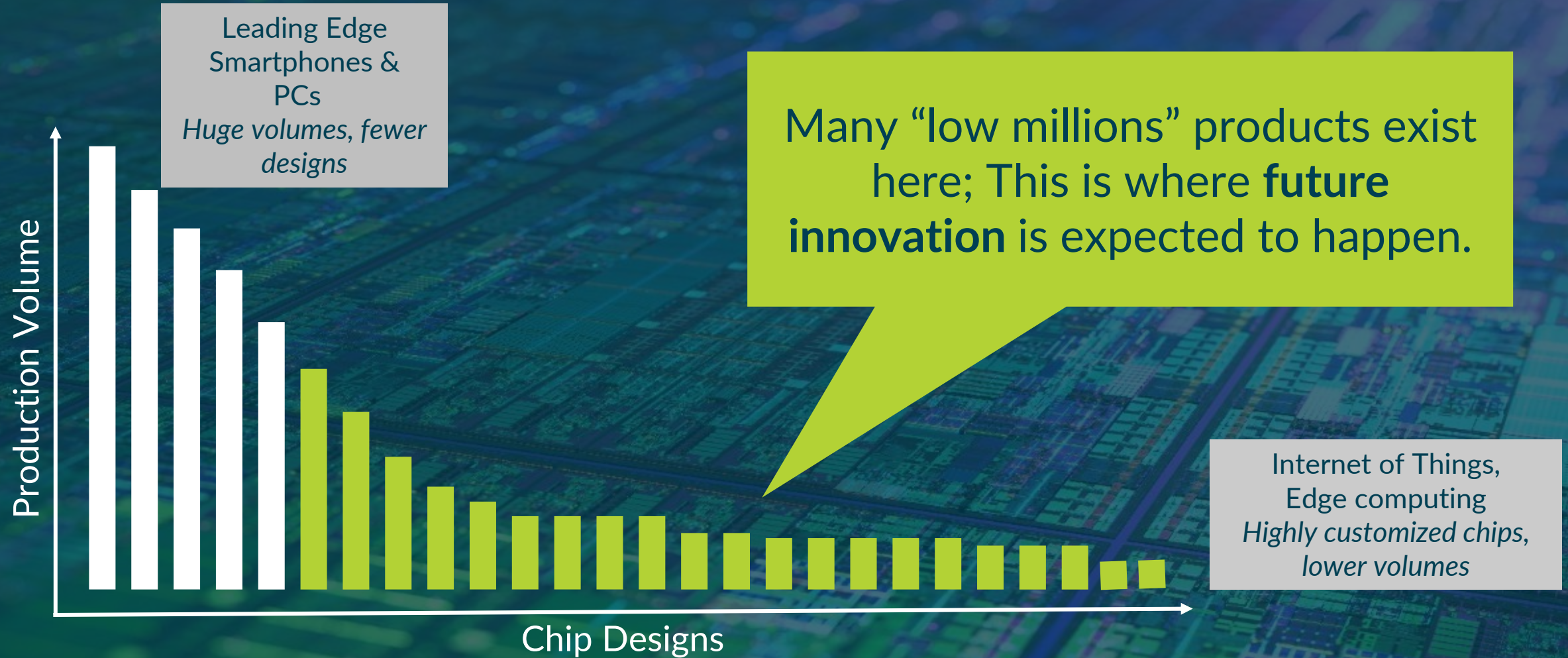
Innovation as a Service



Manufacturing as a Service



# Building the Future in the “Innovation Tail”



# America's Foundry At-a-Glance

**\$286M**

2023 Annual Revenue

**SKYT**

Traded on NASDAQ  
since 2021

**750**  
Total Employees



IATF16949

AS9100

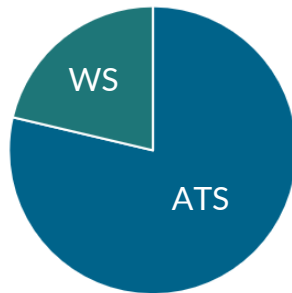
ISO9001

ISO4001

ISO13485

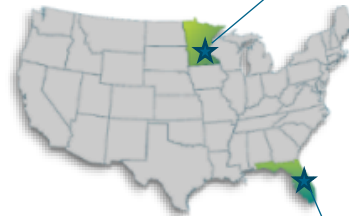
DMEA Cat 1A

Trusted



2023 Revenue by Service

Front-end Wafer Processing



Back-end Advanced Packaging



U.S.-based, investor-owned,  
pure-play foundry



# SkyWater Minnesota

Bloomington, MN



## OPERATION

- ~675 employees
- 200 mm equipment
- 91,000 ft<sup>2</sup> Cleanroom (Class 10 + SMIF)
- 10,000 30 ML CMOS wafers/month or 50,000 MOSFET wafers/month
- 65 nm+ feature geometries

## CERTIFICATIONS

- ISO9001 Quality Management System Certified
- ISO9100/IATF16949 Automotive Certified
- ISO13485 Medical Certified
- AS9100 Aviation, Space and Defense Certified
- ISO14001 Environmental Certified
- DMEA Cat 1A Trusted site since 2010
- ITAR and Secure Processing Supported



# SkyWater Florida

Kissimmee, FL

## OPERATION

- ~60 employees
- 200 mm equipment
- 35,400 ft<sup>2</sup> Cleanroom (class 1,000 & class 10,000)
- Site added to operation Feb 2021
- Facility will enable custom heterogeneous integration solutions
- Unique Public-Private Partnership (PPP)
  - Osceola County owns site/fab
  - SkyWater operates facility
  - Ecosystem partner with BRIDG (nonprofit)

## CERTIFICATIONS

- ISO9001 Quality Management System Certified
- DMEA Cat 1A Trusted – pending

# Trends Influencing the Semiconductor Industry



# Dynamics is Redefining Our Industry

New Product  
Development Costs  
are Skyrocketing

IP Security and  
Supply Chain Risks  
are Accelerating

Supply  
Chain Globalization  
to Improve  
Transparency

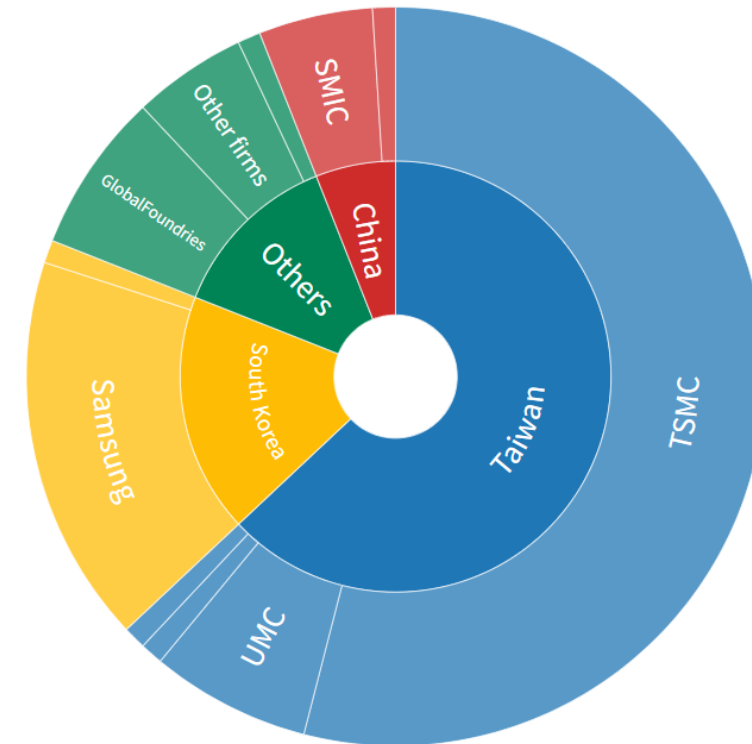
# A Need to Revitalize U.S. Manufacturing has Emerged

U.S. share of semiconductor manufacturing has eroded from 37% in 1990 to 12% today<sup>1</sup>

The U.S. share of global packaging capacity, including advanced packaging, is 3%<sup>2</sup>

## Semiconductor contract manufacturers by market share

Total foundry revenue stood at \$85.13 billion in 2020<sup>3</sup>



1. 2022 SIA Factbook: <https://www.semiconductors.org/the-2022-sia-factbook-your-source-for-semiconductor-industry-data/>

2. CSIS Advanced Packaging and the Future of Moore's Law: <https://www.csis.org/analysis/advanced-packaging-and-future-moores-law>

3. CNBC.com: <https://www.cnbc.com/2021/03/16/2-charts-show-how-much-the-world-depends-on-taiwan-for-semiconductors.html>

# We Need a High-Tech Workforce to be Successful

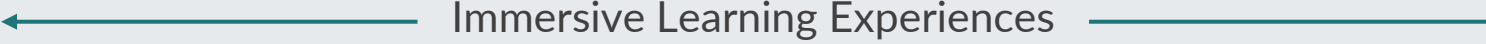
We need talent – 250,000 in the next 5+ years.

All semiconductor disciplines are needed, but also construction workers and workers in adjacent industries.

Nothing else matters!



# Dynamic Learning Supports Workforce Development

| Immersive Learning Approaches | Technicians                                                                              | Engineers                   | Business Functions          |
|-------------------------------|------------------------------------------------------------------------------------------|-----------------------------|-----------------------------|
| K-12                          |        |                             |                             |
| Post Secondary                | Scholarships<br>Apprenticeships<br>Re-education Programs<br>Veteran Workforce Transition | Scholarships<br>Internships | Scholarships<br>Internships |
| Graduate                      |                                                                                          | Rotational Programs         | Rotational Programs         |
| Post-Graduate                 |      |                             |                             |

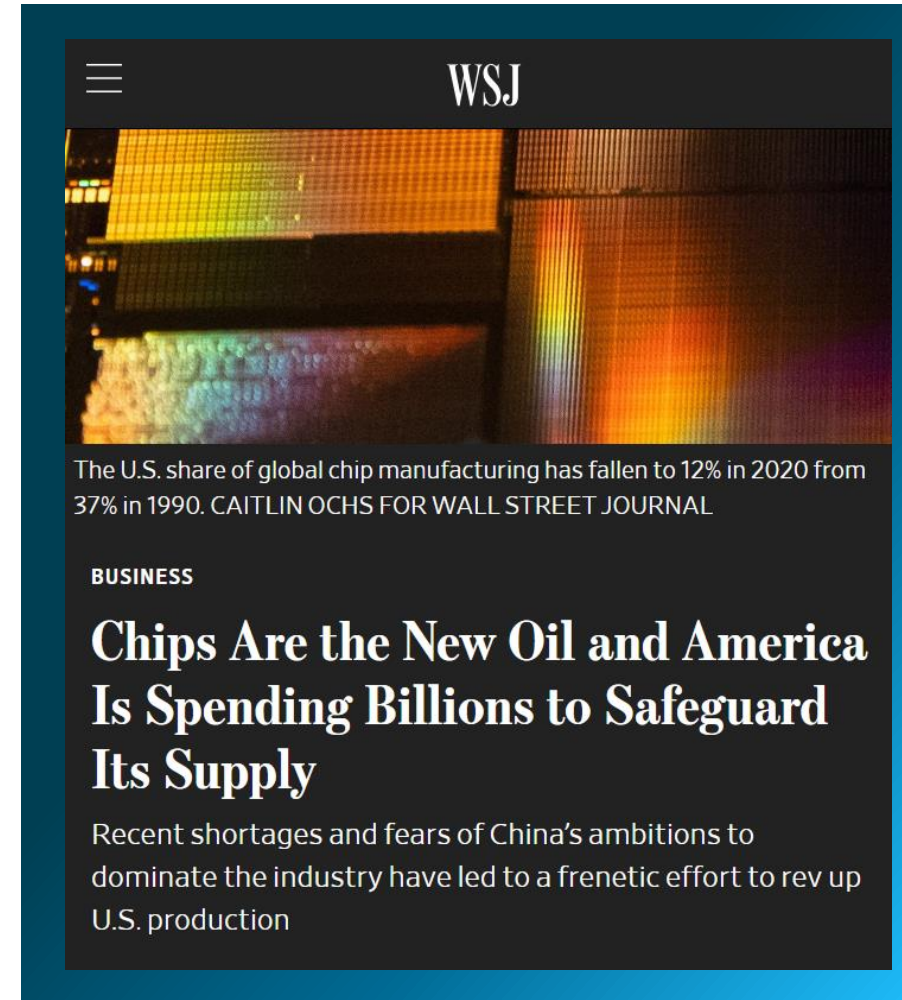
# Investments in Domestic Manufacturing



# Investment Needed for Both Leading Edge and Legacy Nodes

- 60% of microelectronics devices will be on 65 nm or higher platforms through 2030\*
- Investments are concentrated at the leading edge
- Mature nodes offer a base on which advanced emerging technologies can be layered
- Advanced Packaging is an opportunity to advance the leading edge of semiconductor technology

\*McKinsey Presentation at SEMI Industry Strategy Symposium, Jan 8-11, 2023, Half Moon Bay, CA

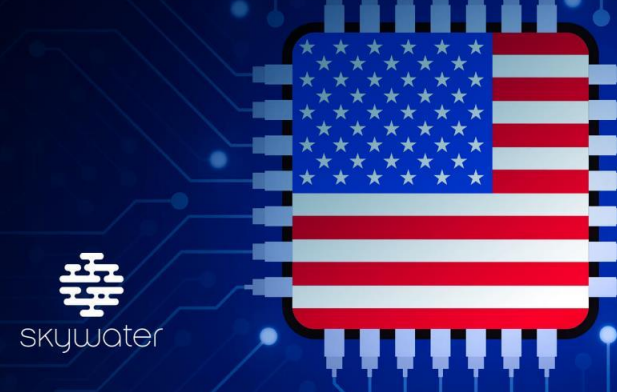


# President Biden Signs the CHIPS & Science Act of 2022



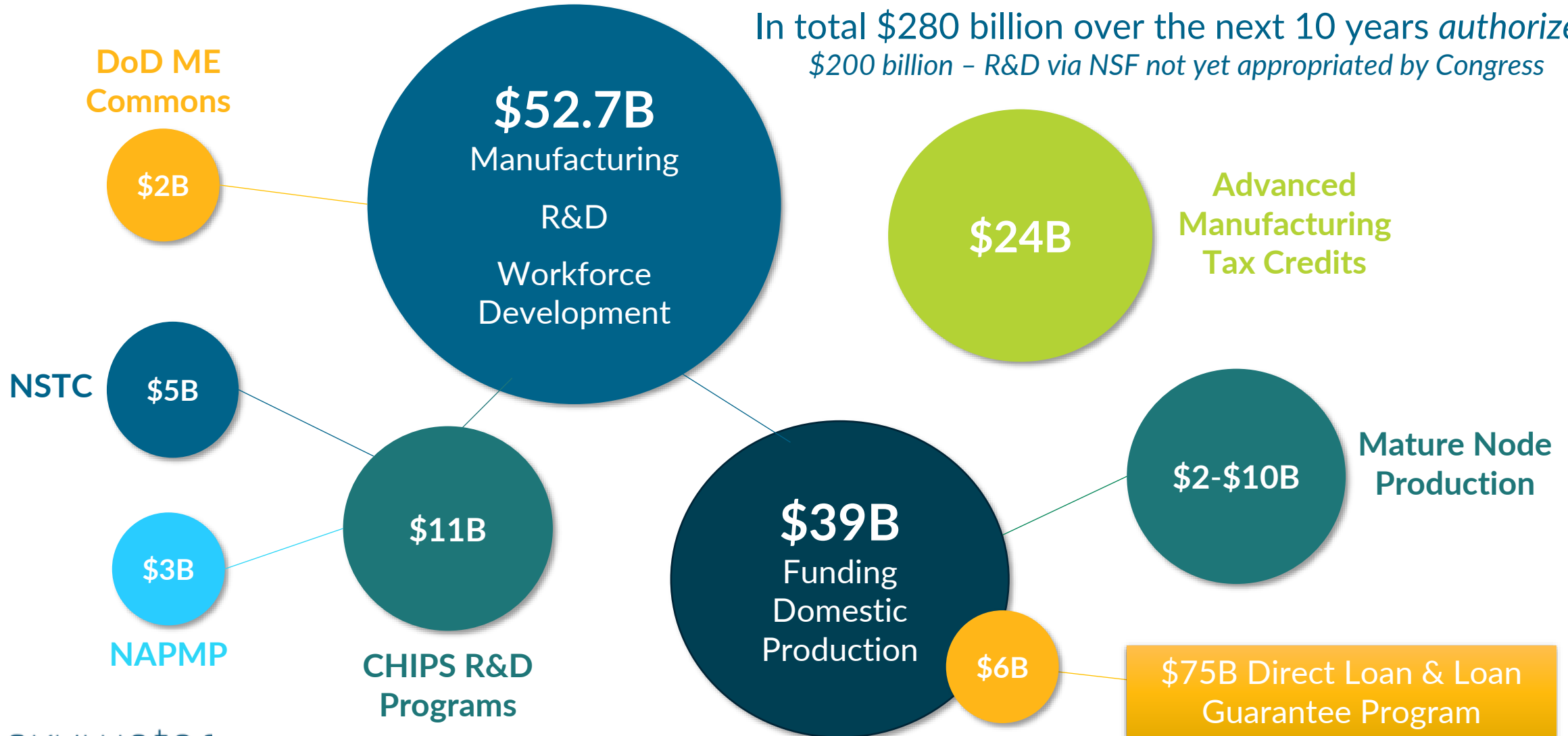
From President Biden holding up a SkyWater wafer at the virtual Chip Summit last year to the signing of the CHIPS & Science Act of 2022, SkyWater has supported this critical initiative.

SkyWater Applauds Historic Legislation to Stimulate US Semiconductor Production

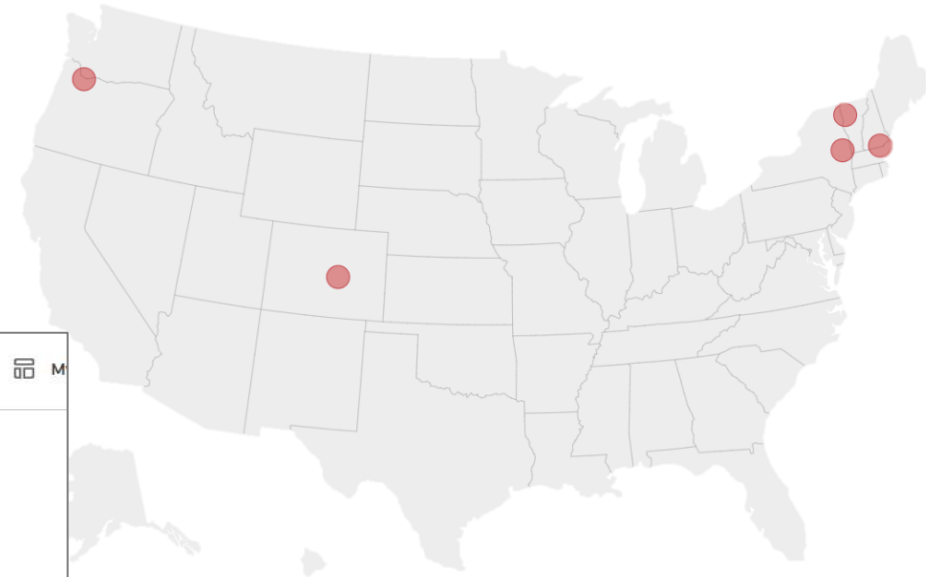
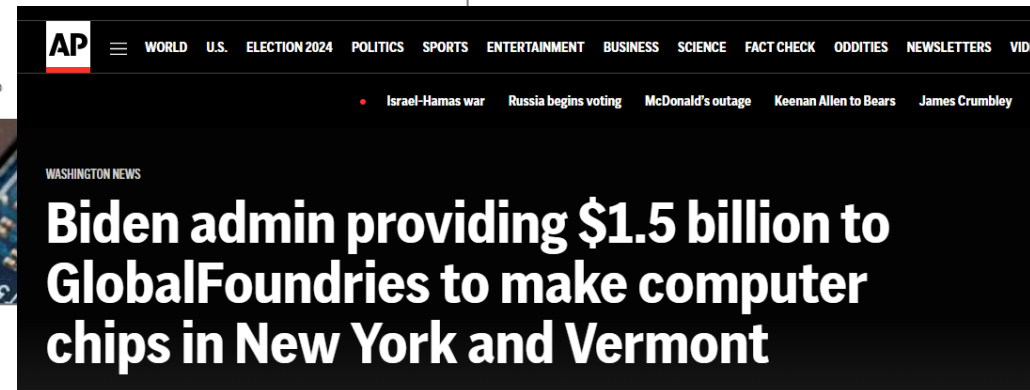
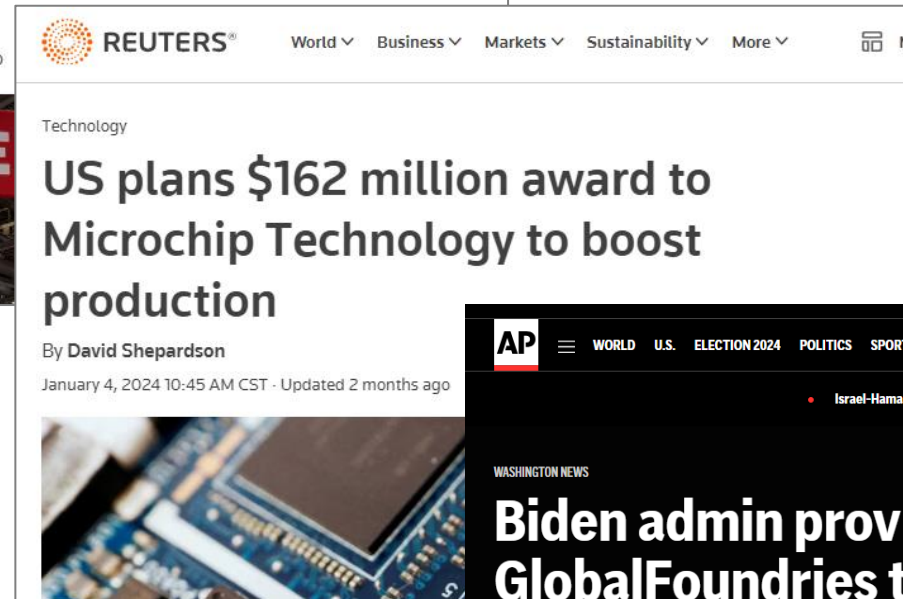


# CHIPS & Science Act Funding

In total \$280 billion over the next 10 years *authorized*  
 \$200 billion – R&D via NSF not yet appropriated by Congress



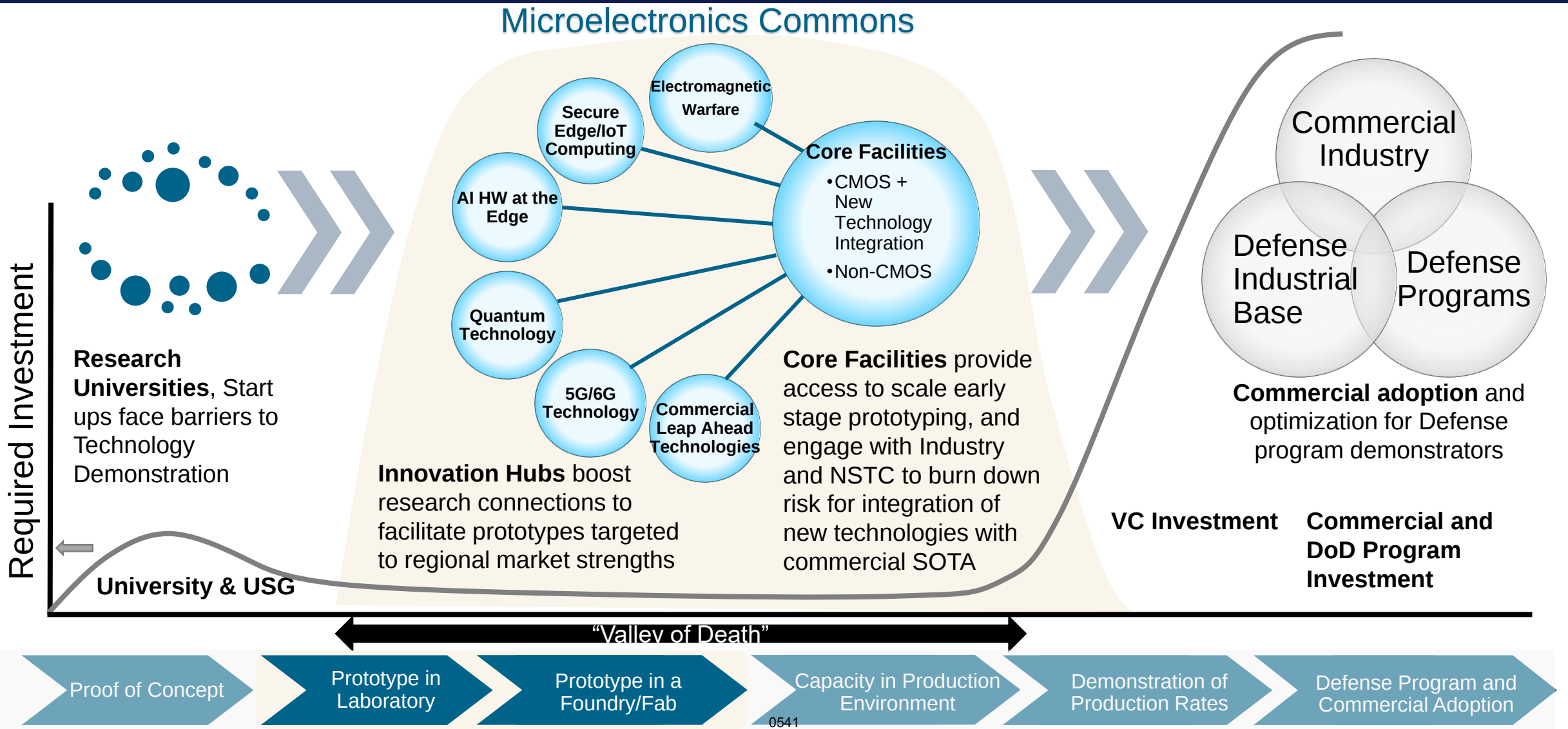
# \$1.6 Billion in CHIPS Awards





# Microelectronics Commons Addresses the Valley of Death

THE OFFICE OF THE DEPUTY TECHNOLOGY OFFICER FOR CRITICAL TECHNOLOGIES





# Microelectronics Commons Awardees

THE OFFICE OF THE DEPUTY TECHNOLOGY OFFICER FOR CRITICAL TECHNOLOGIES



*The responses to the RFS represented the innovation of a combined membership network of 642 unique organizations*

## Applied Research Institute

*Silicon Crossroads  
Microelectronics  
Commons (SCMC) Hub*

## Arizona Board of Regents on behalf of Arizona State University

*Southwest Advanced  
Prototyping (SWAP) Hub*

## The Board of Trustees of the Leland Stanford Junior University

*California-Pacific-Northwest  
AI Hardware Hub  
(Northwest-AI-Hub)*

## Massachusetts Technology Collaborative

*Northeast Microelectronics  
Coalition (NEMC) Hub*

## Midwest Microelectronics Consortium

*Midwest Microelectronics  
Consortium (MMEC) Hub*

## North Carolina State University

*Commercial Leap Ahead for  
Wide-bandgap  
Semiconductors (CLAWS)  
Hub*

## The Research Foundation for SUNY, acting on behalf of SUNY Polytechnic Institute

*Northeast Regional Defense  
Technology Hub  
(NORDTECH)*

## University of Southern California

*California Defense Ready  
Electronics and Microdevices  
Superhub (California  
DREAMS)*

# DOD Industrial Base and Sustainment Program (IBAS)

- IBAS ensures DOD is positioned to address industrial base issues and support National Security innovation base
- IBAS Advanced Packaging focus is known as RESHAPE (Reshore Ecosystemfor Secure Heterogeneous Advanced Packaging Electronics).



- NeoCity in Osceola County, Florida launched its Cornerstone collaboration in January.
- establishing Fan Out Capability in the United States (eFOCUS) 5-year contract awarded with a spending ceiling of \$120 million and options for an additional \$169 million, potentially resulting in a total award of \$289 million.

# Strengthening Domestic Advanced Packaging Technologies

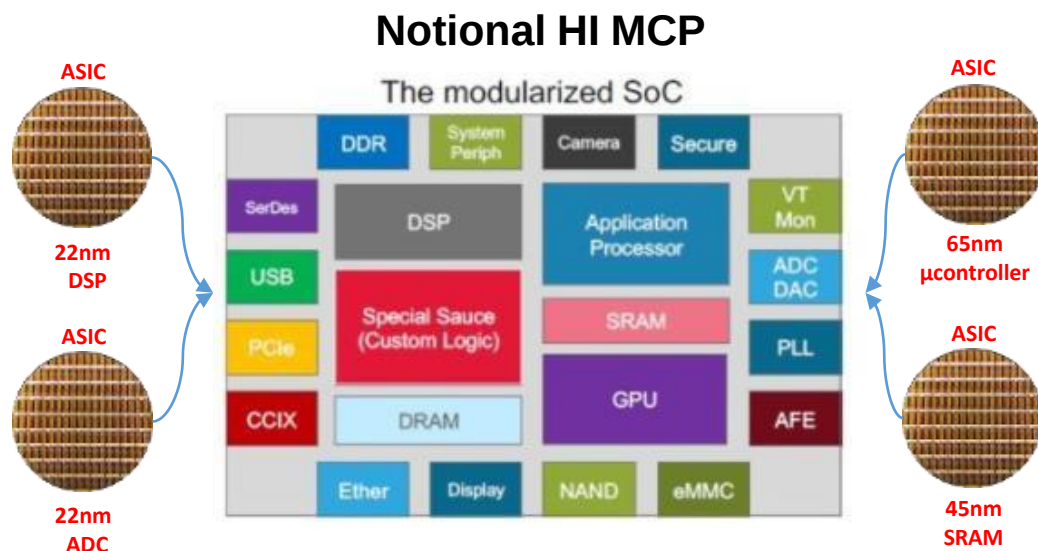




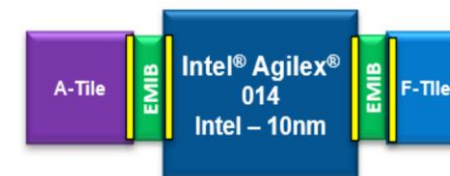
# Heterogeneous Integration (HI) and SWAP Benefits

## Why HI?

- Modular approach vs. Monolithic approach
- Not every logic function (IP) needs to be designed in the same process node (HI)
- Leveraging IP in the form of chiplets
- Current industry trend has led to chiplets on silicon interposers
- Includes latest IC packaging 2.5D, 3D, FOWLP technologies
- Optimize nodes required for ideal performance and cost



**SHIP is leveraging commercial HI solutions to improve SWAP savings and system performance**

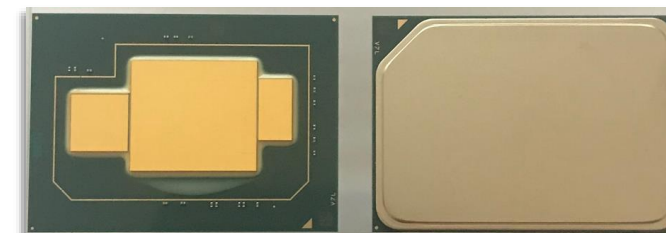


Expected SWAP Savings:  
8x relative to current solution

Through HI enabled SWAP savings, MCP-1 will deliver:

- ✓ Unprecedented spectral agility
- ✓ Enhanced signal processing
- ✓ Lower power consumption
- ✓ Improved thermal management

SHIP-D functional parts have been delivered to lead DIB partner to prove SWAP benefits



MCP-1 consisting of two chiplets integrated with an FPGA

MCP-1 finished package

# Heterogeneous Integration is the Path Forward

Many variations of HI exist; all are striving to increase interconnect and electronic module density to improve size, weight, power and performance.

Silicon Interposer

 **mec**

Wafer Bonding

**adeia**<sup>™</sup>

Fan-Out Wafer Level Packaging

 **DECA**

# Fan-Out Wafer Level Packaging

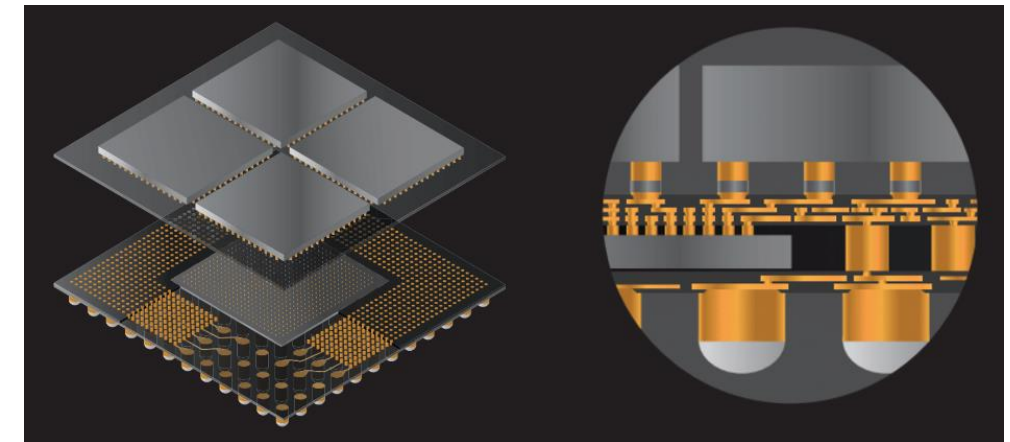
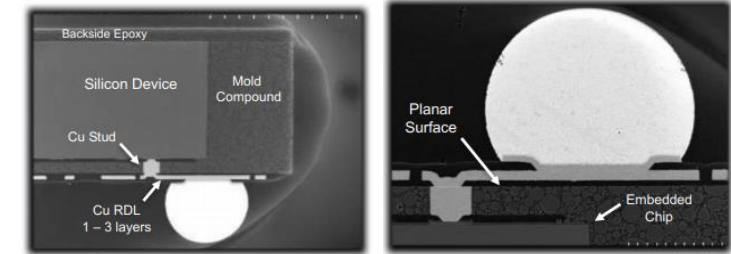


## \$120M Cornerstone RESHAPE program award to establish Fan Out capability in the U.S. (eFOCUS) awarded to SkyWater/Osceola County

- Complete fab tool install with test vehicle build and characterization
- Deca Technology is SkyWater's FOWLP technology partner, under license agreement.

### Deca FOWLP Technology Benefits:

- Highest volume FOWLP technology deployed today, with superior reliability and yield
- Supports multiple die integration in a single package
- Gen 2 capabilities will incorporate additional RDL layers, smaller RDL line/space dimensions, and 20um I/O pitch die
- Supports multiple package architectures and applications



# Successful Collaboration will ensure US Semiconductor Leadership for Years to Come

Revitalize  
Domestic  
Manufacturing

Develop  
the  
Workforce

Strengthen  
Partnerships

Accelerate  
Technologies  
of the Future

