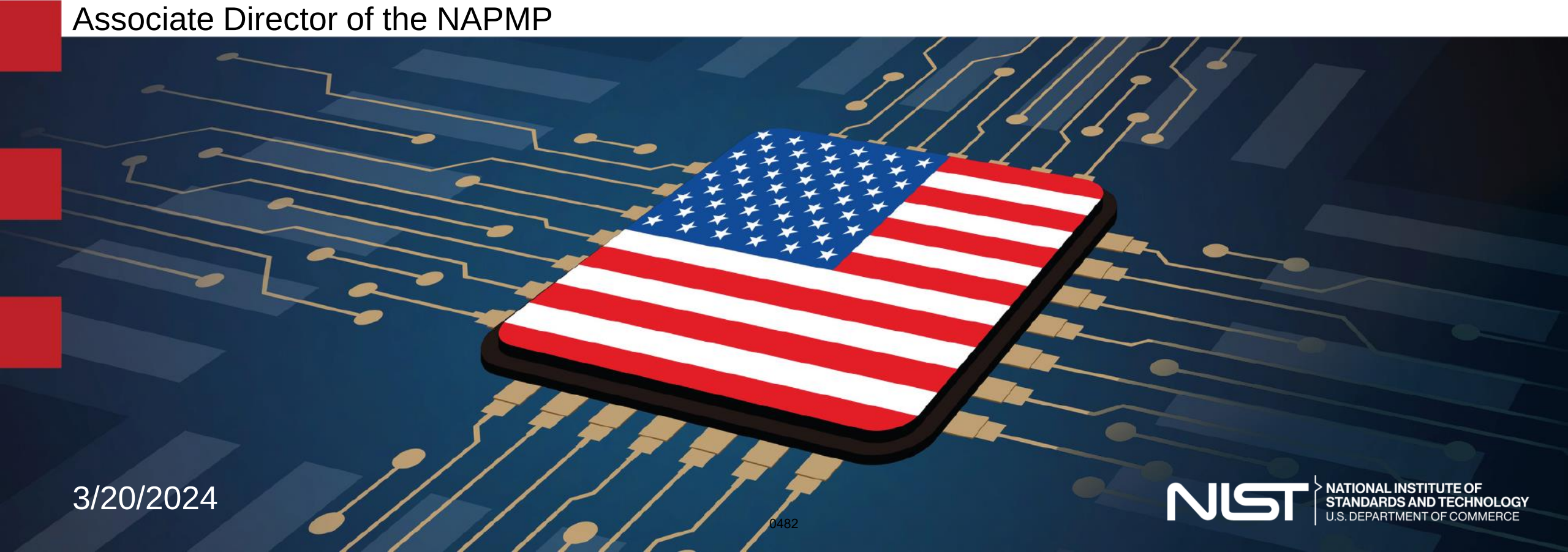


CHIPS for America, National Advanced Packaging Manufacturing Program (NAPMP) and R&D Update

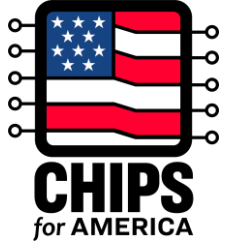
Daniel Berger

Associate Director of the NAPMP



3/20/2024

0482

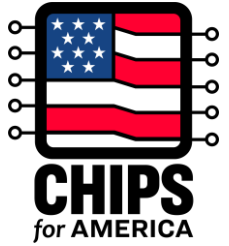


Disclaimer

Statements and responses to questions about advanced microelectronics research and development programs in this webinar:

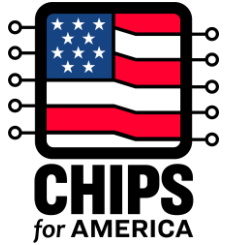
- Are informational, pre-decisional, and preliminary in nature.
- Do not constitute a commitment and are not binding on NIST or the Department of Commerce.
- Are subject in their entirety to any final action by NIST or the Department of Commerce.

Nothing in this presentation is intended to contradict or supersede the requirements published in any future policy documents or Notices of Funding Opportunity.

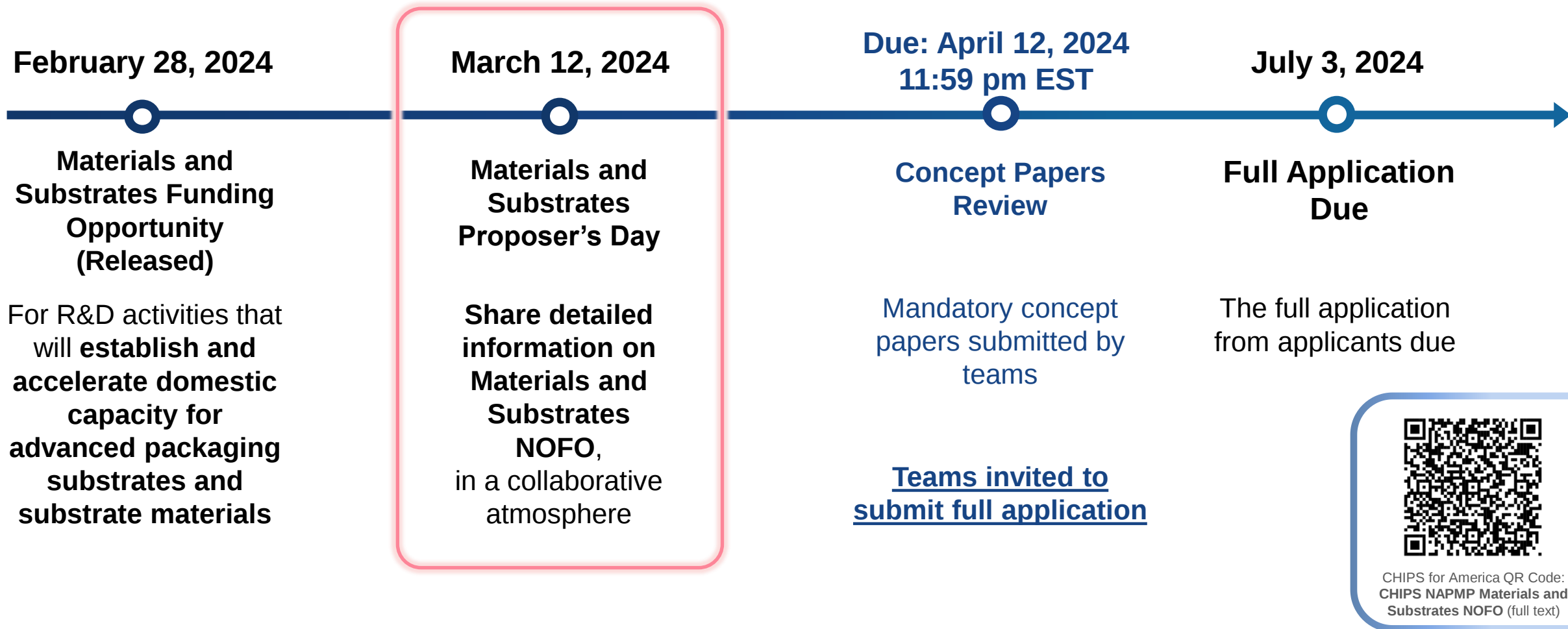


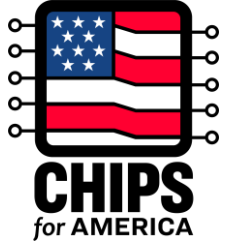
NAMPM Proposer's Day – March 12th



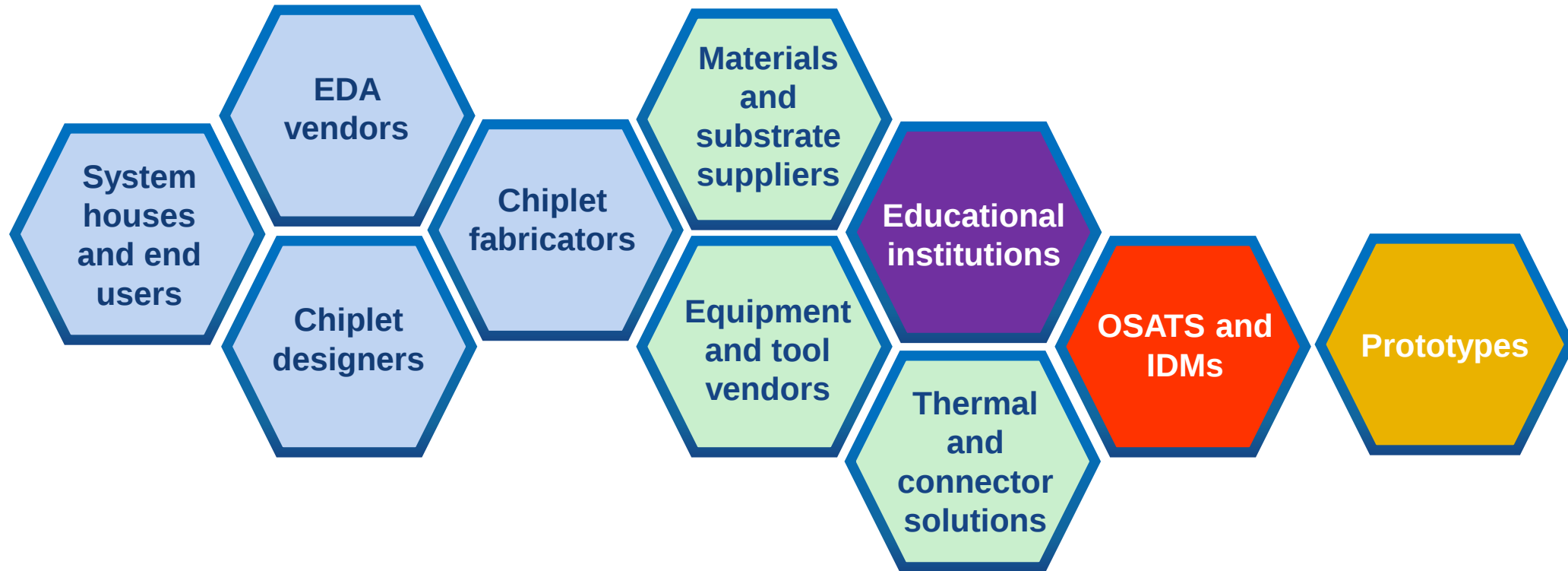


Materials and Substrates NOFO: key dates

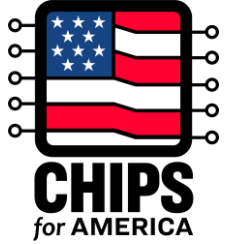




Collaboration is Critical for Success



We encourage you to begin identifying your individual contributions to the ecosystem as well as partners who can help accomplish the vision and goals of the NAPMP.



CHIPS for America

\$39 billion for incentives

Two component programs to:

1. Attract large-scale investments in advanced technologies such as leading-edge logic and memory, and advanced packaging
2. Incentivize expansion of manufacturing capacity for mature and other types of semiconductors

\$11 billion for R&D

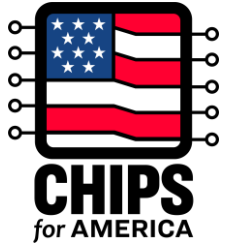
Four integrated programs to:

1. Conduct research and prototyping of advanced semiconductor technology
2. Strengthen semiconductor advanced packaging, assembly, and test
3. Enable advances in measurement science, standards, material characterization, instrumentation, testing, and manufacturing

Together with
CHIPS initiatives
from other
agencies, including
DOD, State, NSF,
and Treasury

Workforce Initiatives

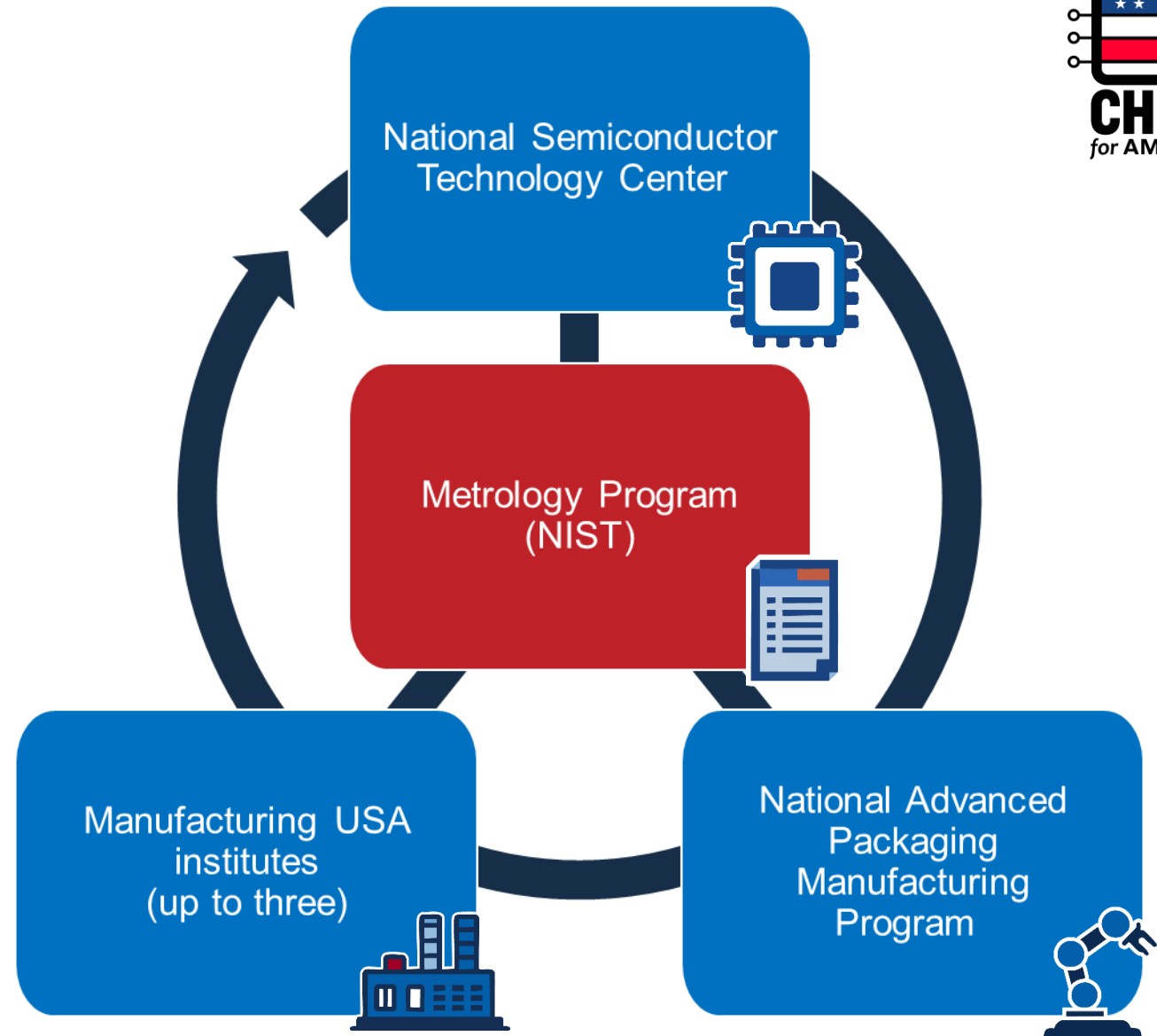


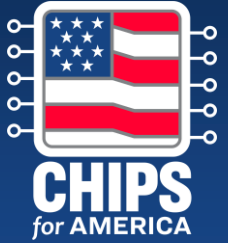


CHIPS R&D

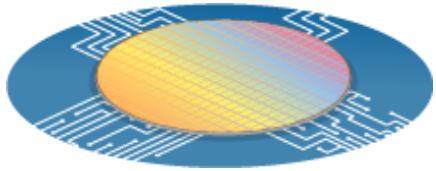
Vision A vibrant and self-sustaining U.S. domestic semiconductor ecosystem that revitalizes American manufacturing, grows a skilled and diverse workforce, and leads the world in semiconductor research and innovation.

Mission Accelerate the development and commercial deployment of foundational semiconductor technologies by establishing, connecting, and providing access to domestic research efforts, tools, resources, workers, and facilities.





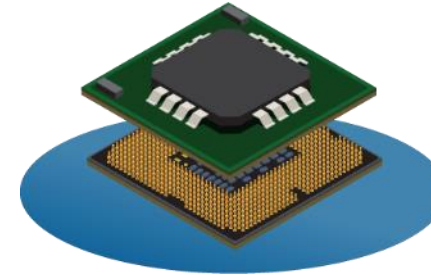
CHIPS R&D Programs



**CHIPS National
Advanced Packaging
Manufacturing
Program (NAPMP)**



**CHIPS Manufacturing
USA Program**



**CHIPS National
Semiconductor
Technology Center
(NSTC) Program**



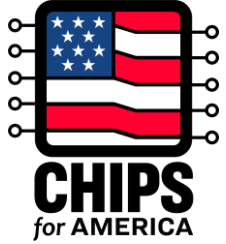
Natcast is an independent nonprofit organization
and operator of the NSTC consortium



**CHIPS Metrology
Program**

Workforce Initiatives





Establishing Advanced Packaging in the U.S.

Packaging Roadmaps

- NIST-sponsored roadmaps: MRHIEP, MAESTRO and MAPT
- Other roadmaps: HIR and IRDS

Technology Investment Areas

- All aspects of technologies required to develop a leading-edge on-shore advanced packaging manufacturing capability

The National Advanced Packaging Piloting Facility (NAPPF)

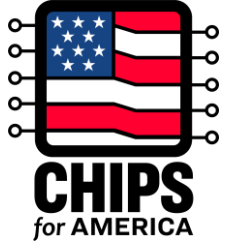
- Key to facilitating high-volume manufacturing
- Piloting and prototyping functions

The Chiplet and Design Ecosystem

- Chiplet discovery, disaggregation and reaggregation methodologies, protocols, standards, fabrication and warehousing design for test, repair and reliability, and holistic design tools and methodologies

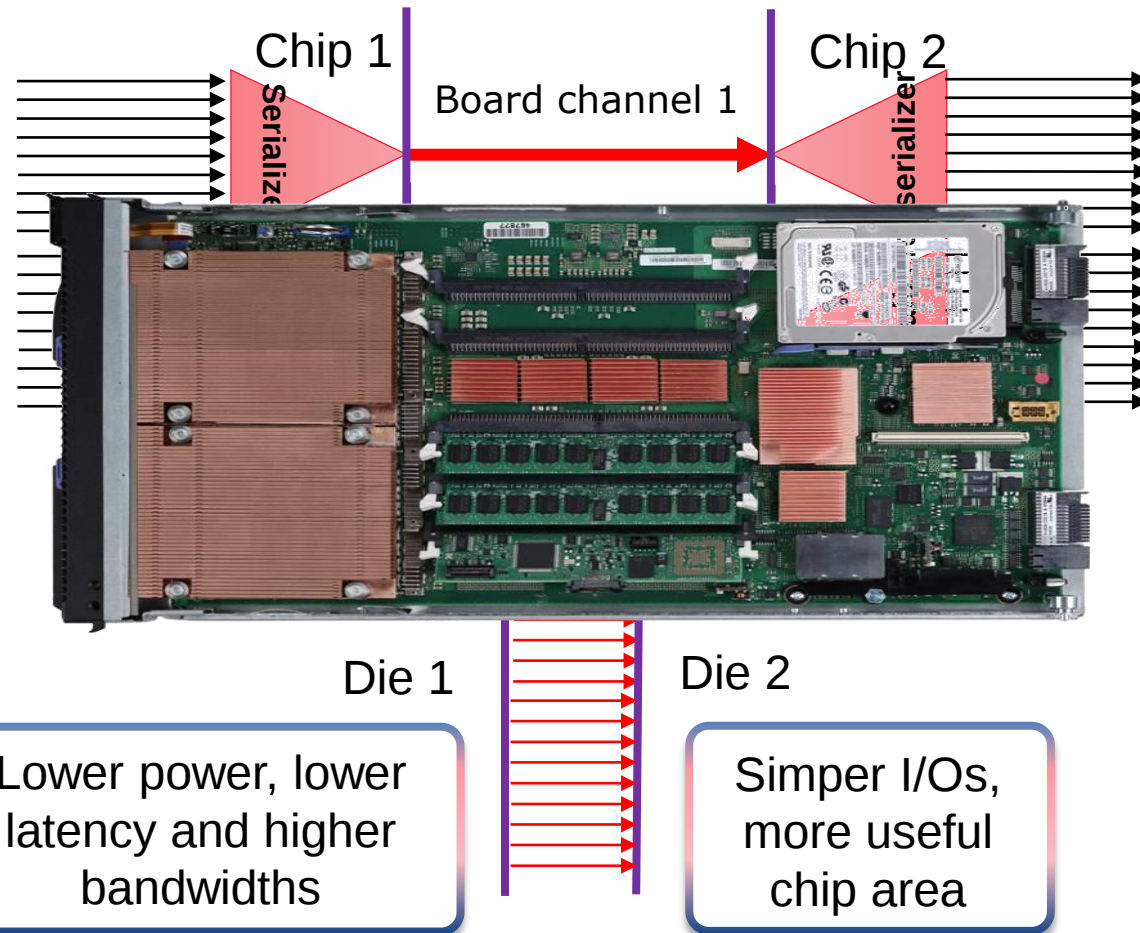
Design in the U.S., build in the U.S., and sell worldwide

- Successful development efforts will be transitioned and validated for scaled transition to U.S. manufacturing



Advanced packaging is all about scale

The difference now is scale:

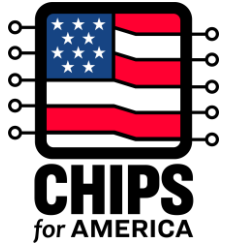


- More Channels on the package
 - Finer "bump/pillar" pitch
 - Approach on-chip via pitches ($<1 \mu\text{m}$)
- Finer Trace Pitch
 - Approach on-chip wiring pitches
- Shorter inter die distance
 - $\sim \mu\text{m}$

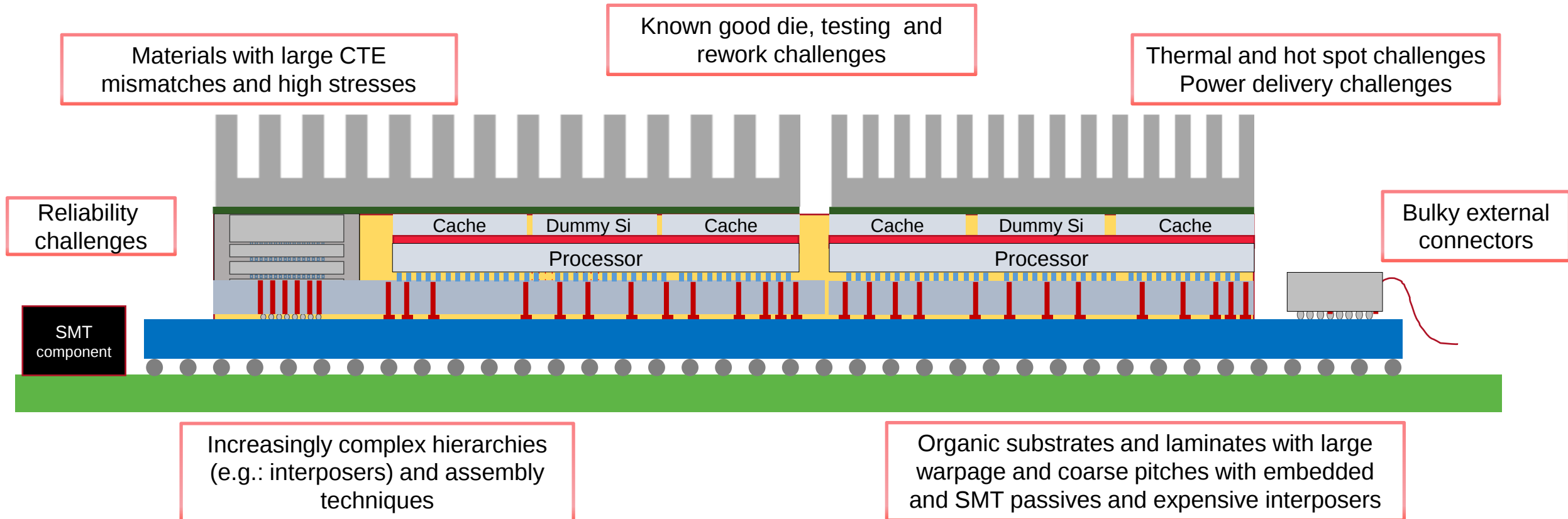
Scale Down

- Significantly more intimately connected Silicon

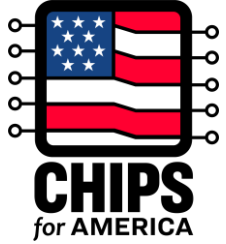
Scale Out



We do it today — but with complexity and added hierarchy



Simplify packaging and make it cost effective to manufacture in the US



The Role of the package

Mechanical protection

- Handling
- Stability

Environmental protection

- Moisture
- Hermeticity
- Corrosion

Thermal protection

- Heat spreading
- Heat sinking
- Hotspot reduction

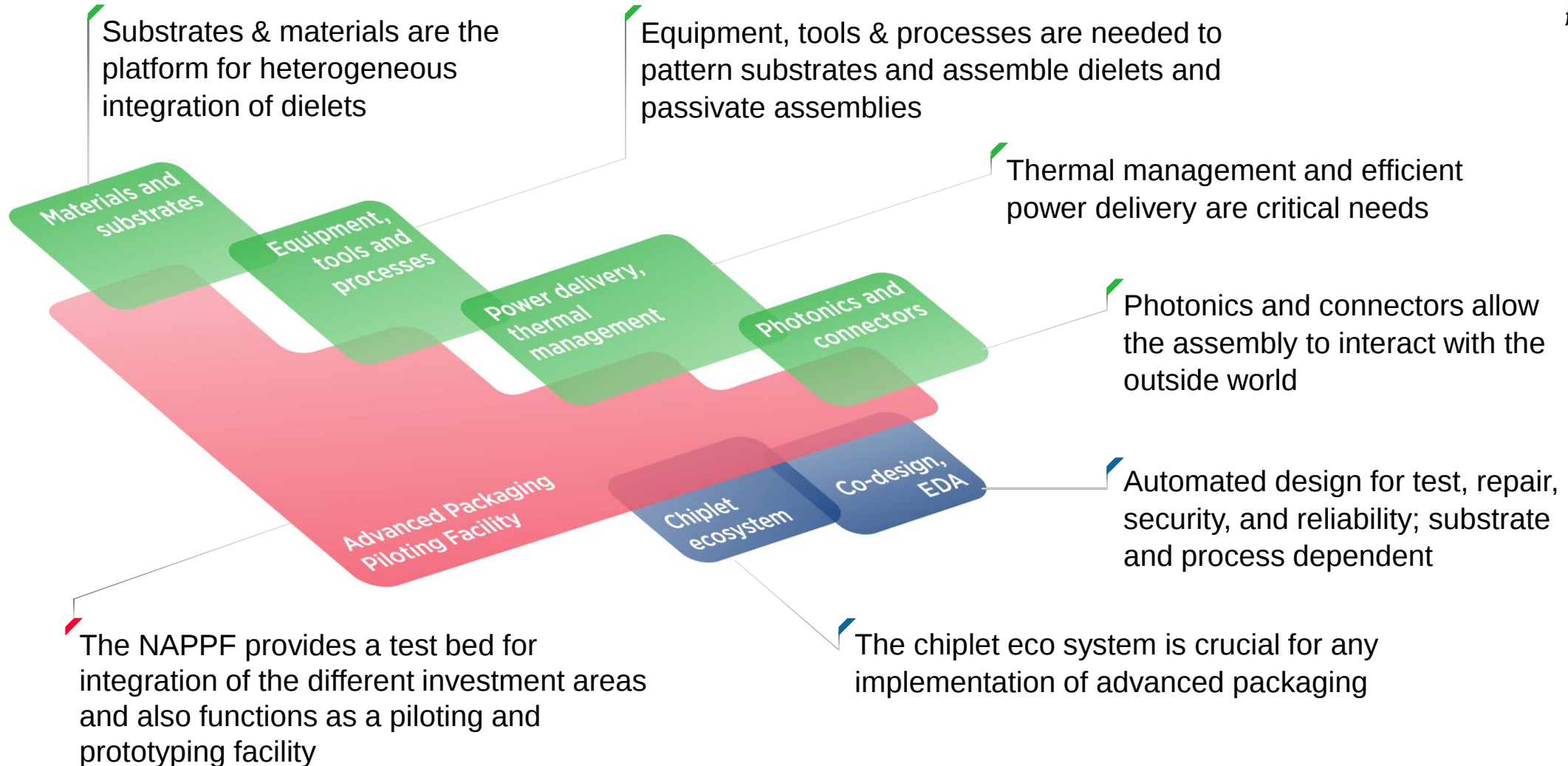
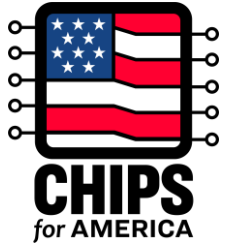
To protect and to serve

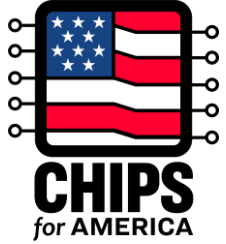
Connect electrically
to other chips

Deliver
power

Stable test and
integration platform

NAPMP Structure: six hardware and eco-system thrusts + piloting facility + prototyping challenges

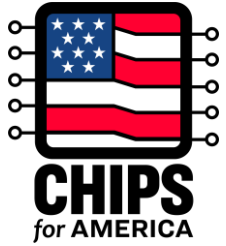




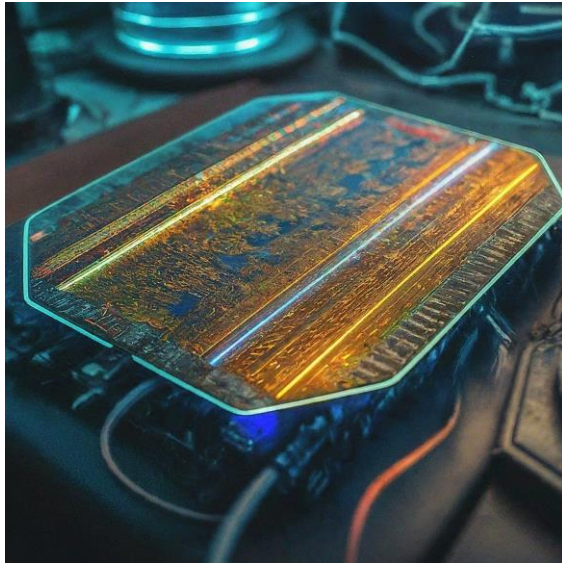
The National Advanced Packaging Piloting Facility (NAPPF) - Where it all comes together

- Investment Area Thrusts should connect activities with the APPF
- NAPPF will be focused on integrated process flows that can reach commercial scale
- NAPPF will be focused on validating new technology specifications, compatibility with other processes, yield, and reliability
- The NAPPF will be focused on assessing technologies for scaled transition to U.S. manufacturing including yield and reliability
- We will do this with baseline processes and prototyping and piloting exemplars





Choosing exemplars and corresponding baseline processes



AI and HPC

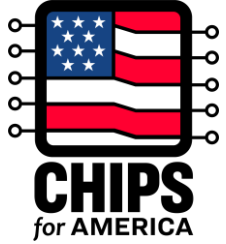


Low power
edge communication
Medical Electronics
devices

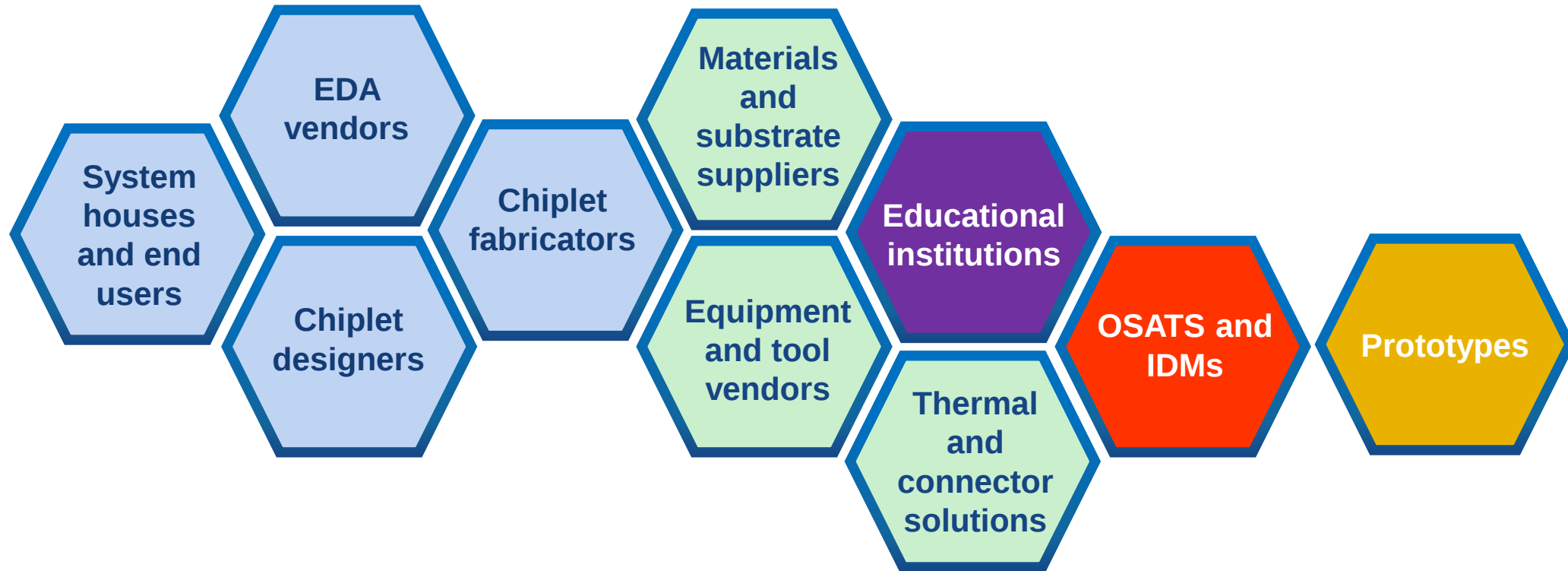


Others: auto,
extreme

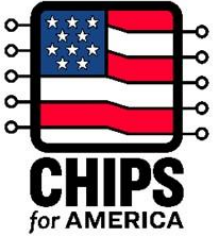
We could probably run two or three baseline processes in the NAPPF based on our three substrate types



Collaboration is Critical for Success

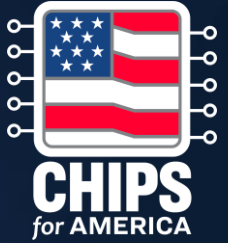


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Next Steps

- [NOFO](#): CHIPS National Advanced Packaging Manufacturing Program (NAPMP) Materials and Substrates
- Visit [CHIPS.gov](https://chips.gov) for resources, including:
 - List of Funding Updates
 - Funding Opportunities
 - Vision for Success papers
- Join our mailing list
- Contact us
 - askchips@chips.gov – general inquiries
 - apply@chips.gov – application-related inquiries



Thank you for attending

Visit CHIPS.gov for future updates and additional information