Memory Chip-to-Chip Integration for High Bandwidth Memory Processor Interface

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Outline

- Motivation
- System Build-up
- Components
  - Processor
  - Memory
- Assembly
- Design Enablement by ADK
- Summary and Outlook

Motivation

- Rising demand for memory apparent in most electronic systems
  - Artificial intelligence
  - Network nodes in 5G infrastructure
  - Edge computing
- Additional - rising demand for speed and/or bandwidth

Motivation

- Currently two ways to solve the problem
  - SoC with memory inside the chip
    - Limited in size of memory
    - Same technology must be used
  - HBM with interposer
    - High end solution – TSVs have to be included inside the memory
    - Interposer required as package

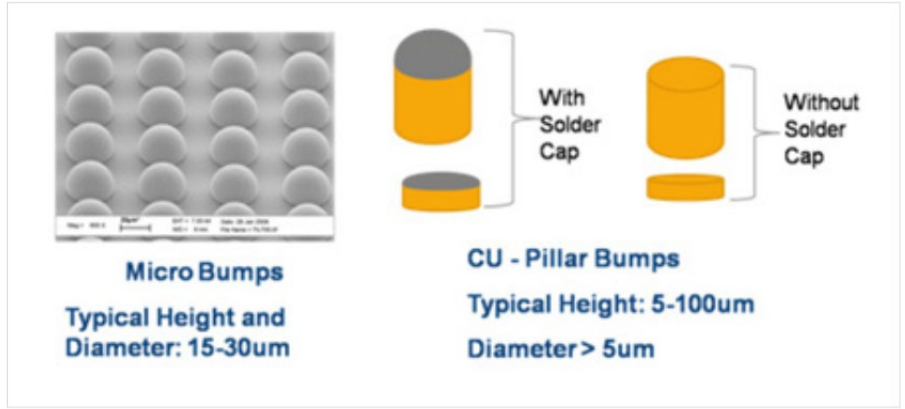
Motivation

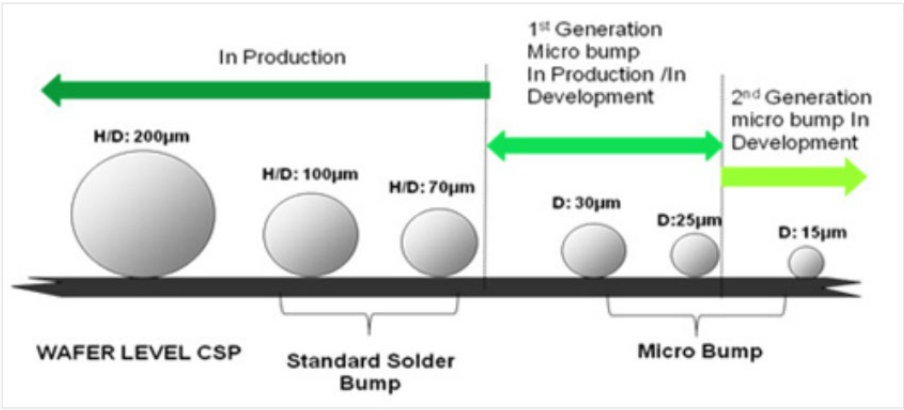
- Low cost options beside HBM are limited in additional rising of speed and density
  - Memory can occupy more then 50% area in SoCs
  - Side by side approach limits the number of connections and length of connections

- Also for high end solutions like HBM further enhancement of bandwidth limited, by number of physical contacts on the chip

Motivation

- Copper pillars are small physical contacts
  - In general assembly of ICs on package substrates
  - Increasing number of connections per area
  - Pitch even below 100um





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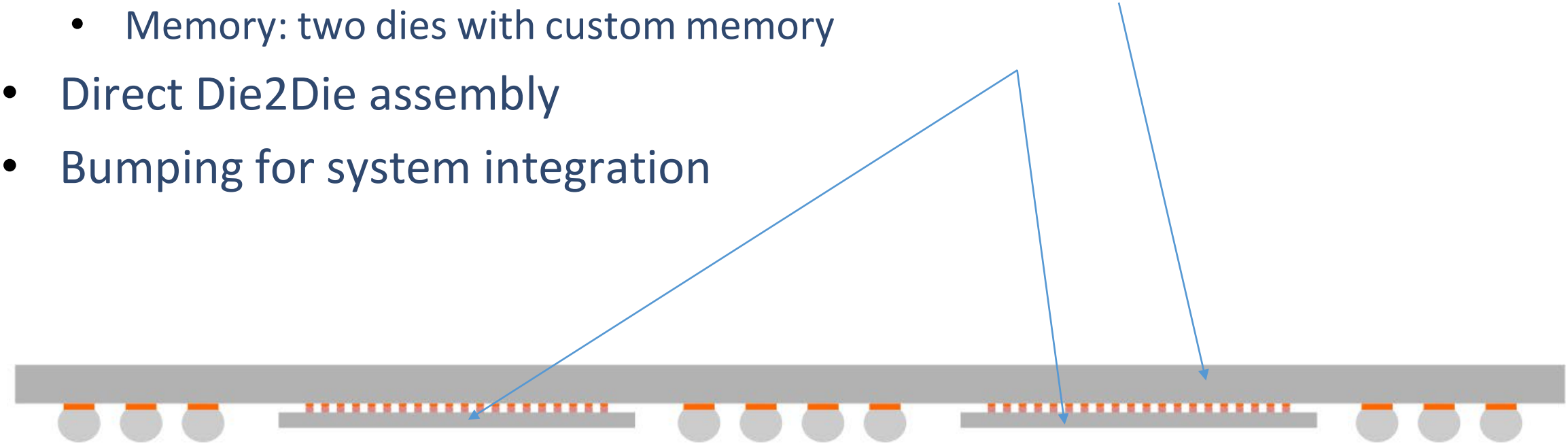
System Build-up

- Proposed approach – Face-to-Face integration of memory and processor

- Face-to-Face integration of processor and memory enables both
  - High-speed (very short connection compared to SoC up to 20mm and HBM up to 50mm)
  - High-bandwidth (more then 100 connections per mm^2 - up to processor speed)
  - Different technologies for memory and processor possible

System Build-up

- Stacked system with two components
  - Processor: an integrated circuit in FD-SOI technology
  - Memory: two dies with custom memory
- Direct Die2Die assembly
- Bumping for system integration

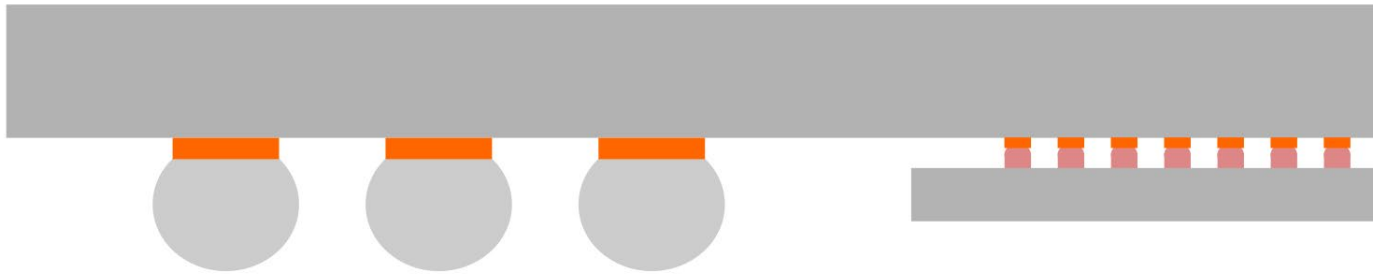


System Build-up

- High-bandwidth (more then 100 connections per mm² - up to processor speed)
  - 100 connections * 2Ghz -> 200Gbit/s/mm²
  - Every memory 10mm² -> 2Tbit/s/memory

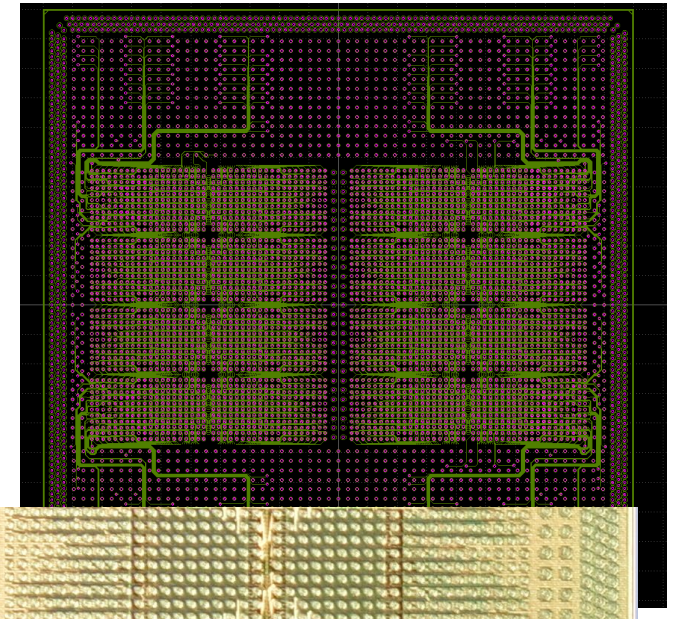
System Build-up

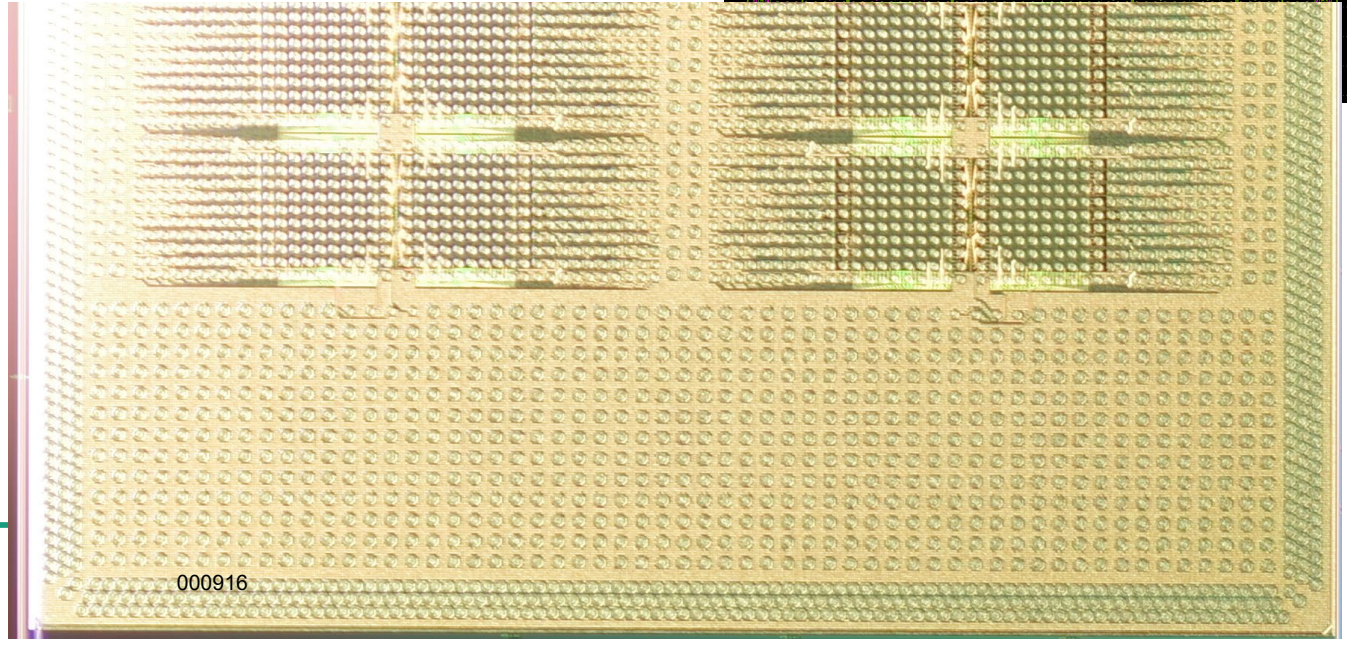
- Memory IC is equipped with copper pillars
  - Flip-Chip assembly to processor IC
  - Thinned device to fit assembly of bumps
- Processor IC
  - Wafer-Level-Package Fan-In; Equipped solder balls
- Very close communication channel between IC and memory



Components - Processor

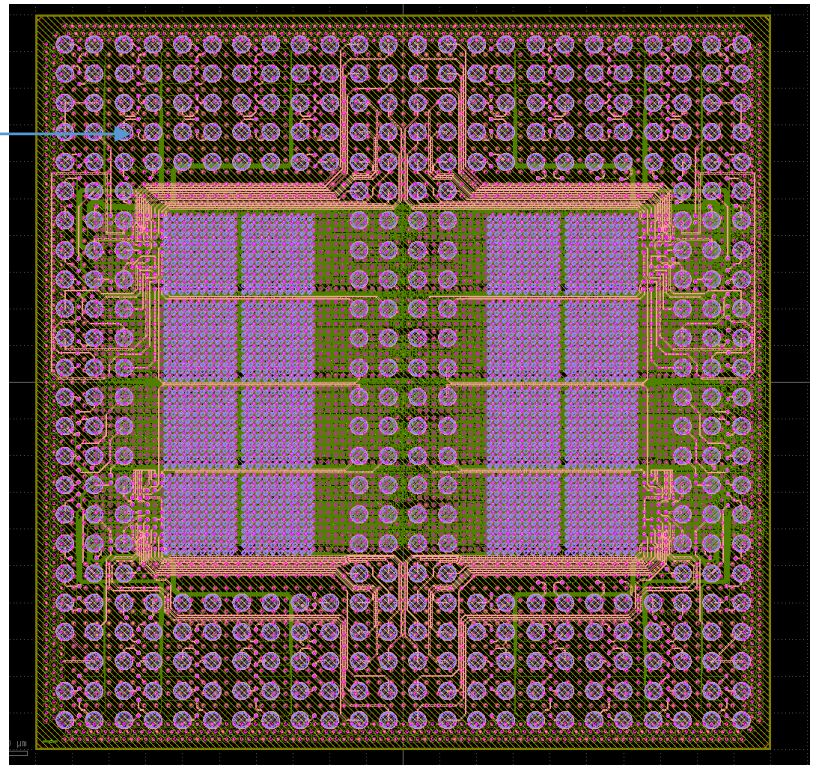
- 10x10 mm IC fabricated on FD-SOI technology
- Standard BEOL stack
- Manufacturing sample





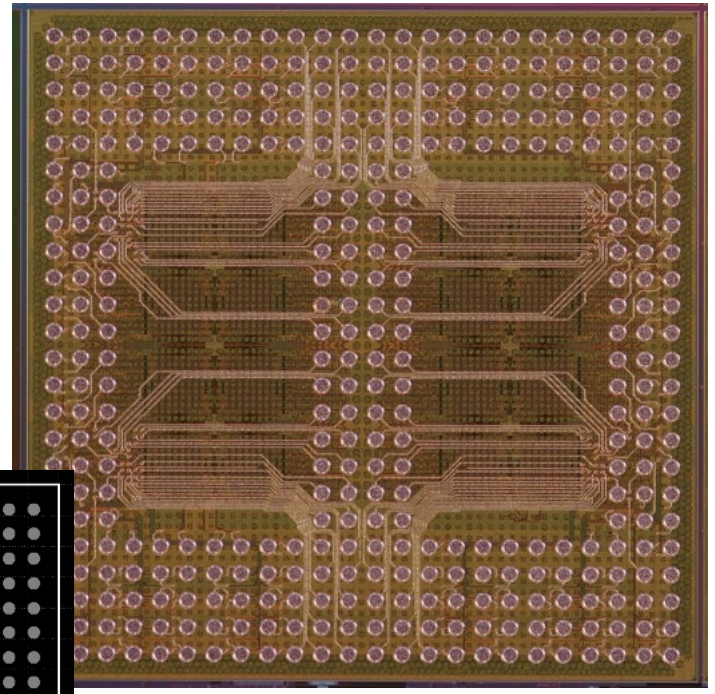
Components - Processor

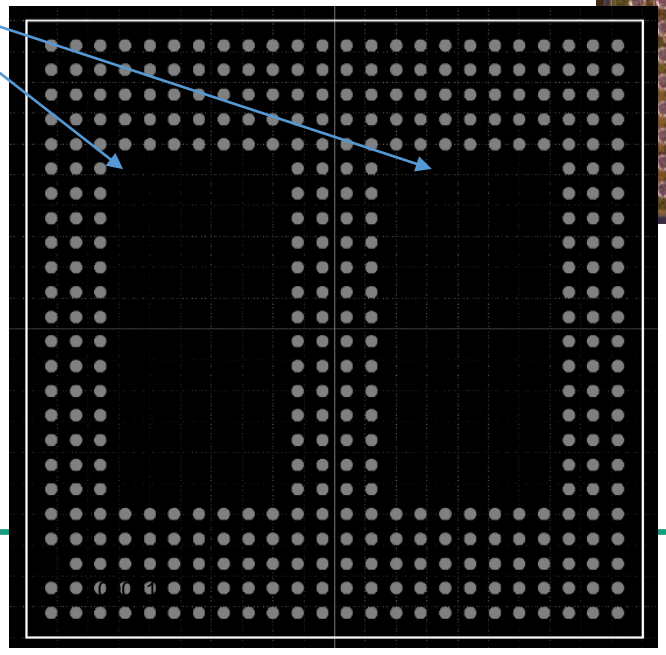
- After BEOL manufacturing WLPFI RDL is applied
- Slight modification of foundry standard WLPFI process
  to enable die2die assembly



Components - Processor

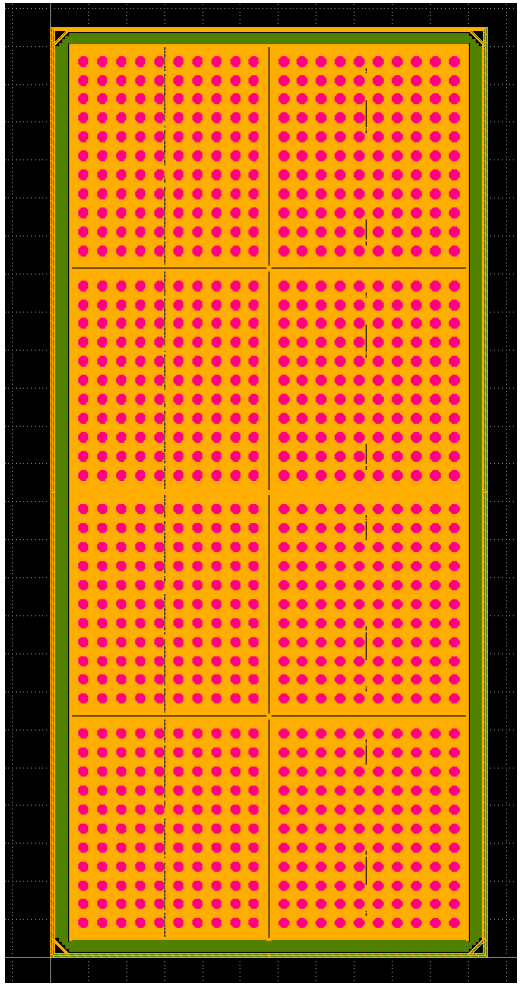
- Wafer-Level-Package-Fan-In RDL
- Bumping layout
  - Spare areas for memory ICs





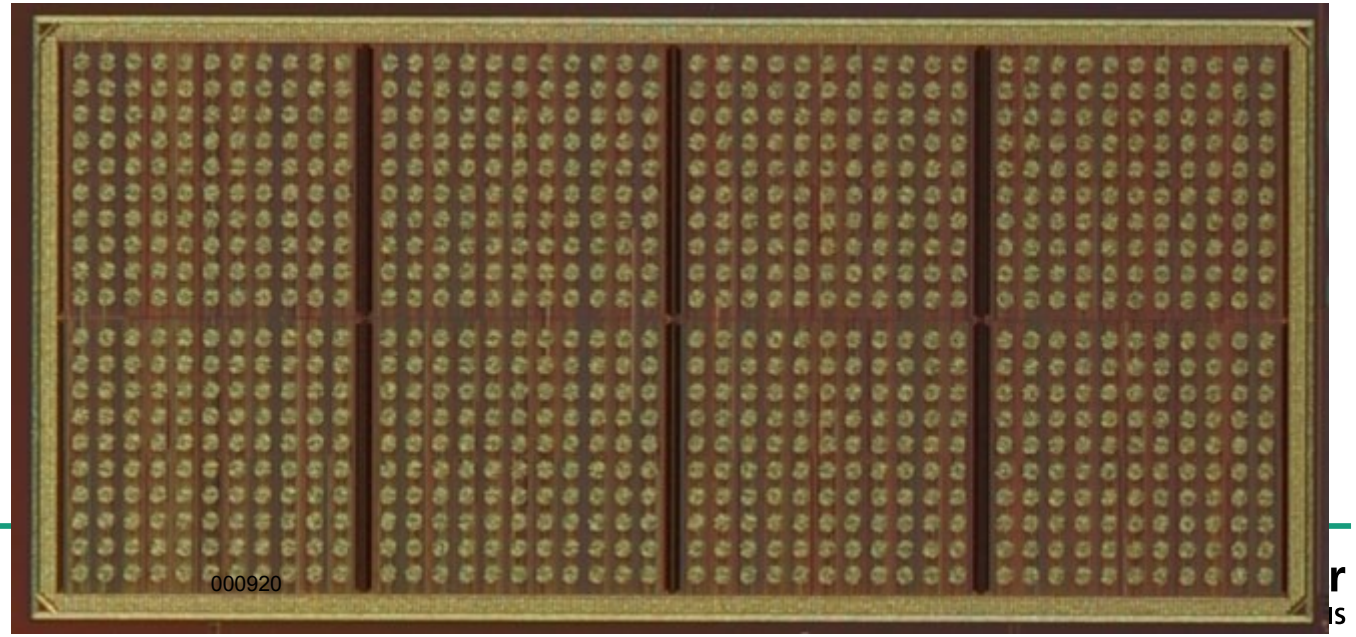
Components - Memory

- Integrated memory device with a size of 2.3x 4.9 mm
- Block organization
  - 2x4 indepedent blocks
- System: each FPU alligns to a dedicated memory block



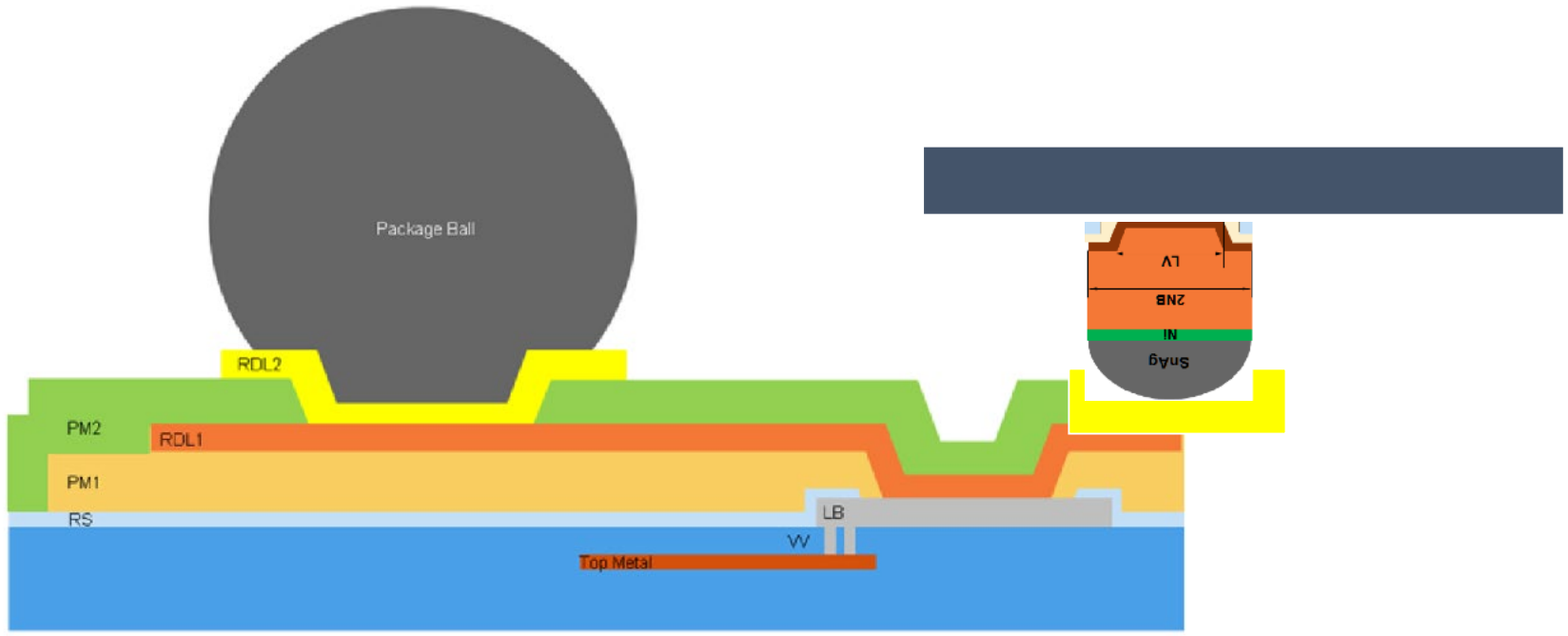
Components - Memory

- Equipped with copper pillars
  - 50um diameter
  - 100um pitch
  - Around 58um pre-assembly stand-off height



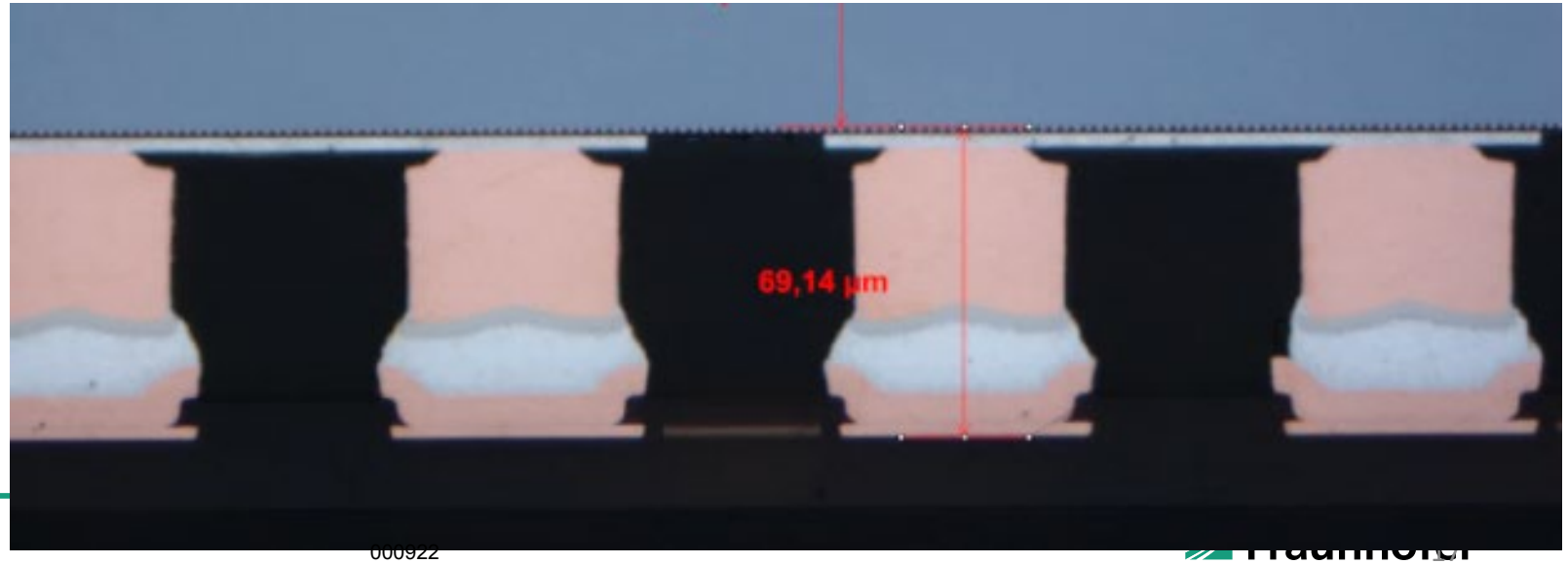
Assembly Details

- Assembly involves processor and memory ICs
- Flip-Chip copper pillar assembly to IC with WLPFI RDL
- Bumping of
  the processor IC



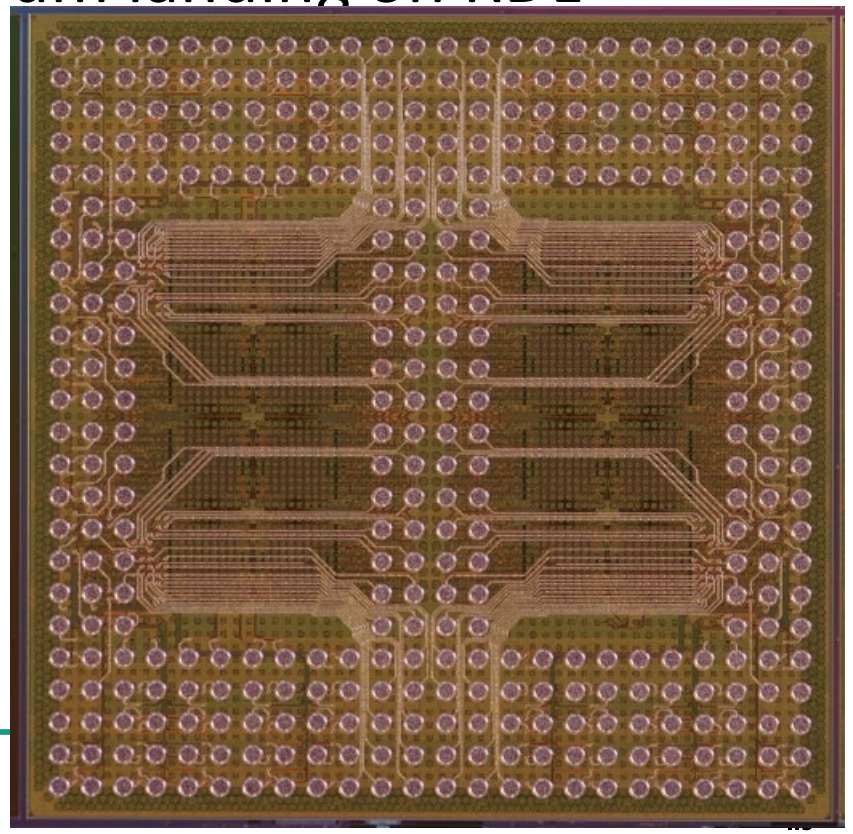
Assembly Details - Copper Pillars

- Memory IC is equipped with copper pillars
- Assembly cross section shows final copper pillar stand-off height after assembly on RDL
- Copper pillar build-up
  - Copper
  - Nickel
  - SnAg



Assembly Details - Bumping

- Processor IC involves bumping as WLPFI
- Solder balls with 250um diameter and 190um landing on RDL
- Pitch of 400um

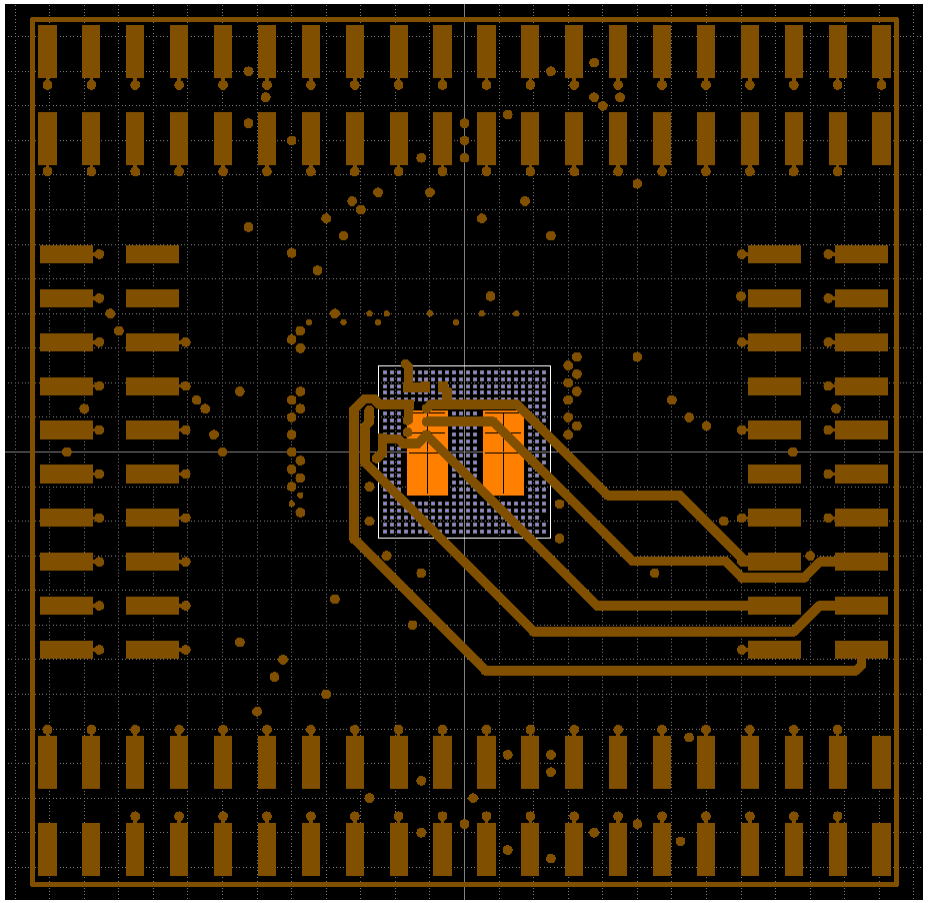


Process Flow

- Independent manufacturing of processor and memory
  - Copper pillars are part of memory IC processing
  - WLPFI is applied to the processor IC
- Bumping the processor IC on wafer-level
- Flip-Chip assembly of memory to processor
- Final assembly of the system to a validation printed circuit board

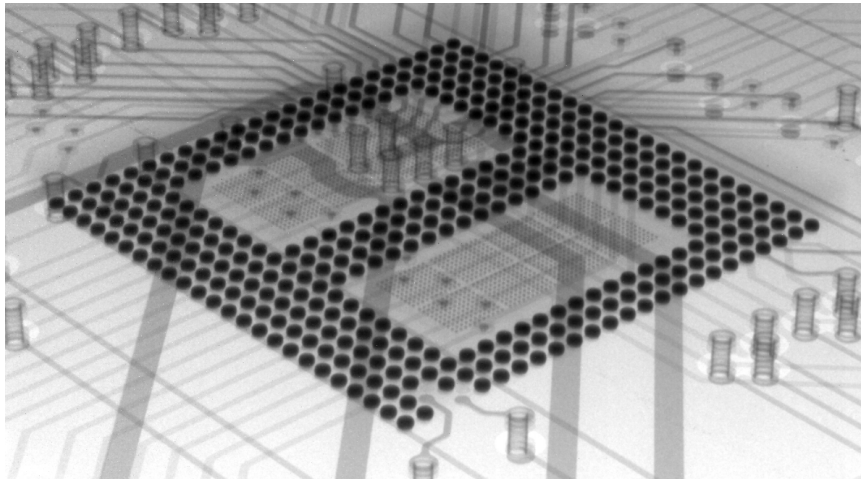
Validation PCB

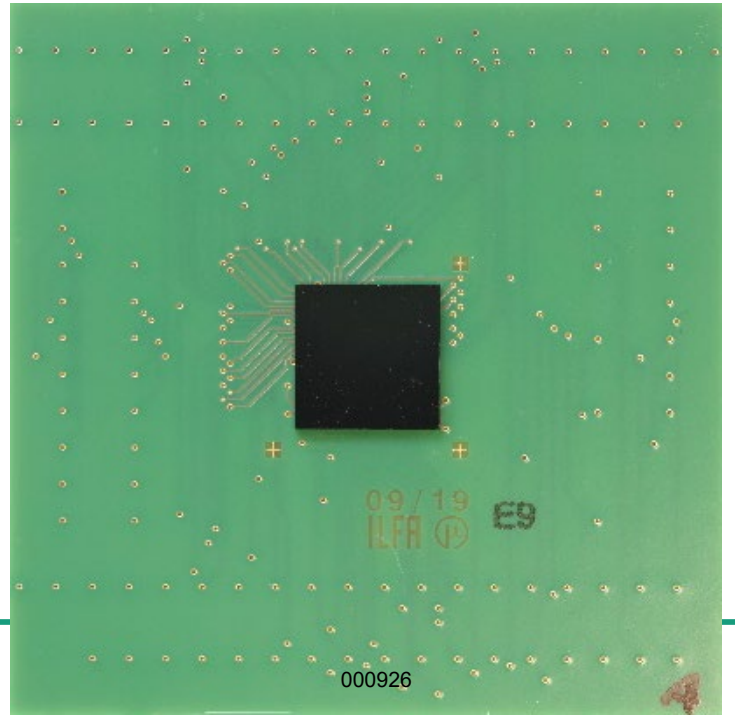
- Stack is assembled on PCB
- PCB assembly validation
- Functional and performance validation
- Allignment of measurements and simulation results

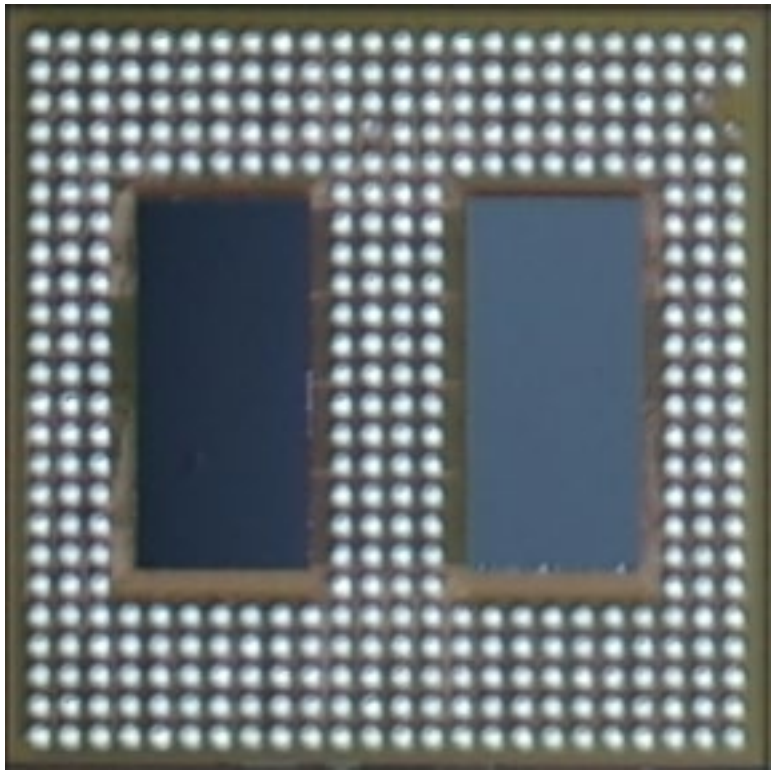


Production Sample

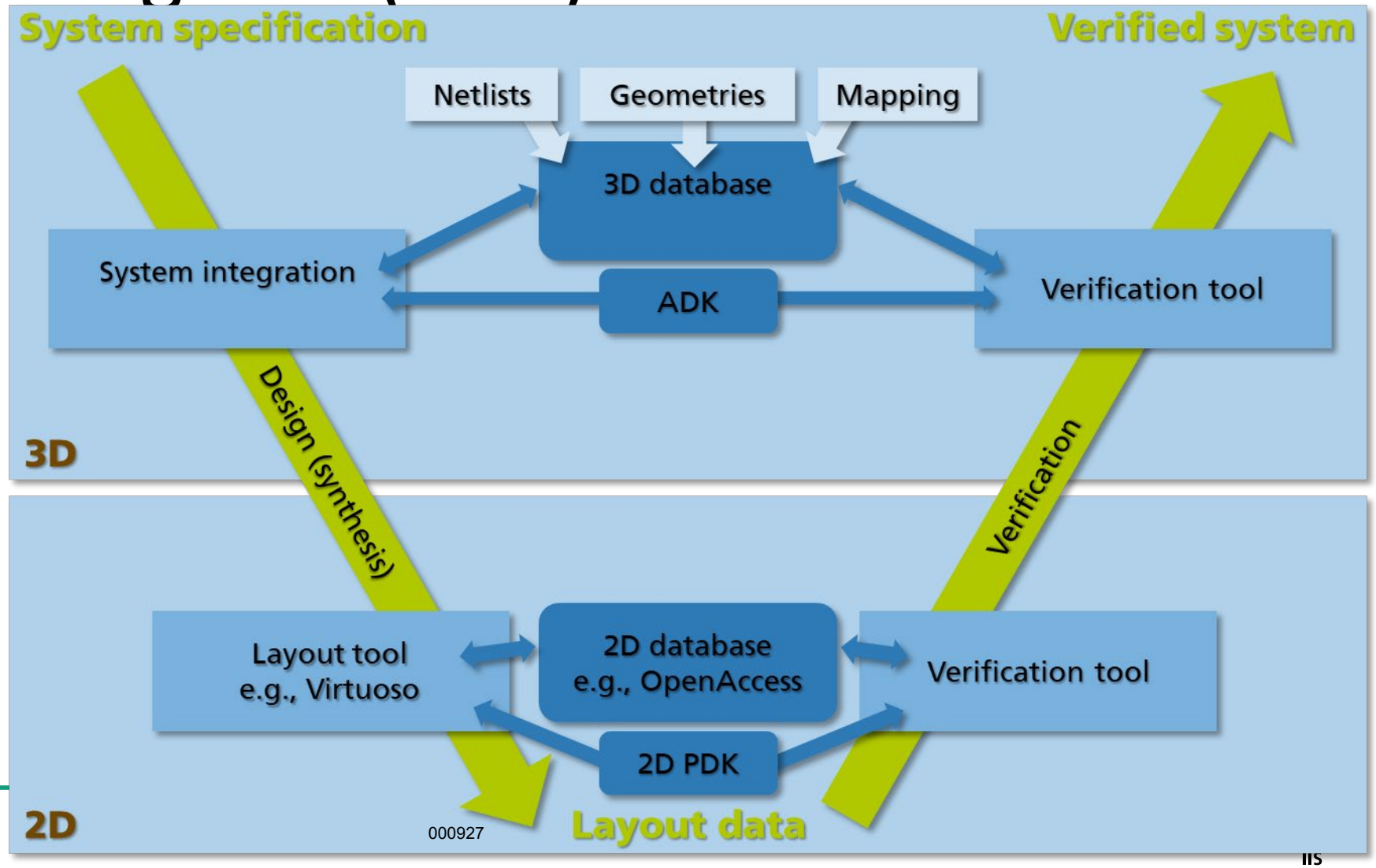
- Chip2Chip
- PCB Assembly
- X-Ray inspection







Design Enablement by Assembly Design Kit (ADK)



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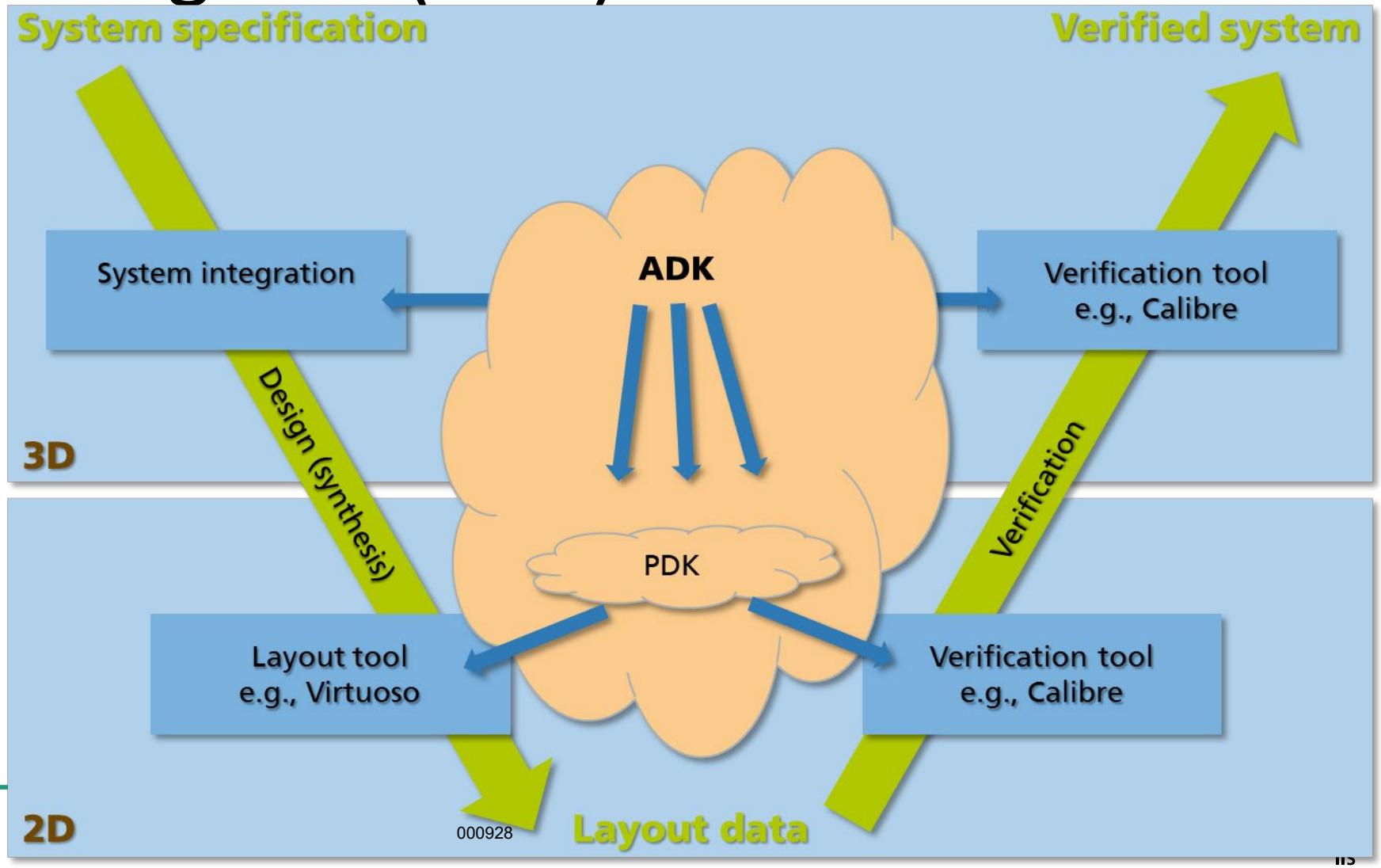
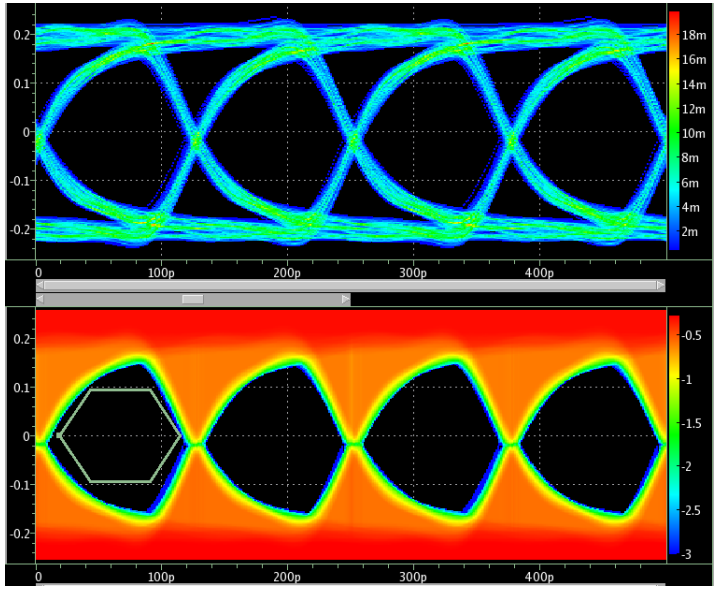
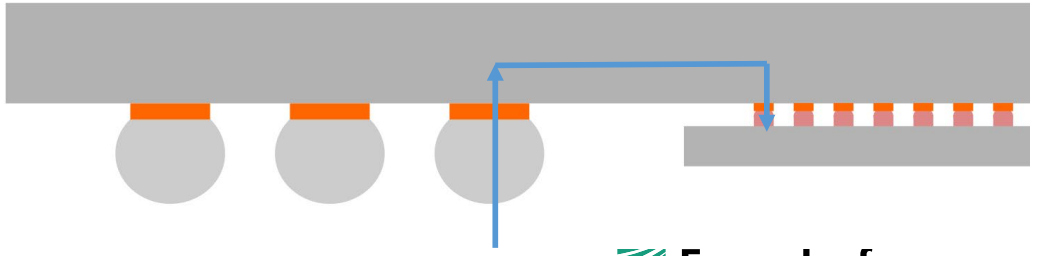


Design Enablement by Assembly Design Kit (ADK)

- DRC and LVS checking
  - Includes assembly
  - Across integration levels
- Enables comprehensive design optimization by
  - Simulation
  - Signal Integrity Analysis
  - Power Integrity Analysis





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Design Enablement by Assembly Design Kit (ADK)

- ESD covers less occupied area
- Reduced drive strength in driver cells – less area and power consumption
- Reduced signal recovery effort on receiver cells – less area and power consumption

Pros and Cons Discussion

- Low cost flip-chip approach
- Very tight connection of ICs, leading to short communication channels
- Requirement of low drive strength leading to smaller driver cells
- Pro for signal integrity, but drawback for power integrity

Summary and Outlook

- Flip-Chip stack using a new assembly approach
- Stack consists of processor and two memory devices
- Assembly process involves die2die stacking using copper pillars and bumping for solder ball assembly

Summary and Outlook

- Design enablement across technologies by ADK
- Coming next:
  - Improving power delivery
  - Adoption to different system components
  - Comprehensive optimization across all components
  - Bring process flow to production mature
  - Investigation of direct bonding techniques

Summary and Outlook

- Acknowledgement
  - Thanks to the colleagues from Fraunhofer IZM and IZM-ASSID for involvement in assembly.

Thank You!

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