



Thin Glass Substrates with Through-Glass Vias

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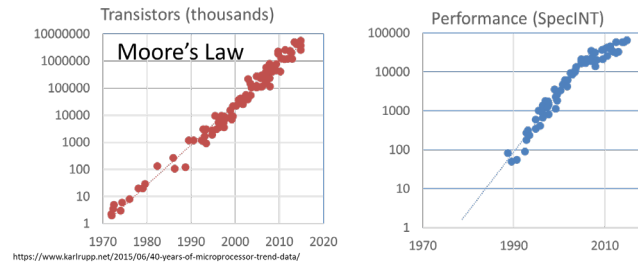
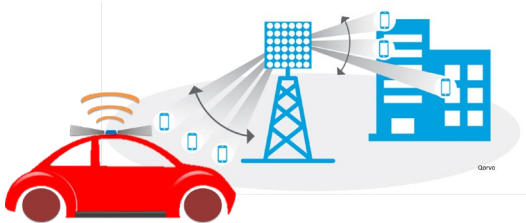
Paul Ballentine, PhD



Outline/Agenda

- Motivation
- Advantages of glass packaging solutions
- Handling challenges
- Solutions to enable volume manufacture
- Summary
- Q & A

Forces of change



IC performance is not
keeping pace with Moore's
Law

- New material solutions are needed to address needs in RF communications
- New packaging solutions are needed to extend industry performance targets

Glass has advantages over other materials

	Good
	Fair
	Poor

Based on chart from Georgia Tech PRC

Characteristic	Ideal property	Materials			
		Glass	Si	Organic	Ceramic
Electrical	- High resistivity - Low loss, low k				
Physical	- Smooth surface - Large area scalability - Ultra thin				
Thermal	High conductivity				
Mechanical	- High strength, modulus - Low warpage				
Chemical	Resistance to process chemistry				
Via and RDL cost	Low cost for both				
Reliability	CTE match to Si and PWB				
Cost/mm ²	@25 um I/O pitch				

- ✓ Low loss
- ✓ CTE match
- ✓ Smooth
- ✓ Cost-effective
- ✓ Scalable

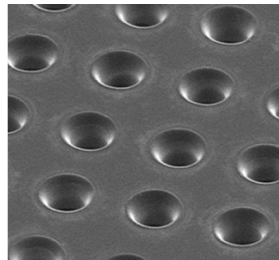
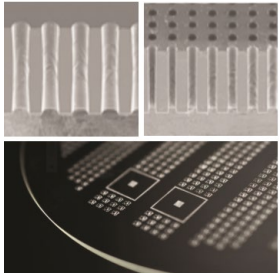
Flat, smooth, and extremely thin glass is available in the market

www.mtixtl.com



Through-glass via (TGV) solutions have been developed

TGV examples (not exhaustive)

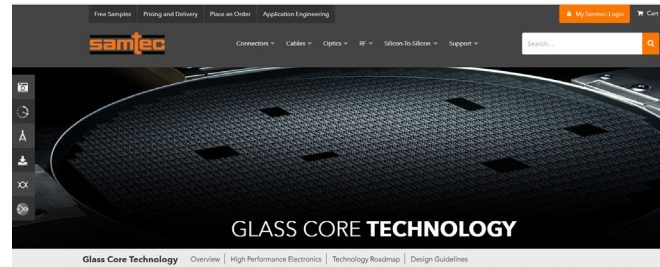


AGC

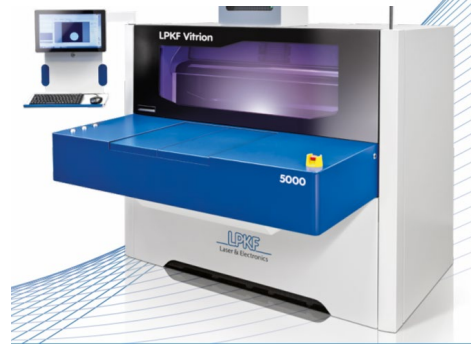
<https://www.agcem.com/index.php/advanced-packaging/3-en-a1-glass-for-tgv-wlp-and-mems>

Schott

https://www.us.schott.com/english/news/press.html?NID=com4588&wss_setorigin=1&wss_iso=en-US

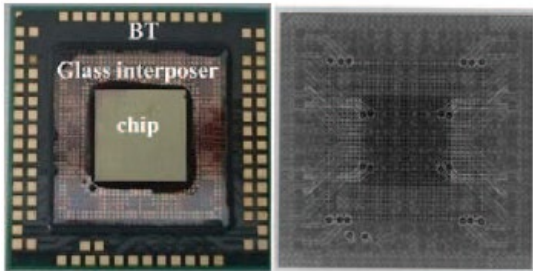


Micromachining of Glass by Laser Induced Deep Etching (LIDE) LPKF Vittron® 5000

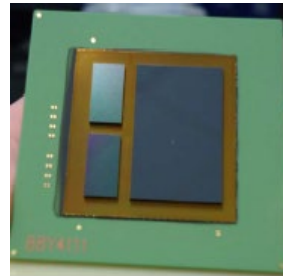


Many demonstrators and products have been made Blind via and through via processes

Interposers



Lee et al.
IMPACT 2016



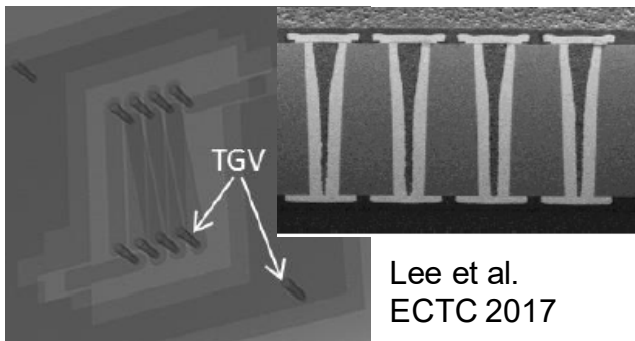
Hedrick et al.
ECTC 2016

MEMs

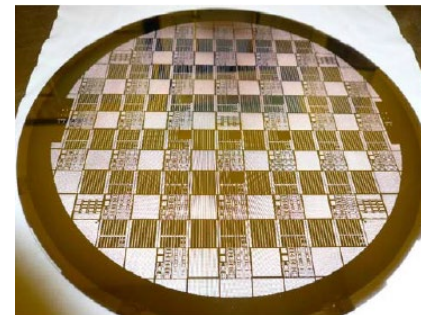


Moran et al.
EuMW 2016

IPD



Lee et al.
ECTC 2017



Kuramochi et al.
ECTC 2014

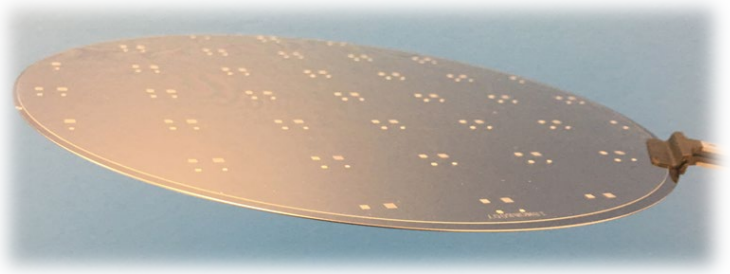


Industry gaps still exist for thin-glass TGV



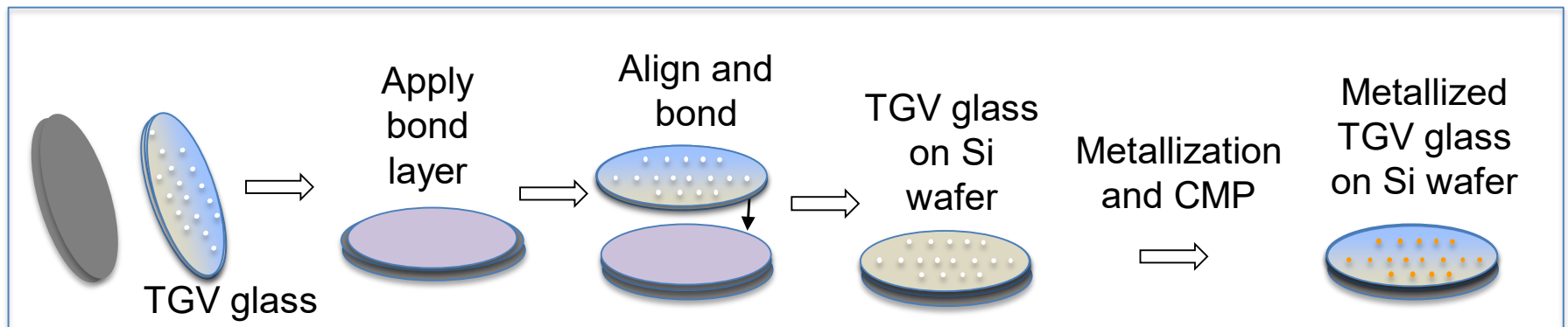


New approach to enable thin glass

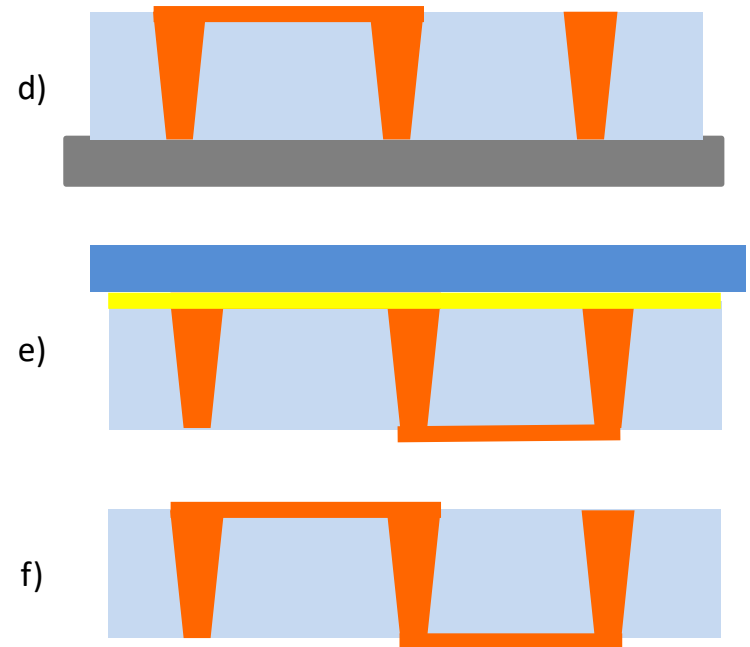
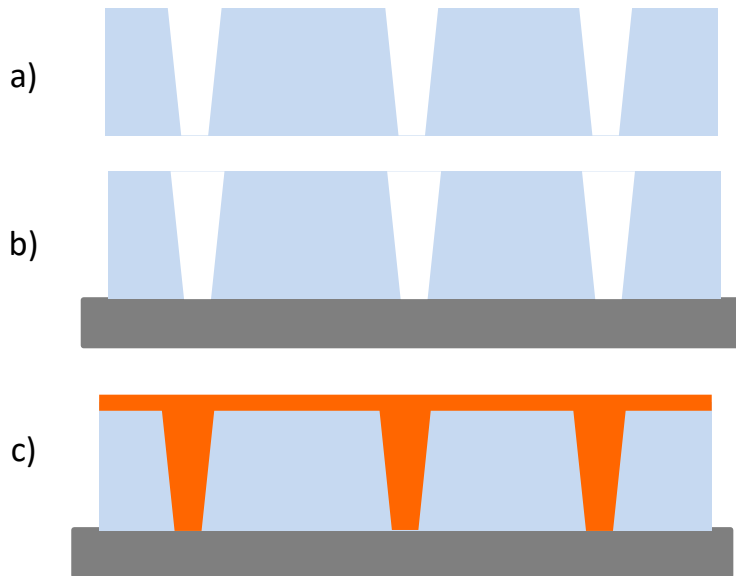


Can be processed like a standard silicon wafer

Mosaic Process Flow

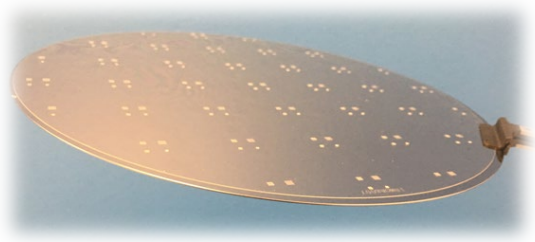


Mosaic Process Flow – Via fill



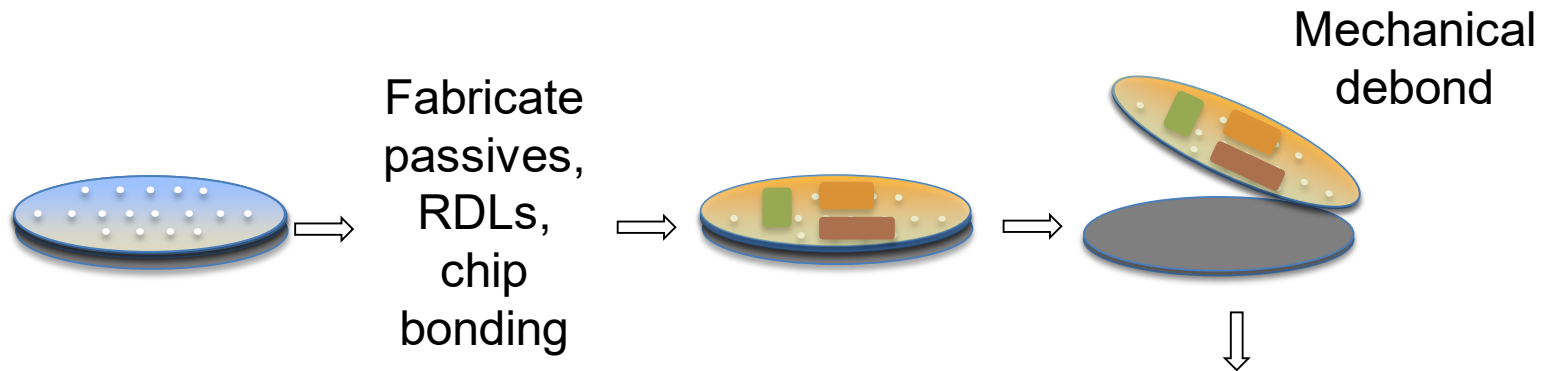


New proprietary bond approach is key

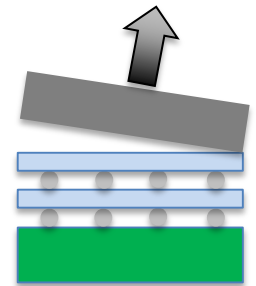


Mechanical de-bond
with low force

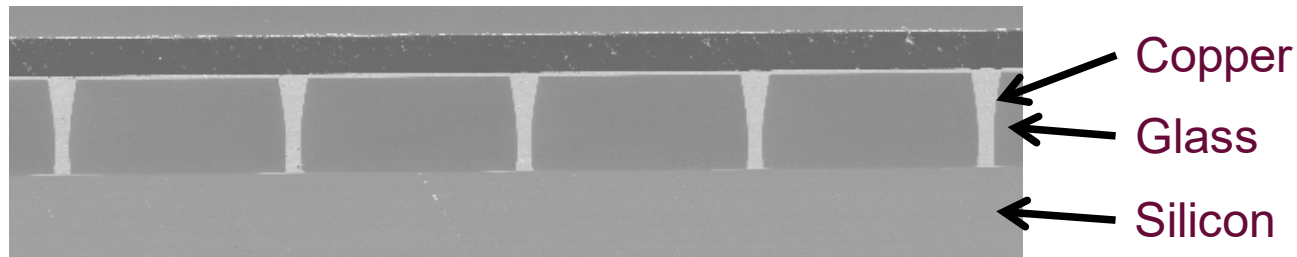
Integrating with downstream processes is straightforward



- Straightforward integration with existing infrastructure (Si fab, TSV processes)
- Mechanical de-bond provides attractive integration approach
- Overall process is scalable

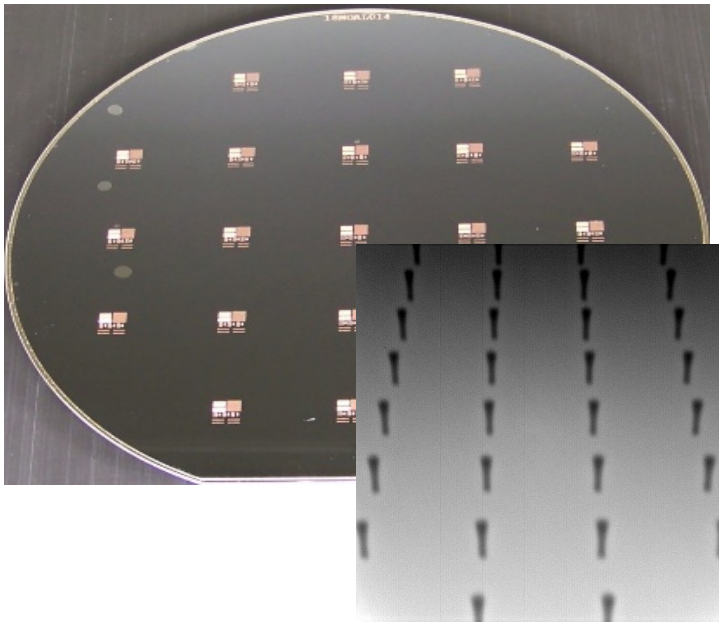


Via Fill: Mosaic TGV plated on Si carrier SG3, 100 um thick



- Achieved void free via fill – important for reliability

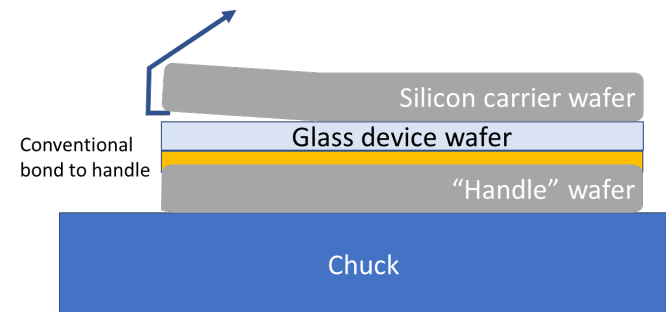
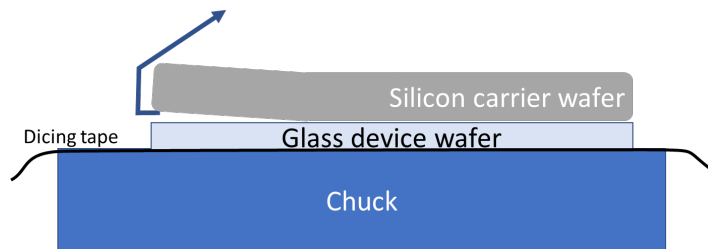
CMP: Wafer after via fill and CMP



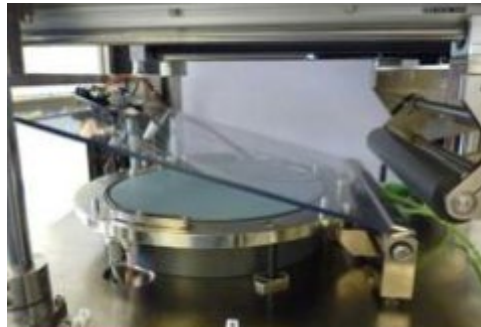
- All wafers successful Cu overburden removal/CMP

Mechanical De-bond Options

- Glass “device” wafer mounted to dicing tape
- Carrier wafer is removed (mechanical deformation is on carrier, not thin glass)



Mosaic Mechanical De-bond Demonstrated with Commercial Tools



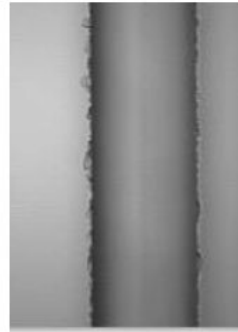
<https://www.slideserve.com/siyavash-tareq/room-temperature-temporary-bonding-debonding-processes-for-2-5-3d-integration>

- Onto dicing tape
- Onto Brewer Science temporary bond to handle





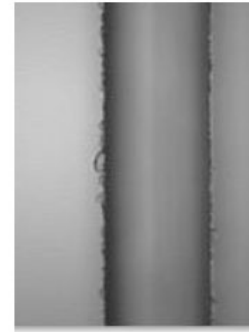
Singulation: Accretech saw dicing SG3 glass



13um



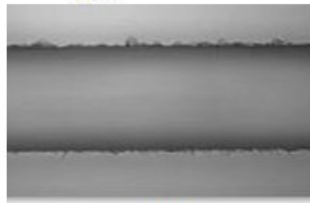
14um



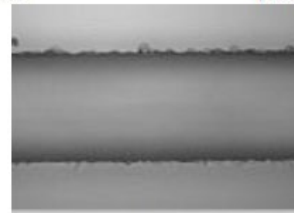
16um



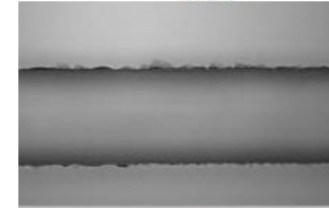
20um



ch1-19um



ch1-19um

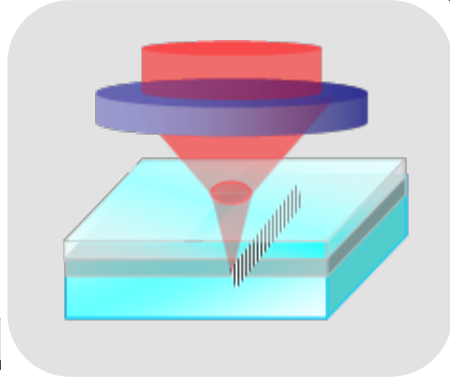


ch1-21um

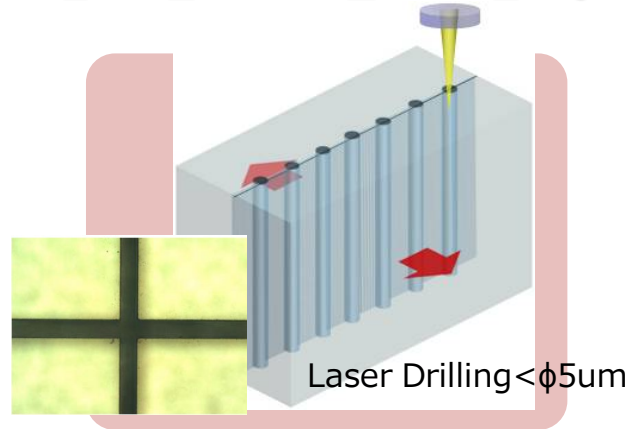
Singulation: Disco saw and laser

Experience with many glass types

Laser Stealth Dicing



Laser Enhanced Ablation Filling



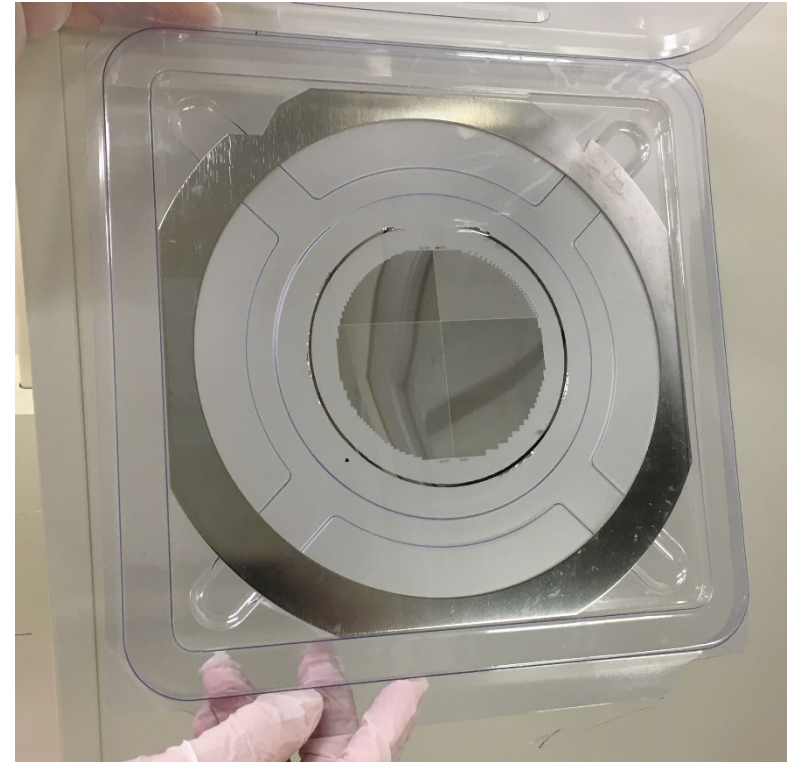
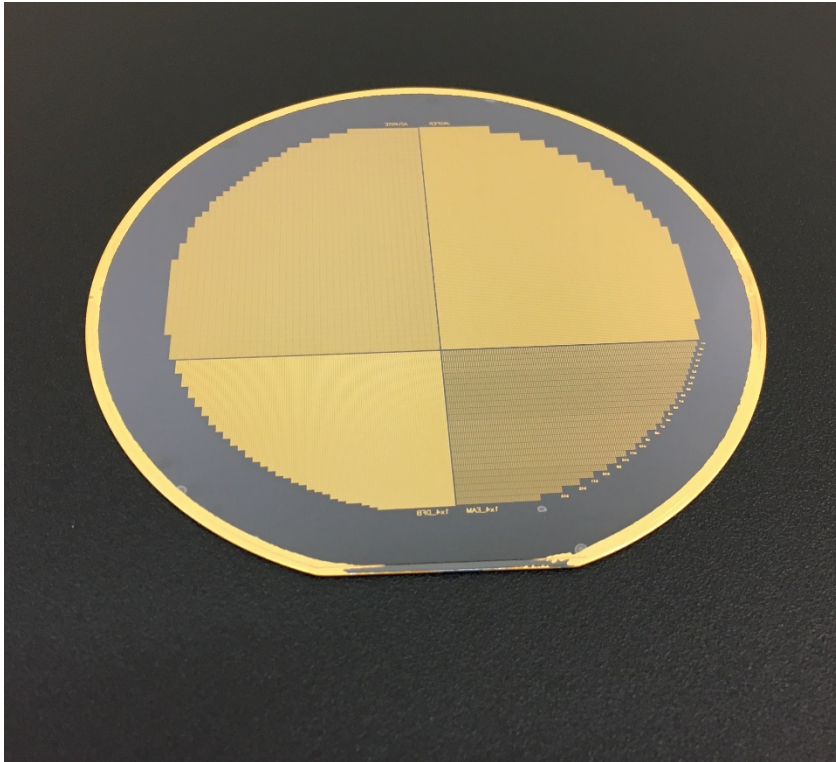
Blade Dicing



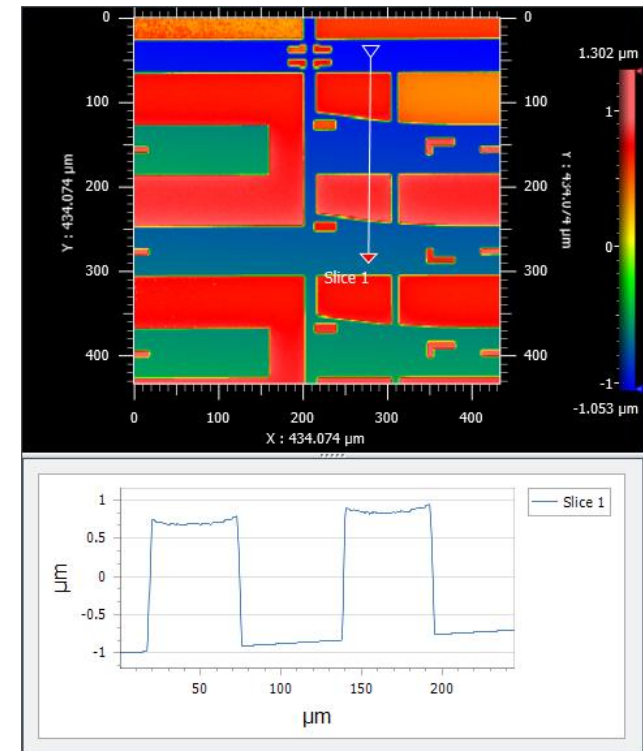
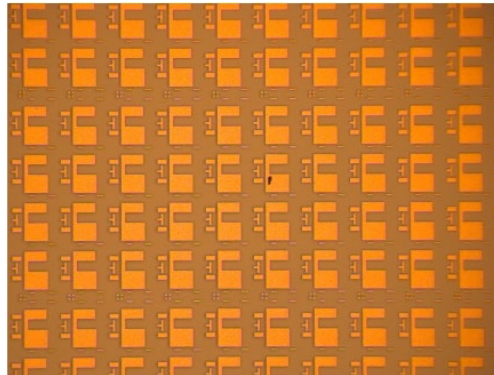
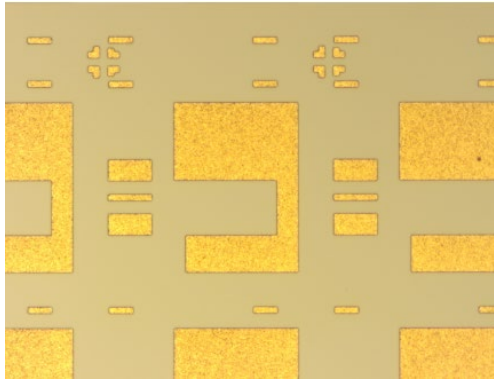
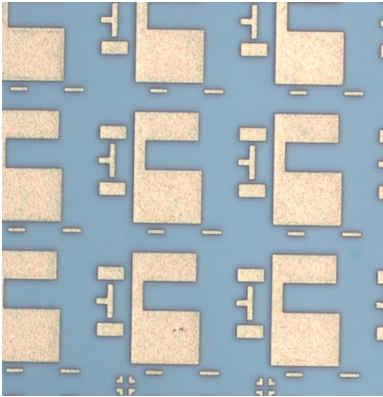
Glass Dicing	Laser Stealth Dicing	LEAF	Blade Dicing
Process Env't	DRY	DRY	WET
Process Speed	FAST	FAST	SLOW
Kerf	NARROW	NARROW	WIDE
Ancillary Process	TAPE EXPAND – THIN BREAKING – THICK	TAPE EXPAND – THIN BREAKING – THICK	NONE

Recent 100x0.1 mm wafer – Plated and de-bonded

All wafers yielded

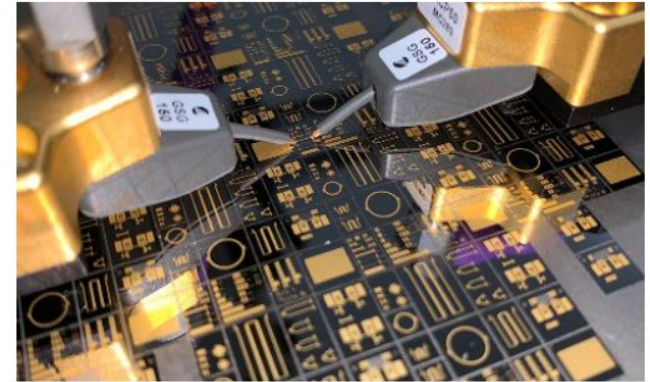
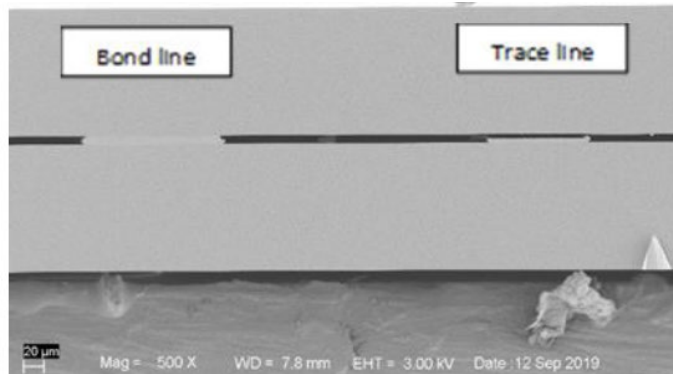


Recent 100x0.1 mm wafer ~2 μm Ni/Au structures



mmW packaging in glass

TEG design, process, test
provided by GE Research



- 0.15 mm thick fused silica
- Thermal compression bond Au

Future implementation

- Multi-layer thin glass with integrated passive devices
- Mosaic handling approach suited for multi-layer structures





March 3 2020 - Press Release



Mosaic Microsystems Summary





Thank You!

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VP Business Development

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