
JCET
LEADING PROVIDER OF ADVANCED SEMICONDUCTOR PACKAGING
AND TEST SERVICES TO GLOBAL CUSTOMERS

Die Backside Metallization for Low Cost High Thermal Package

Nokibul Islam
Director, FAE
JCET Group

Content

- Objective
- How to mitigate heat from package
- Drivers for low cost high thermal package
- Typical assembly process
- Simulation results
- Conclusion

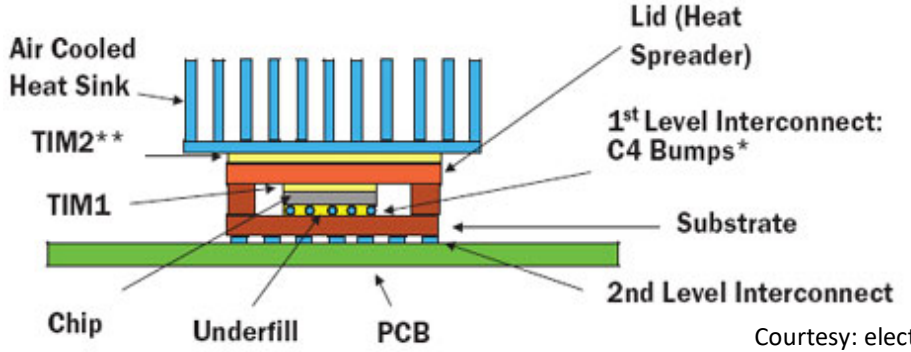
Objective

- Project goal is to qualify a low cost fcCSP solution for high thermal applications
- Define a fully optimized process and BOM to extend the technology to potential other areas

How to mitigate heat from the package

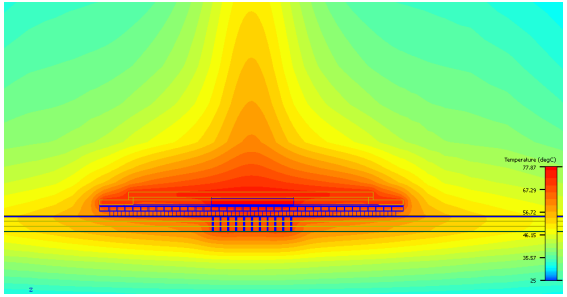
Important parameters for higher thermal performance in a package

1. TIM1 Type (Material and BLT)
2. Lid Design and Material
3. EMC, Underfill type
4. Laminate/LF type
5. Lid Attach Process
6. System type
7. etc



Courtesy: electronic cooling

*Flip Chip Solder bumps
C4 = Controlled Collapse Chip Connection
**TIM = Thermal Interface Material



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Thermal Enhancement Options for fcCSP

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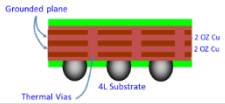
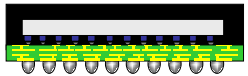
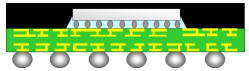
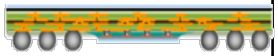
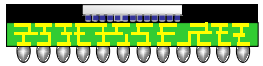
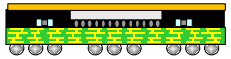
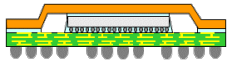
Type	Description	Feature	Pros & Cons	SCK Product (Experience)
Substrate	Thermal vias and Ground Plane (4 layers), thicker Cu (2 oz)		Pros: No additional BOM Cons: Limited thermal improvement	Qualified
Mold Compound	High K EMC mold compound		Pros: No additional BOM Cons : Limited thermal improvement as Silicon is still embedded in Mold	Eval. For FC HVM for WB
Capillary Underfill	High K CUF material		Pros: No additional BOM Cons : Limited thermal improvement	Eval.
Marsupial	Heat dissipation path through PCB		Pros: Direct heat dissipation path from Silicon to PCB. Cu thermal pad for dissipation from the substrate side Cons: Requires special design in PCB	HVM
Exposed Die	Exposing die surface through film assisted molding		Pros: Silicon surface exposed for direct heat transfer Cons: Slower throughput and higher cost than transfer mold	HVM
Exposed Die with flat Heat Spreader	Flat heat spreader with TIM on exposed die		Pros: heat spreader attached to Silicon Cons: High Cost	HVM
Exposed die with hat type	Hat Type heat spreader with CUF based fcFBGA (no mold)		Pros: high thermal performance heat spreader design Cons : Cost, requires larger body size	HVM

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Thin fcCSP Molded Package

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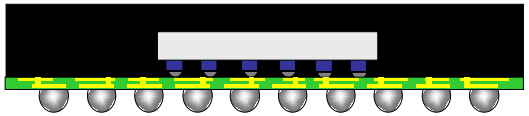
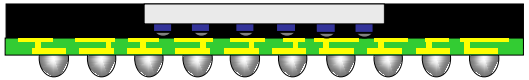
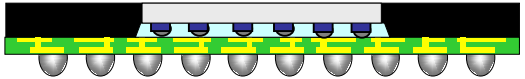


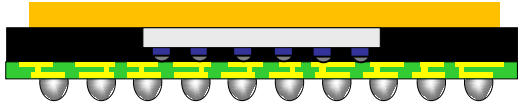
Over molded package



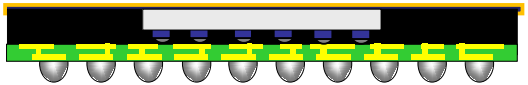
Exposed die molded package



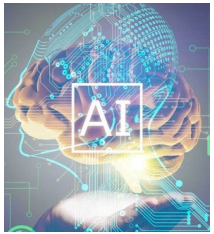
Exposed die molded w/ CUF package

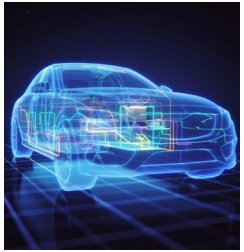


Exposed die molded package with lid



Exposed die molded package
with backside metallization





Key Applications:

Mobile

Computing (CCM, Storage)

AI

Automotive

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Thermal Performance Improvement

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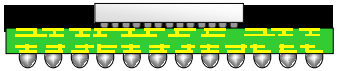
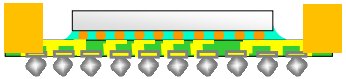
Thermal Resistance Comparison per package type

- Package fcFBGA 12x12 127LD
- Device AP / 3.9x4.2
- Bump Pitch 150/180um

#	Options	Package	Est Rjc on JEDEC 4L PCB	Remark
A	Mold with Exposed Die with MUF		0.07C/W	HVM
B	Bare die with CUF w/ stiffener ring		0.07C/W	HVM
C	Bare die on ball side with CUF, solder interface, 90% Cu top layer.		11.0C/W	HVM

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Thermal Performance Improvement

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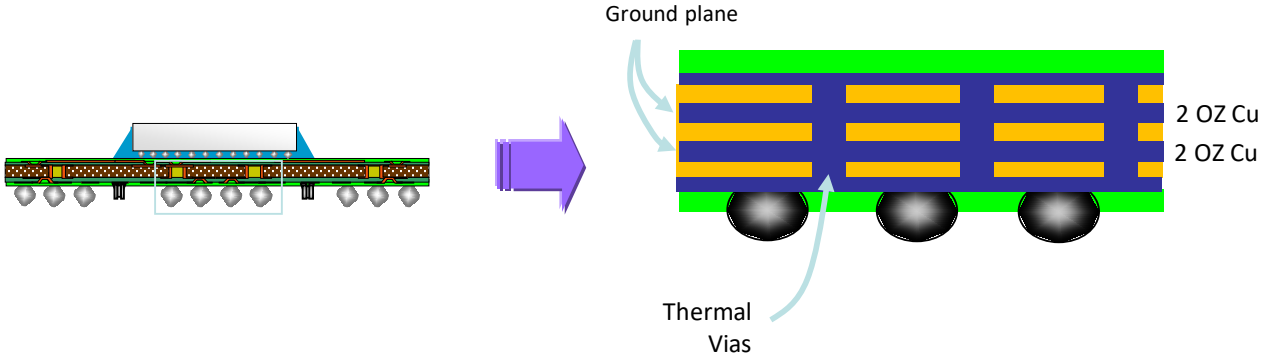
Thermal Via and GND Plane



- Laminate has four or more layers, including power and ground layers, is used as the package substrate for BGAs to ensure satisfactory electrical characteristics.
- The use of a 4-layer structure is to lower the thermal resistance, rather than improve electrical characteristics.
- Thermal Pathway Design with electrical power/ground

Other Ways to Improve Thermal for fcCSP

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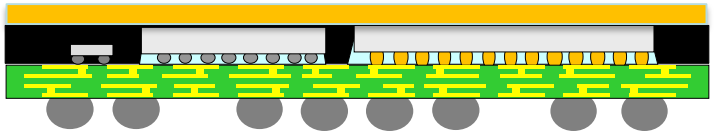
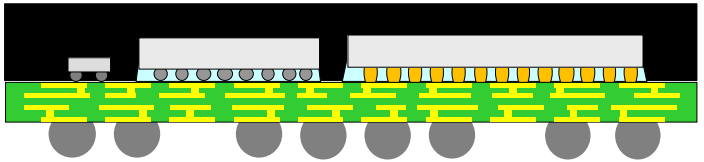
Ambient Temperature (°C)				55 °C	Remark
Power				Total 5W (2.5 W per each die)	
Classification		EMC	*Mold clearance	$Q_{JC\text{-}max}$ (°C/W)	
1	Overmold	0.9W/mK	0.18mm	5.88	
2	Exposed + heat spreader	0.9W/mK	NA	1.46	POR
3	Overmold	3.0W/mK	0.18mm	2.29	
4	Overmold	4.0W/mK	0.18mm	1.82	
5	Overmold	4.0W/mK	0.15mm	**1.61**	Proposal

* Mold clearance is distance between die surface and mold cap surface.



Exposed die MUF + H/S



Overmold Package

Body size: 9X9mm
Die size: 3.2X3.9 and 3.3X5.8mm
Die thickness: 0.2mm
Mold cap thickness: 0.26mm
Substrate thickness: 0.14mm (2L)
Ball pitch: 0.8mm

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EMI Shielding Technology

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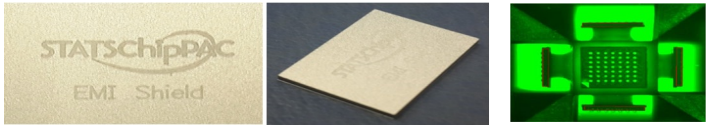
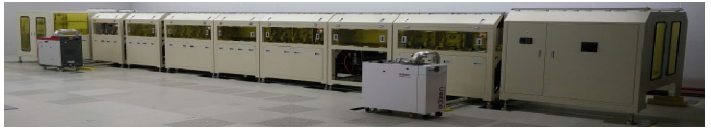
- **Conformal Shielding Overview**
  - Fully automatic In-line batch type sputtering system
  - Package availability : 3x3mm – 35x35mm (Singulated BGA and LGA)
  - Shielding material: SUS-Cu-SUS

FBGA-SiP-ES (Passives+WLCSP or FC)

FLGA-SiP-ES (Passives+FC+WB)





- **Conformal Shielding Capabilities**
  - **Any BGA or LGA package**
  - Fine pitch BGA capability
  - 6-side vision inspection to inspect sputtering quality (4 side wall + Top/BTM)
  - Thickness Aspect Ratio: >40% step coverage btwn Top and Side Wall
  - Metal Peel Test: Min. 3B (EOL & After reliability test)

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EMI Shielding Process

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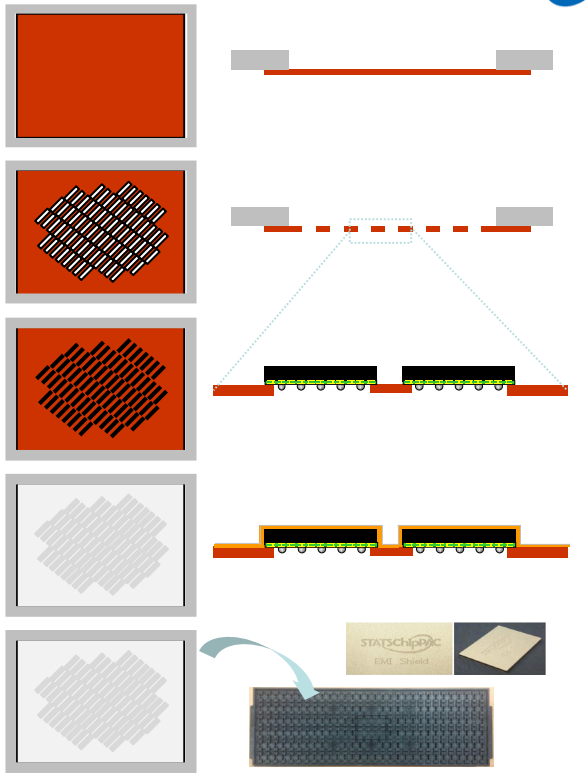
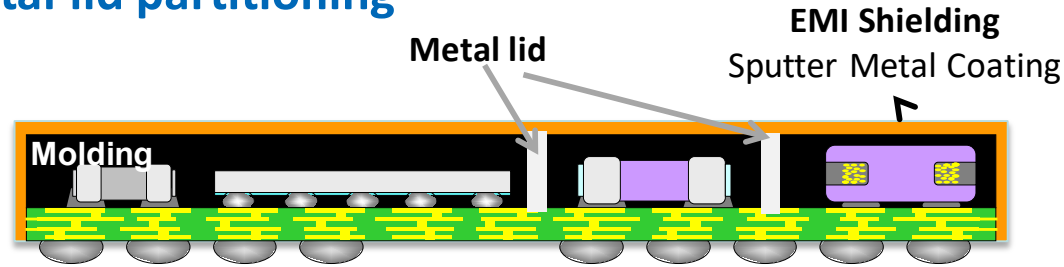
Conformal EMI Shield Process Flow

- **Tape mounting process**
  - PI film lamination on metal frame
- **Laser cutting process**
  - Cavity formation on film to avoid bottom over sputtering
- **Package loading process**
  - Module loading on film cavity
- **Sputtering process**
  - Metal deposition on module & PI film
- **Package unloading process**
  - Module unloading to JEDEC tray

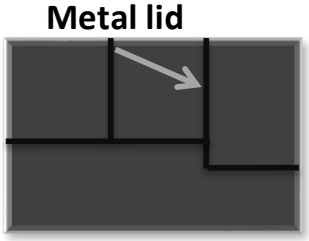


Compartmental Shielding (Alternate)

Metal lid partitioning



Cross-section view



Top view

Various metal lid can be formed less 0.1~0.05mm thick

- Low cost solution than laser trench and fill concept
- Better for thermal

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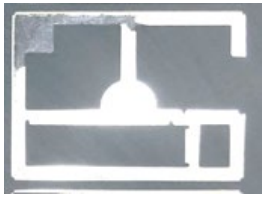
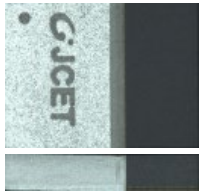
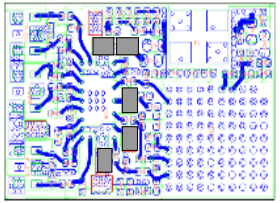
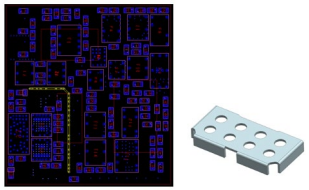
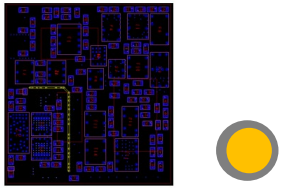
Compartmental Shielding (Alternate)

Option #	Metal Frame	Trench + Ag Epoxy	Metal Chip	Metal Can	Cu Core Ball
Key design					
Structure					
Pros	High Shield effectiveness Medium Cost	Proven Process High Shield effectiveness	Proven Process Component (C0201) equiv. cost Top Side	Utilize SMT process	Utilize SBM process Btm Side
Cons	Design limitation Metal frame supply chain	Design limitation High cost	Design limitation Shield effectiveness	Design limitation	Design limitation
Status	Qual	HVM	HVM	Design review	Design review

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Die Backside Metallization Process Flow

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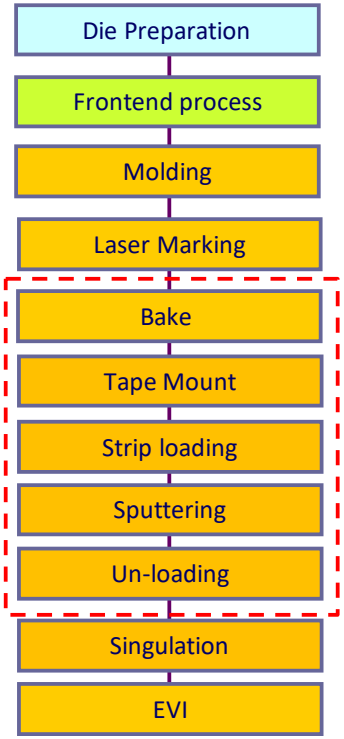
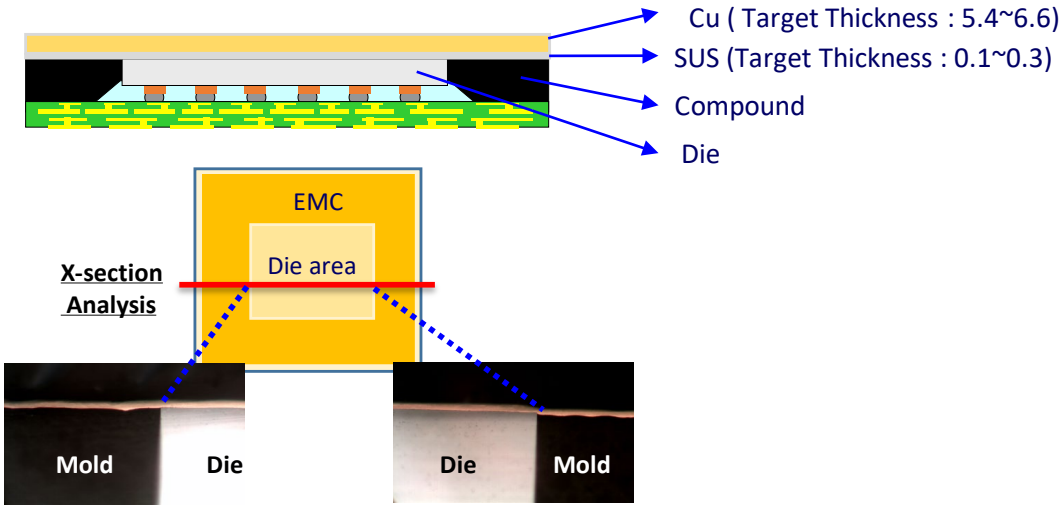
Process flow and Structure



PKG metallization Process flow

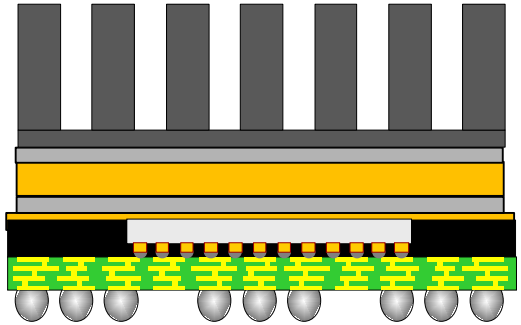


- Key Process Check items
  - ✓ SUS/Cu Thickness measurement
  - ✓ Peeling test to confirm adhesion strength

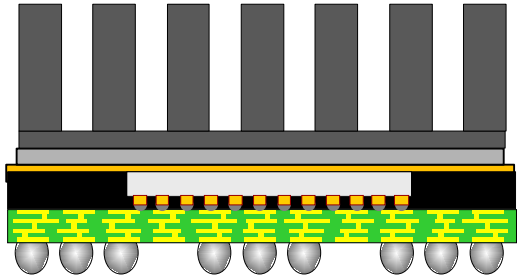
000899

Thermal Simulation Results

Ambient Temperature (°C)			25 °C			
Power			1 W			
2m/s airflow			$T_{J\text{-}max}$	T_T	T_B	Q_{JA}
Package type	TIM1	TIM2	(°C)	(°C)	(°C)	(°C/W)
BSM with lid	Solder	Solder	27.93	27.91	27.26	2.93
BSM no lid	X	Solder	27.97	27.96	27.27	2.97



Backside metal package with solder TIM, Lid, and Heatsink



Backside metal package with solder TIM, and Heatsink

No additional heatspreader is needed with BSM package
BSM is very cheap and robust solution for fcCSP

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FC Thermal Solution

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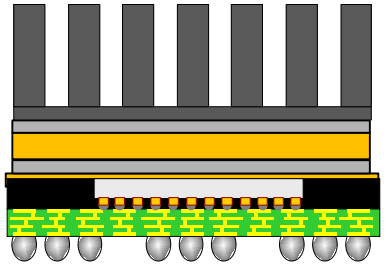
Thermal Simulation for Exposed Die fcCSP-H, BSM

Package / Device	
Package Type	ED fcFBGA-H
Package Size	17x17mm
Die Size	10X10 mm
Die Thickness	200um
TIM thickness	60um
TIM material	Std and solder based
Sputtering thickness	6 um

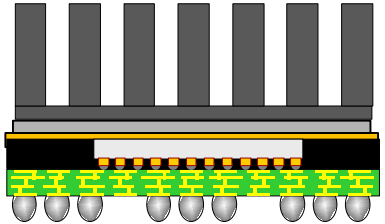
Substrate	
Core Thickness	200um T
Layer Count	4Layers
Total Thickness	400um

17x17x23mm (7pins) HeatSink Applied
Forced air 2m/sec
JEDEC board (4L) Applied

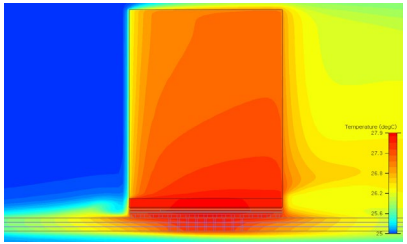
Ambient Temperature (°C)				25 °C			
Power				1 W			
2m/s airflow				$T_{J\text{-}max}$	T_T	T_B	Q_{JA}
LEG #	PKG type	TIM1	TIM2	(°C)	(°C)	(°C)	**(°C/W)**
LEG#1	EDfcBGA-H	Typical TIM	Typical TIM	28.21	27.98	27.36	**3.21**
LEG#2	EDfcBGA-H w/ Sputter	Solder TIM	Solder TIM	27.93	27.91	27.26	**2.93**
LEG#3	EDfcBGA	X	Typical TIM	28.15	28.14	27.34	**3.15**
LEG#4	**EDfcBGA w/ Sputter**	X	**Solder TIM**	27.97	27.96	27.27	**2.97**
LEG#5	ED fcBGA-H	Typical TIM	Solder TIM	28.10	27.86	27.31	**3.10**



Leg#2 : Sputtering + Solder TIM w/ HS



Leg#4 : Sputtering + Solder TIM w/o HS



BSM improved thermal resistance by ~9% when use solder TIM

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Thermal Enhancement with BSM

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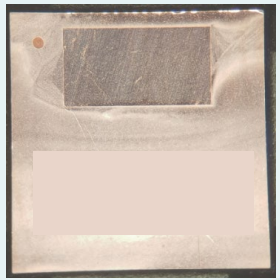
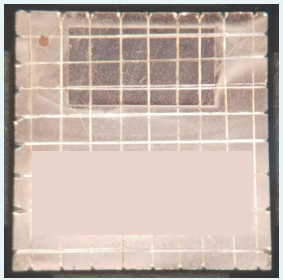
Sputtering thickness Control and Adhesion strength test

SUS/Cu Thickness (XRF analysis for Cu and SUS thickness)

Spec.limit (um)	S/S	Avg	Min	Max	Cpk
SUS (0.1~0.3)	5	0.189	0.187	0.194	16.67
Cu (5.4~6.6)	5	5.909	5.827	6.007	6.32

Metal Adhesion Strength (Metal Peeling test)

Item	S/S	Before peeling	After peeling (Spec.: Min. 3B)	
Peeling Test	5unit/ lot		 Pass	4B

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Summary

- Successfully demonstrated the capability of developing and qualifying thin backside metal on flip chip CSP molded package to improve thermal performance, and the same time lower packaging cost.
- EMI shielding process has been used for die backside metallization
- There are various ways to improve thermal performance of fcCSP but BSM appears to be one of the best solution for low power packages
- Extensive reliability tests are conducted to make sure process and packages are robust enough to meet applications criteria
- More characterization and process development is needed to expand the technology to wide range of applications and packaging types

Acknowledgement

Special thanks to our customers, JCET Korea R&D team for their continued guidance in this study. Our sincere gratitude to our suppliers too

THANKS

JIANGSU CHANGJIANG ELECTRONICS TECHNOLOGY CO., LTD