Fluxless Bonding Via In-Situ Oxide Reduction

IMAPs Device Packaging
March 2020
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Kulicke & Soffa®

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Oxide Reduction Bonding For High Performance Applications

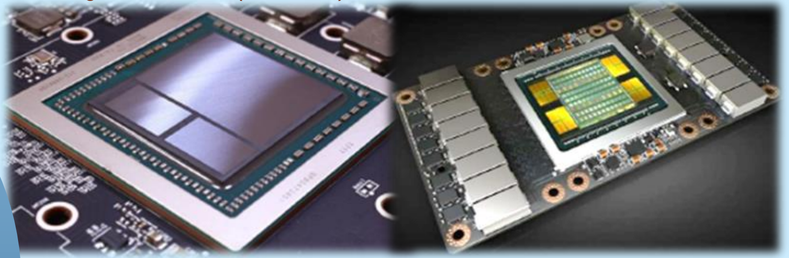
High Performance GPU, CPU, & ASIC with High Performance Memory

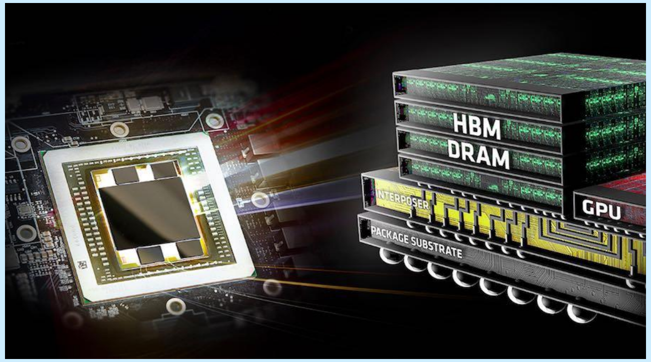
- *Gaming*
- *3D Computer Graphics*
- *Workstation*
- *Cloud Computing*
- *Artificial Intelligence*
- *Autonomous Vehicles*

Target Applications Of Oxide Reduction Bonding

AMD Vega10 with HBM (~500GB/s)

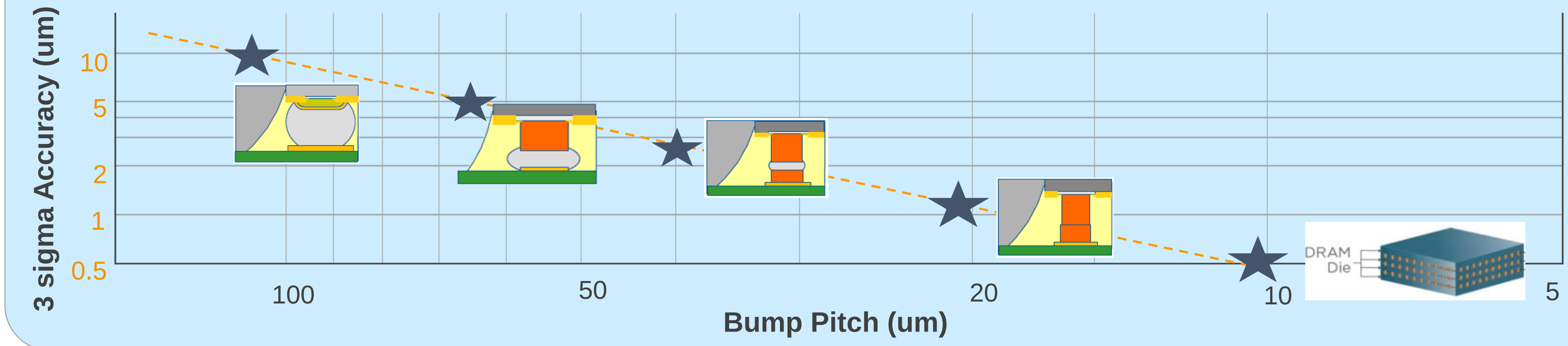
NVIDIA Volta with HBM (~900GB/s)





Sources: nVidia.com, 3Dincites, Micron.com

Flip Chip Package Interconnects



Accuracy Evolution (µm)

High Accuracy Hybrid SMT and FC

High Accuracy Flip Chip

TCB → *Oxide Reduction* → *Direct Hybrid Bonding*

7µm 5µm 3µm 2µm 1µm > 0.5 µm

Source: Yole Developpment

Reference to
- Yole 2.5D / 3D TSV & Wafer-Level Stacking Technology & Market Updates 2019
- Yole Fan-Out Packaging Technologies & Market Trends 2019
- R. Swaminathan, "2D to 3D Architectures Back to the Future", IMAPS 2018 Device Packaging Keynote

Challenges with Fluxed Based TCB

- Fluxing adds TCB process complexity
  - Pre-bonding fluxing step
  - Post-bonding clean-up step
  - Flux fumes clog bond heads requiring daily cleaning
- Challenges
  - Bonding of large chip areas i.e. ≥ 400 mm^2 with high density interconnects
  - Flux clean-up is difficult – can leave residue
  - Underfill will not adhere to regions where flux residue exists
  - Leads to reliability failures with solder shorts

Large Die With Fine Pitch Solution - Oxide Reduction Bonding

Technology node		Critical dimension (nm)								
		130	90	65	45	32	22	14	10	7
Interconnect	Pitch	400	280	200	126	104	88	56	40	28
	Width	200	140	100	63	52	44	28	20	14

ium.com, Cambridge.org

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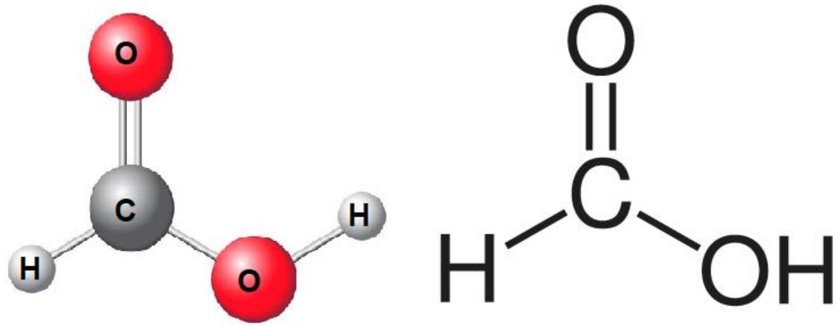
Tin Oxide Reduction via Formic Acid Vapor

Formic acid:



- Molecular formula: HCOOH
- Nitrogen saturation limit: 4.5% at 25 °C
- Sn-formate decomposition rate increases with temperature

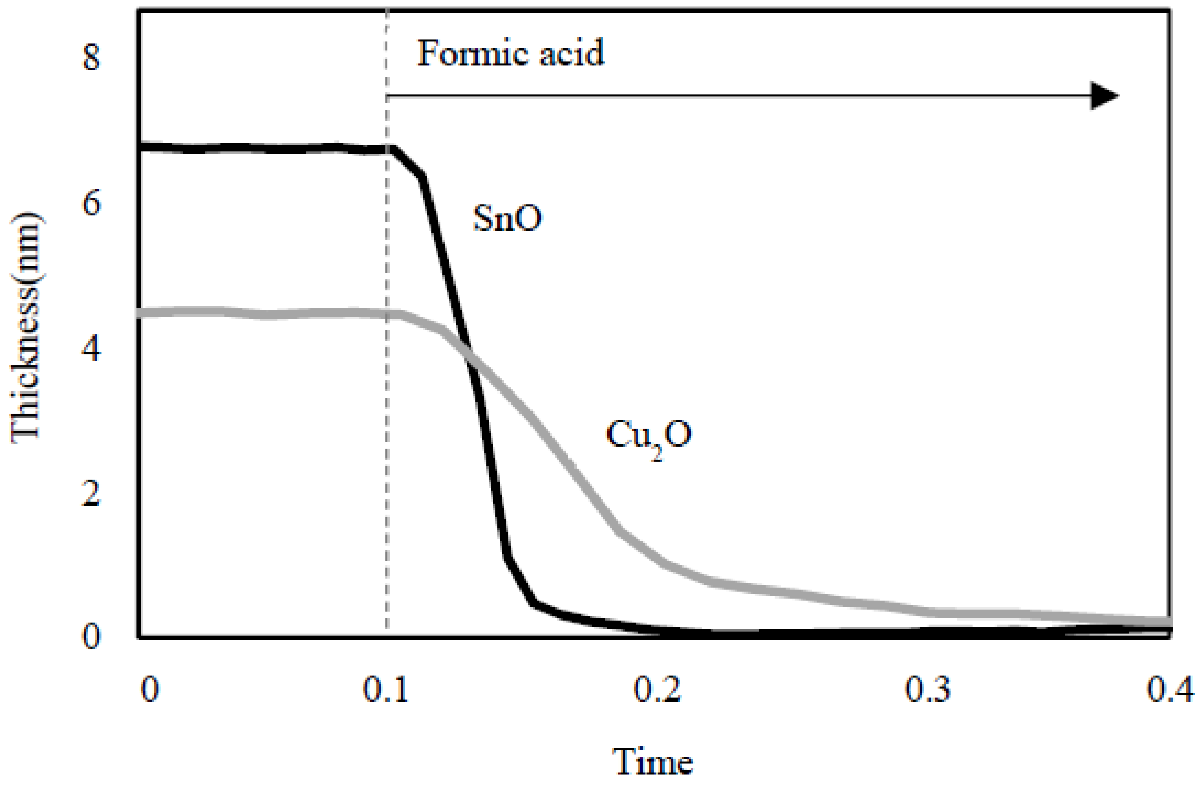
Step 1: Sn formate creation (100 °C < T <150 °C)

$$SnO_{(s)} + 2HCOOH_{(g)} \longrightarrow Sn(COOH)_{2(s)} + H_2O_{(g)}$$

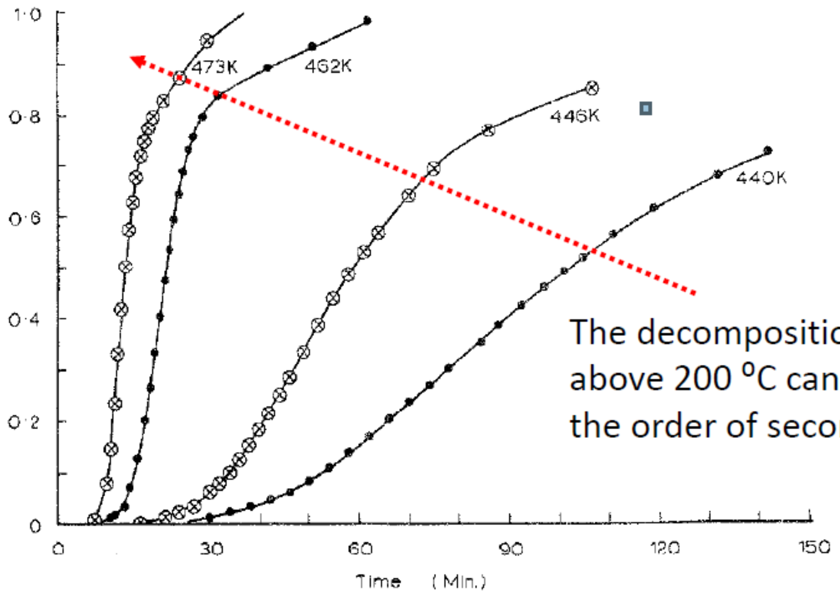
Step 2: Sn formate decomposition (T > 150 °C)

$$Sn(COOH)_{2(s)} \longrightarrow Sn_{(s)} + 2CO_{2(g)} + H_{2(g)}$$

Oxide Reduction via Formic Acid Vapor

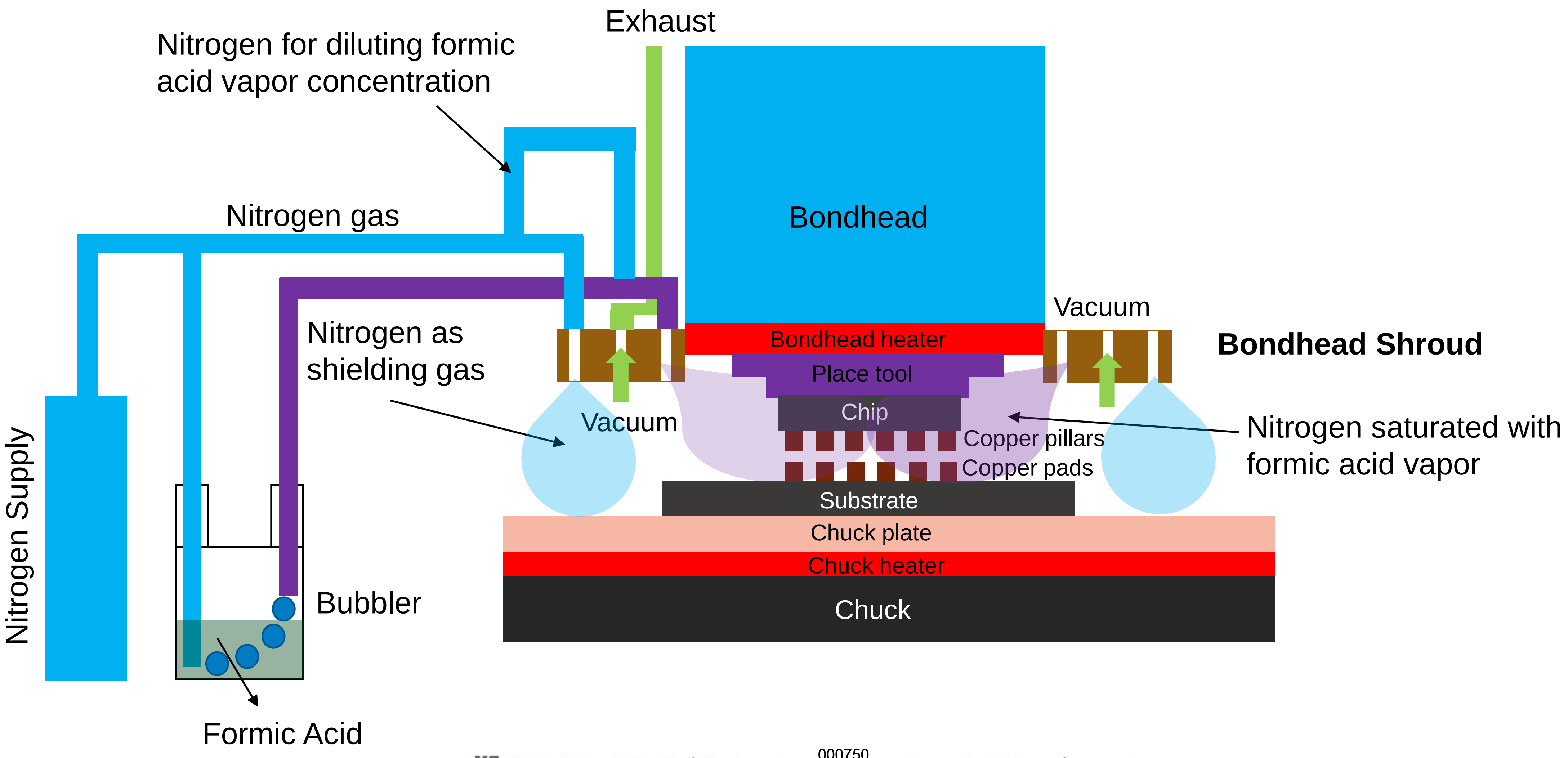


Fractional decomposition (α)-time curves for the isothermal decomposition of Copper (II) Formate

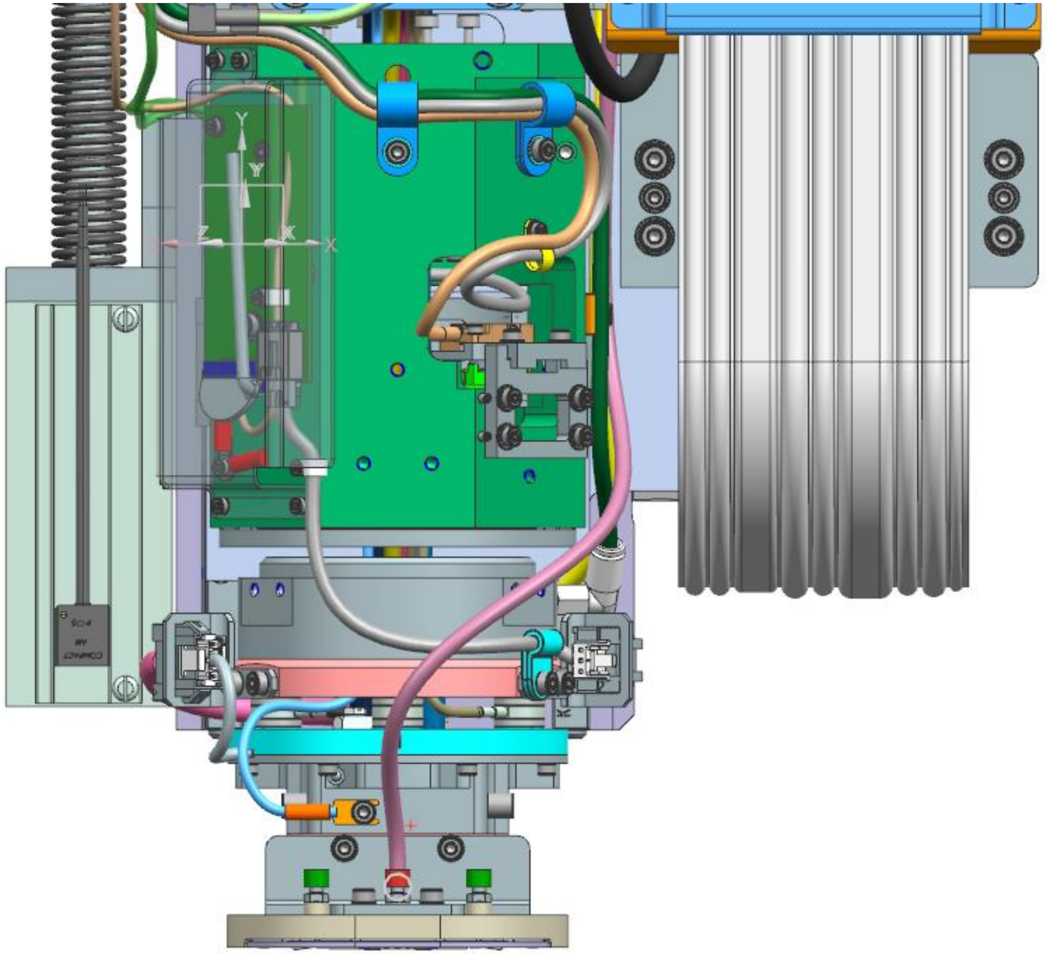


The decomposition rate above 200 ^{o}C can be of the order of seconds

Schematic of Patented Formic Acid Delivery System



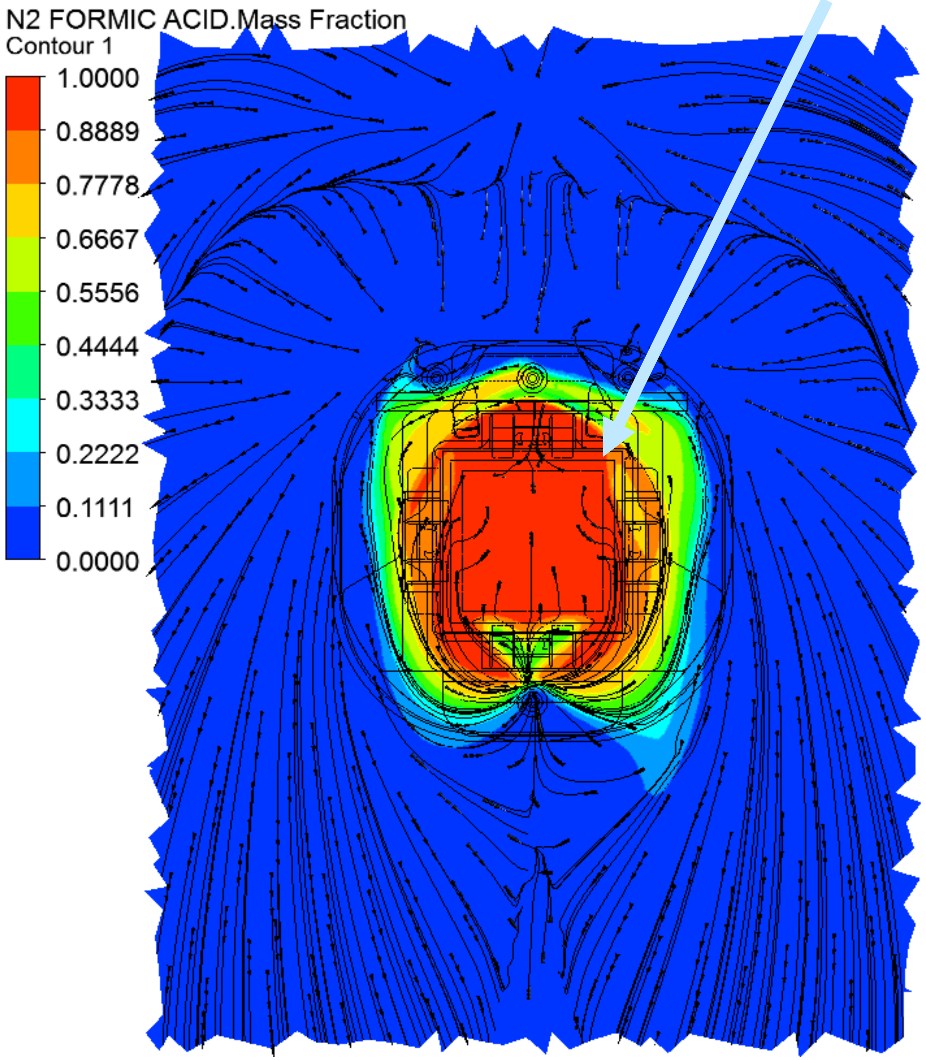
Formic Acid Shroud – Generation 5



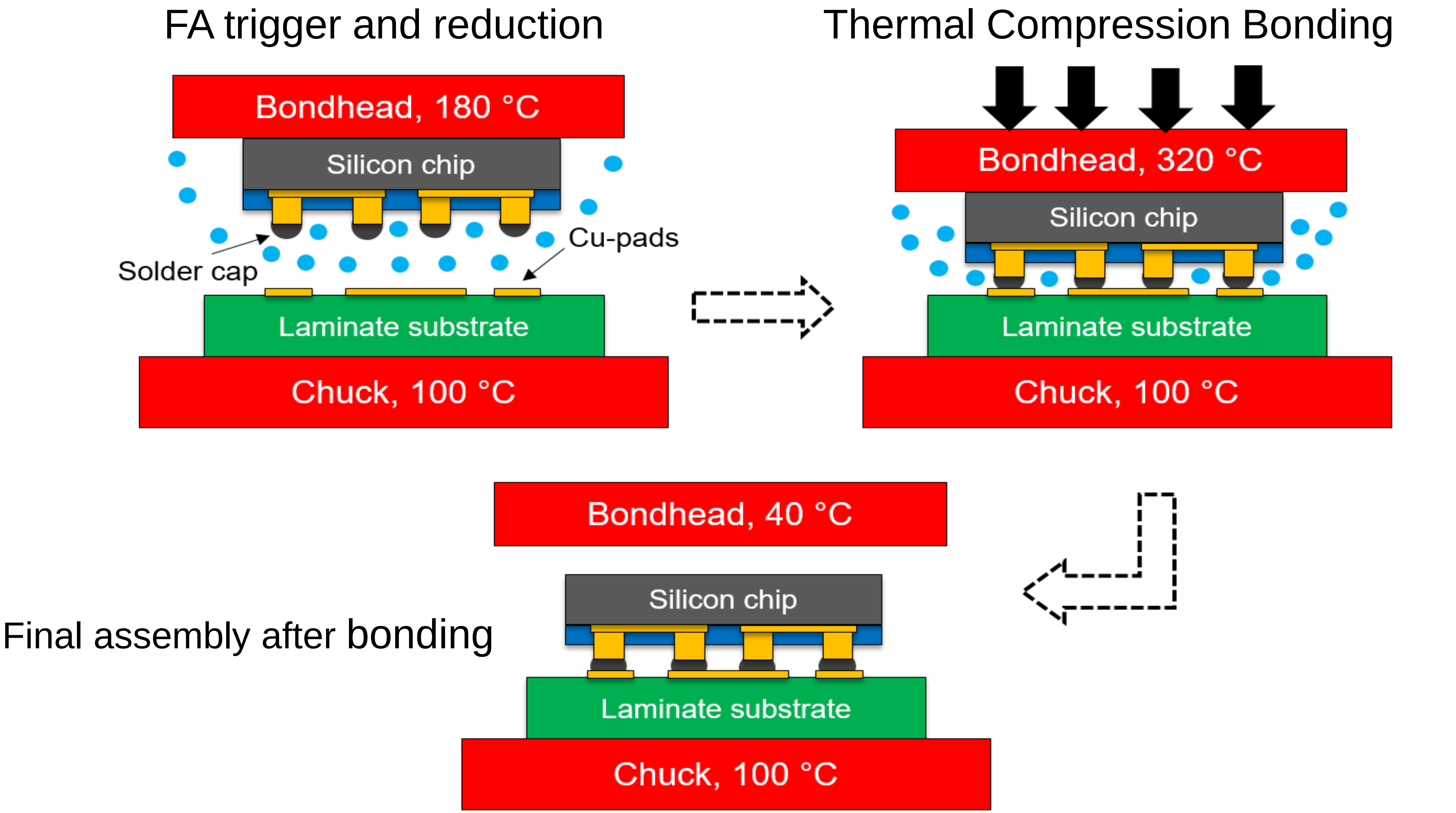
Shroud Design Using CFD Simulation

- Bondhead shroud design using CFD simulations
  - Maximize saturated formic acid vapor contents e.g. > 95 %
  - Minimize oxygen contents e.g. < 1%
  - Optimize gas flows i.e. shielding gas and vacuum to eliminate escape of FA vapor into main machine environment

32 mm X 28 mm
Die on tool



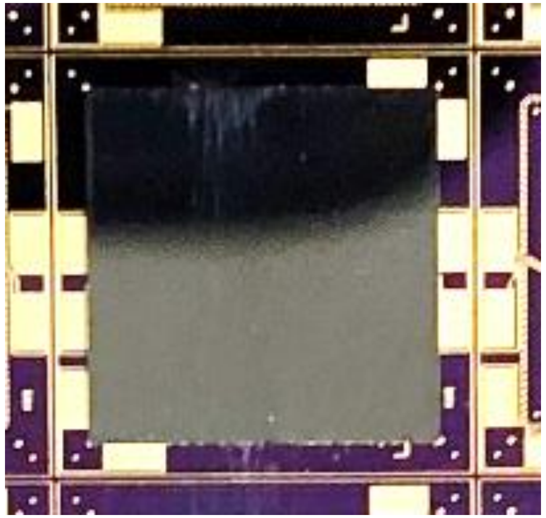
In-Situ Formic Acid TCB Process Flow

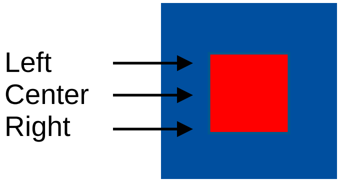


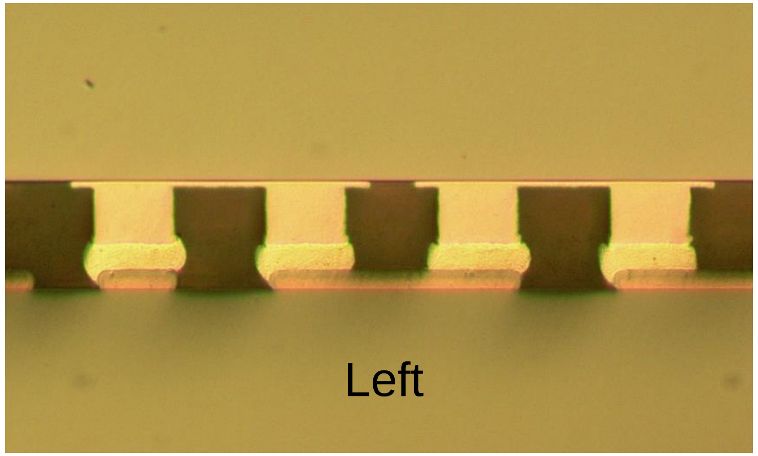
Fluxless Bonding

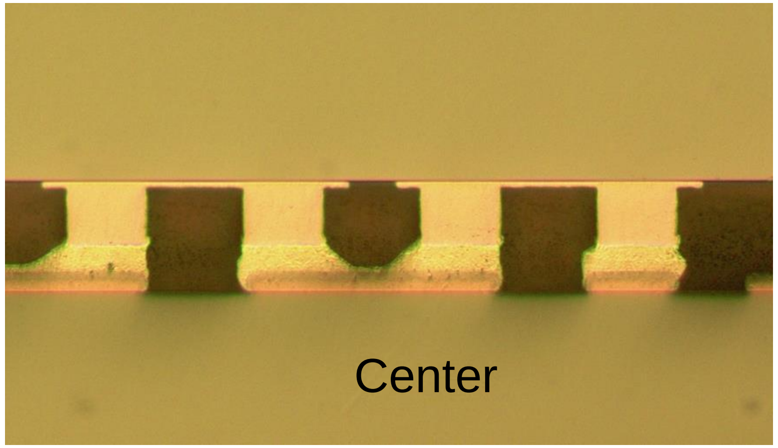
- Chip size 20 X 20 mm
- Pillar diameter: 35 microns
- Pillar pitch: 80 microns
- Substrate metallization: Cu/Ni/Au (7.5/2/0.15 microns)
- Solder line thickness: 11 microns

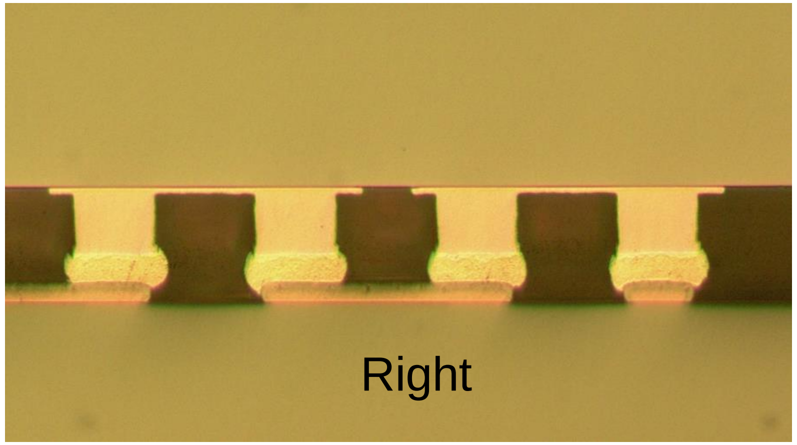
Chip bonded to the substrate using fluxless TCB





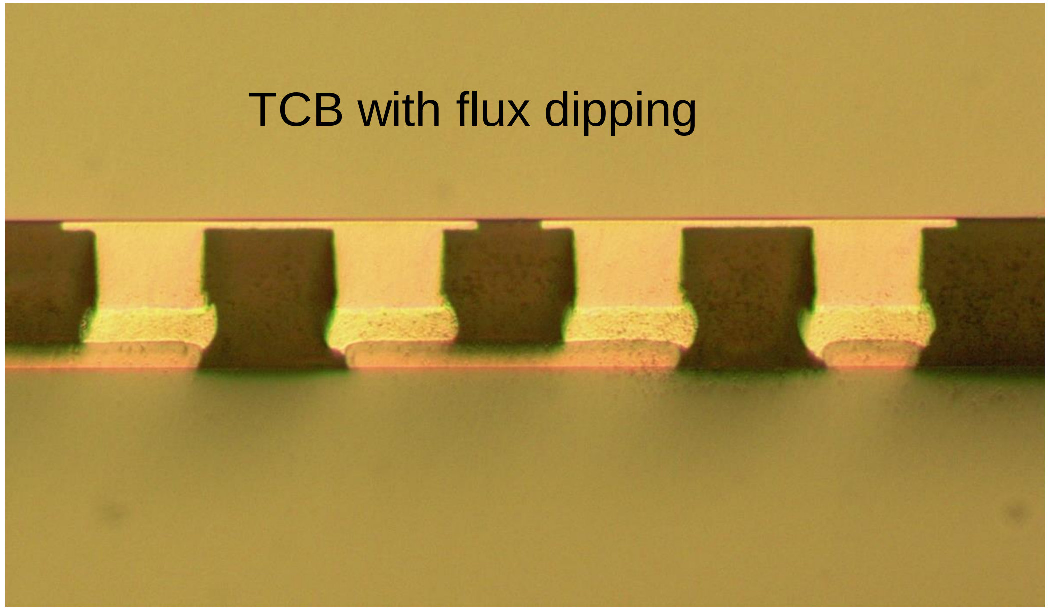


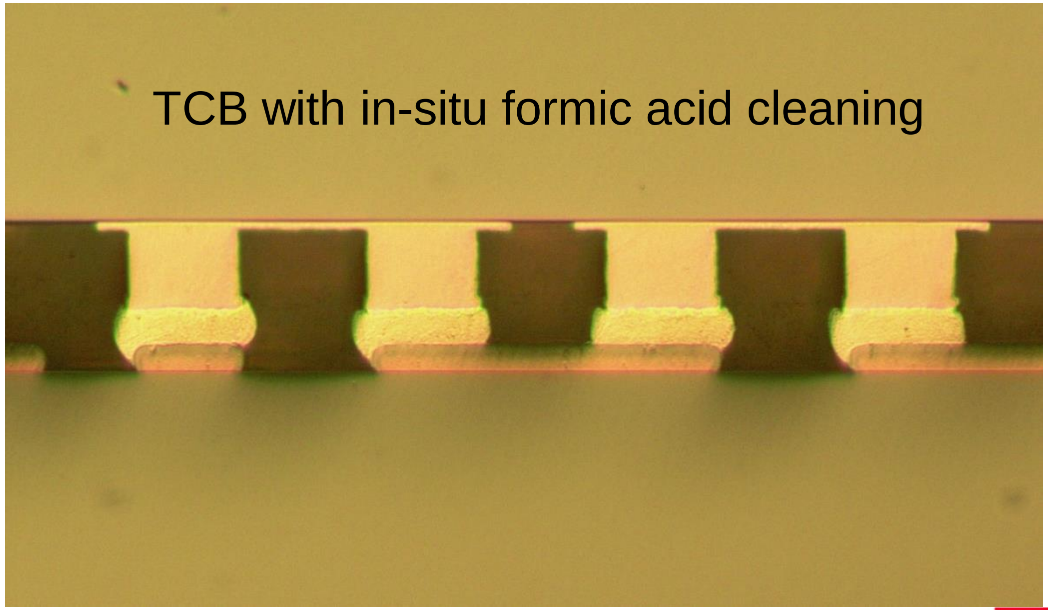




Fluxed vs. Fluxless Bonding

- Bond quality for both dip-fluxed and fluxless TCB was found to be excellent
- Flux-less bonding avoids two critical steps
  - Pre-bond flux dipping
  - Post-bond cleaning





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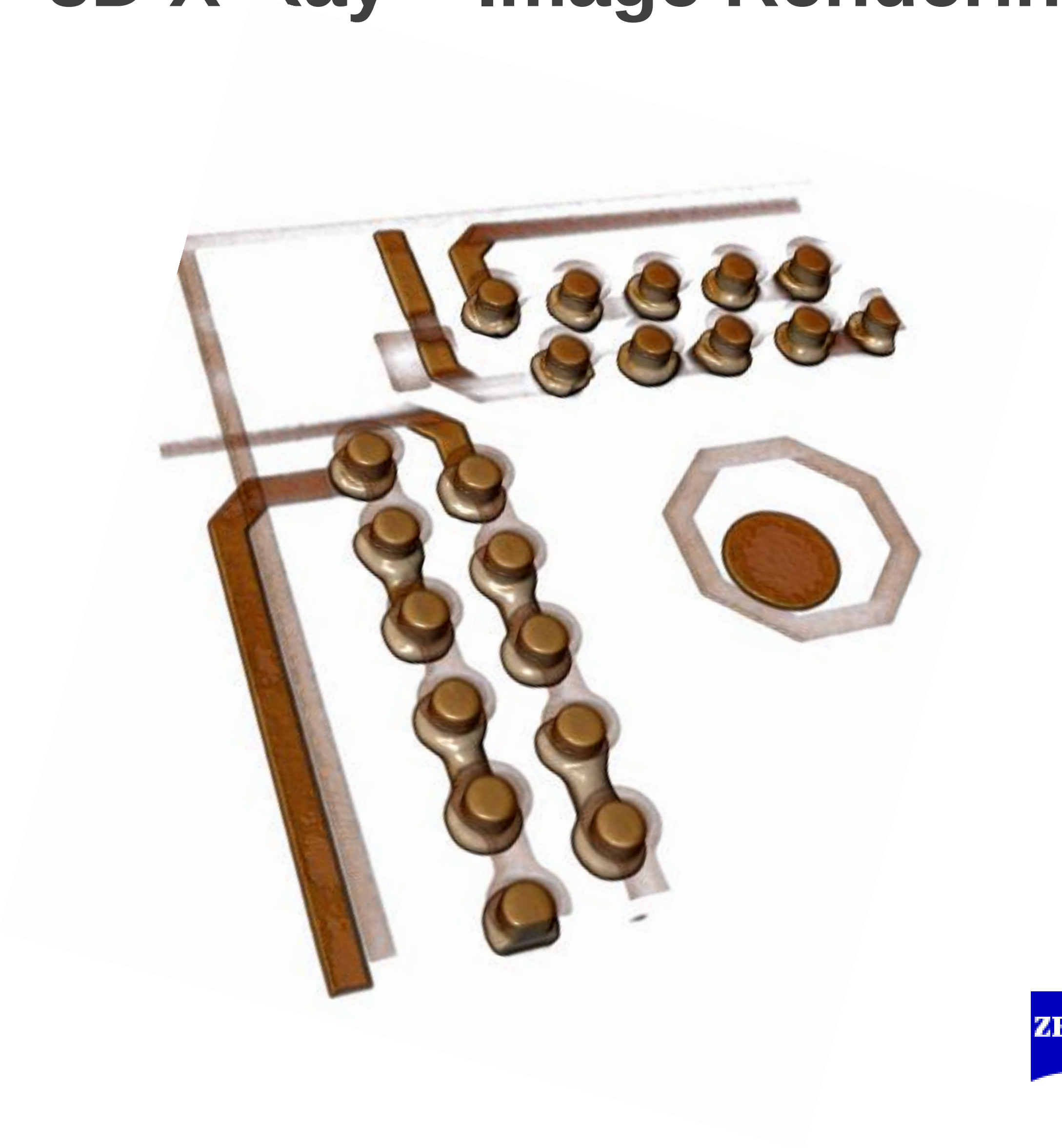
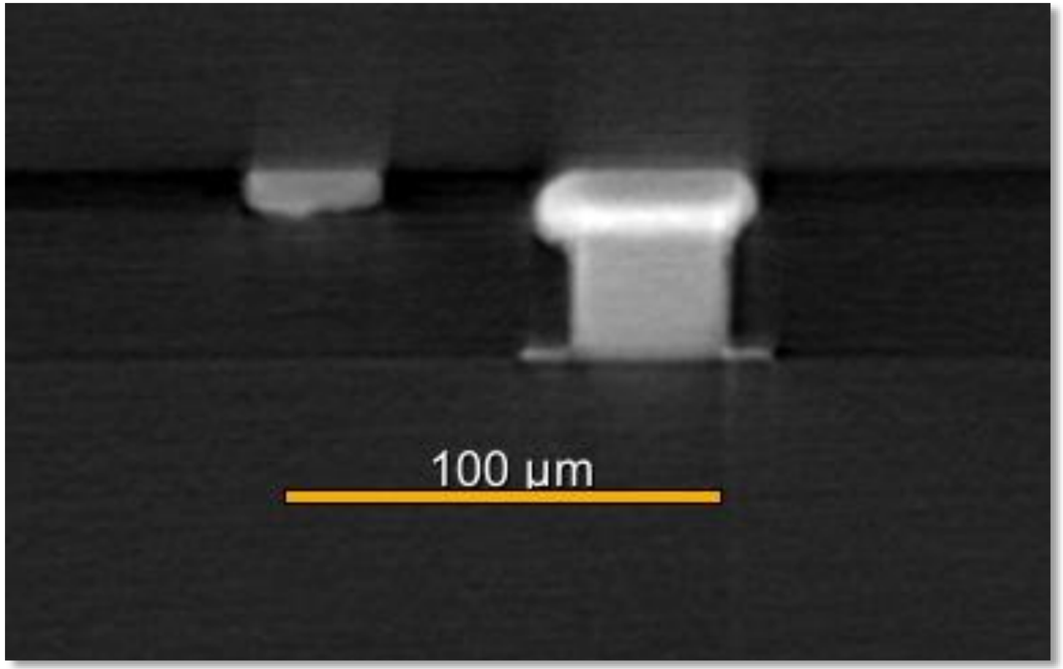
3D X-Ray – Image Rendering and Virtual Slice

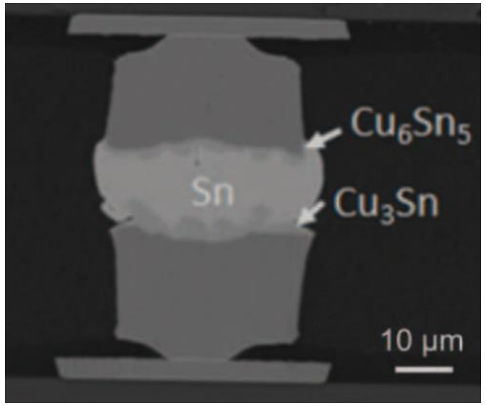




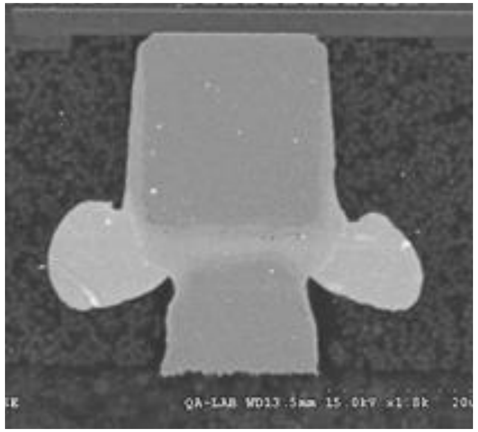
Images courtesy of Zeiss
Xradia 620 Versa tool

Extension of Fluxless Process to Cu-Cu Bonding

- Direct thermo-compression Cu-Cu bonding
    - Allows sub-10 µm interconnect pitch
    - Cu exhibits superior electrical and thermal properties
- Solder for sub-10 µm pitch scaling is challenging
    - Solder extrusion & bridging
    - Brittle intermetallics formation
- Formic acid vapor based copper oxide reduction
    - Reduces copper oxides and allows pure metal contact



Brittle intermetallic formation (Wang et al. ECTC 2016)

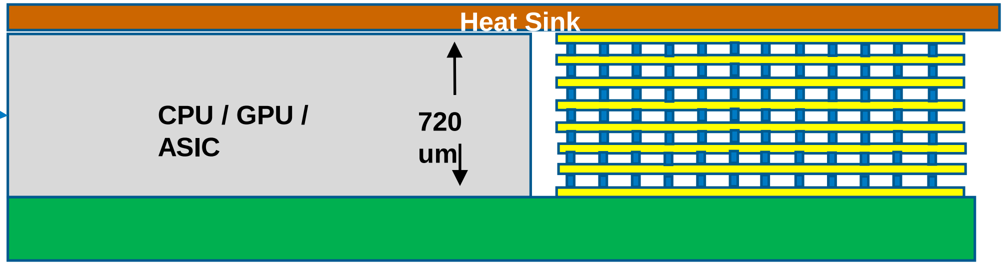


Solder extrusion during TCB (Cheng et al. ECTC 2015)

Drivers for Cu to Cu Interconnect

1. Higher Density Memory Stacking – Micron, Samsung, and Hynix
2. Extremely Fine Pitch – Intel, Huawei, Mediatek, Apple
3. Heterogeneous Integration – TSMC SoIC

Cross-Section with Heat Sink



Technology node		Critical dimension (nm)								
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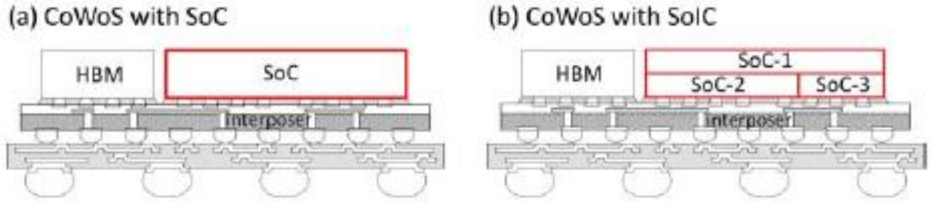
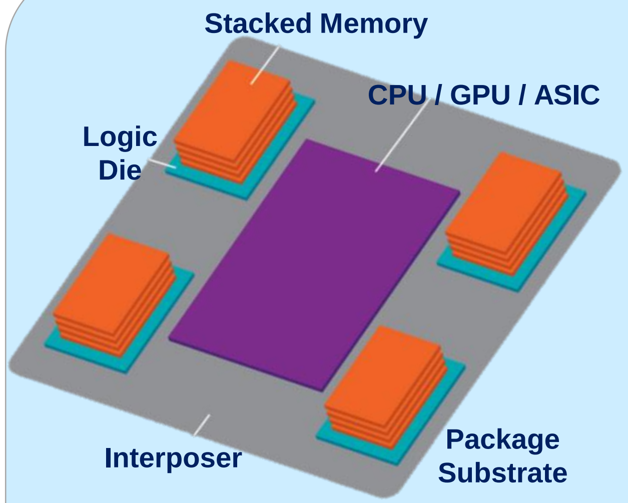
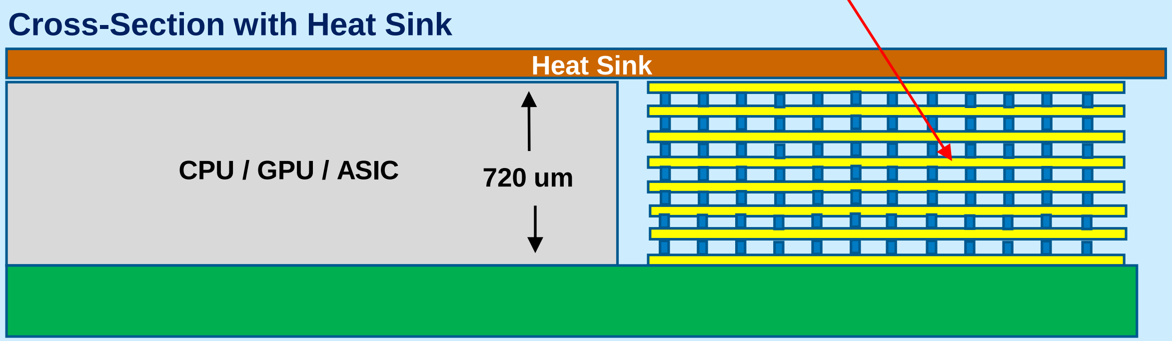


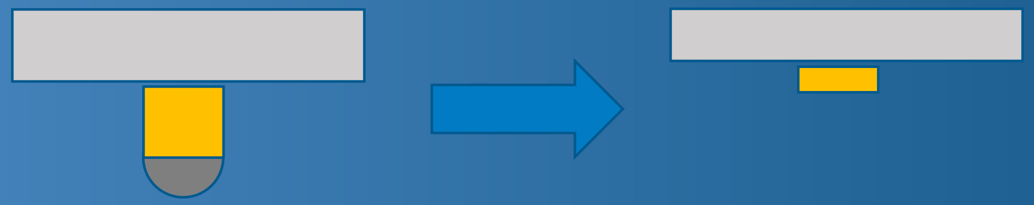
Memory Cu to Cu Stacking Solution – Small Pillars with Oxide Reduction (Formic Acid) Bonding



Typically 8-layers memory stacks : 90 um/layer
- **DRAM: 50 um,**
- **Cu pillar & solder cap: 40 um**



Memory stacks would trend towards 16 or 32 layers, but still maintain height requirement as GPU (heat sink)



Thinner die and eliminate solder with small Cu pillars with Cu to Cu interconnects

Source: K&S

Cu-Cu Bonding Results

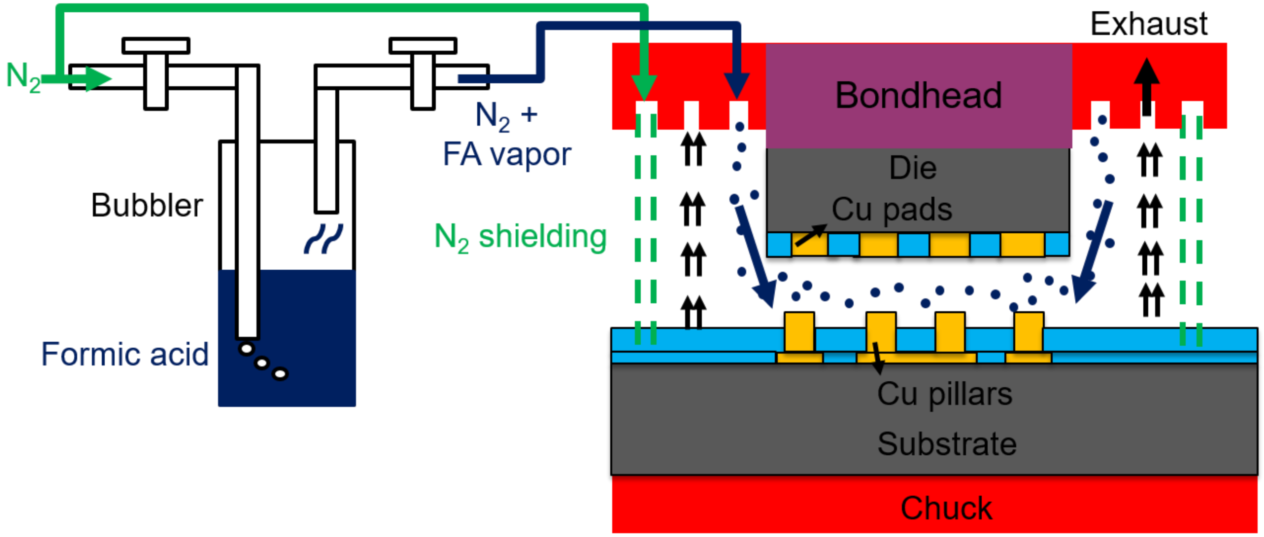
- Localized FA vapor delivery via shroud
- FA vapor reduces copper oxide and exposes pure copper

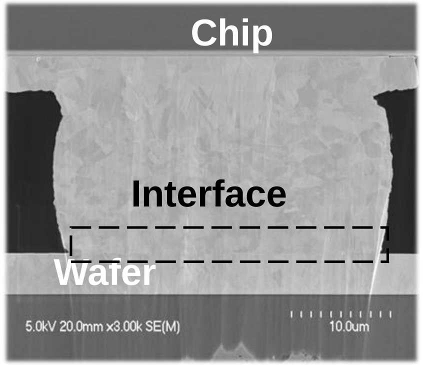
Step 1: Cu (II) formate creation (100 °C < T <150 °C)

$$\mathrm{CuO}_{(s)} + 2\mathrm{HCOOH}_{(g)} \longrightarrow \mathrm{Cu(COOH)}_{2(s)} + \mathrm{H_2O}_{(g)}$$

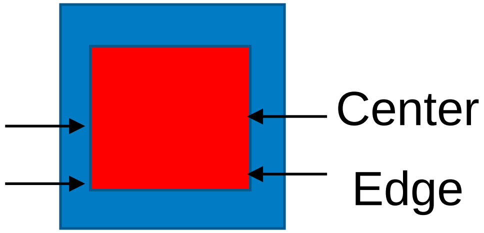
Step 2: Cu (II) formate decomposition (T > 200 °C)

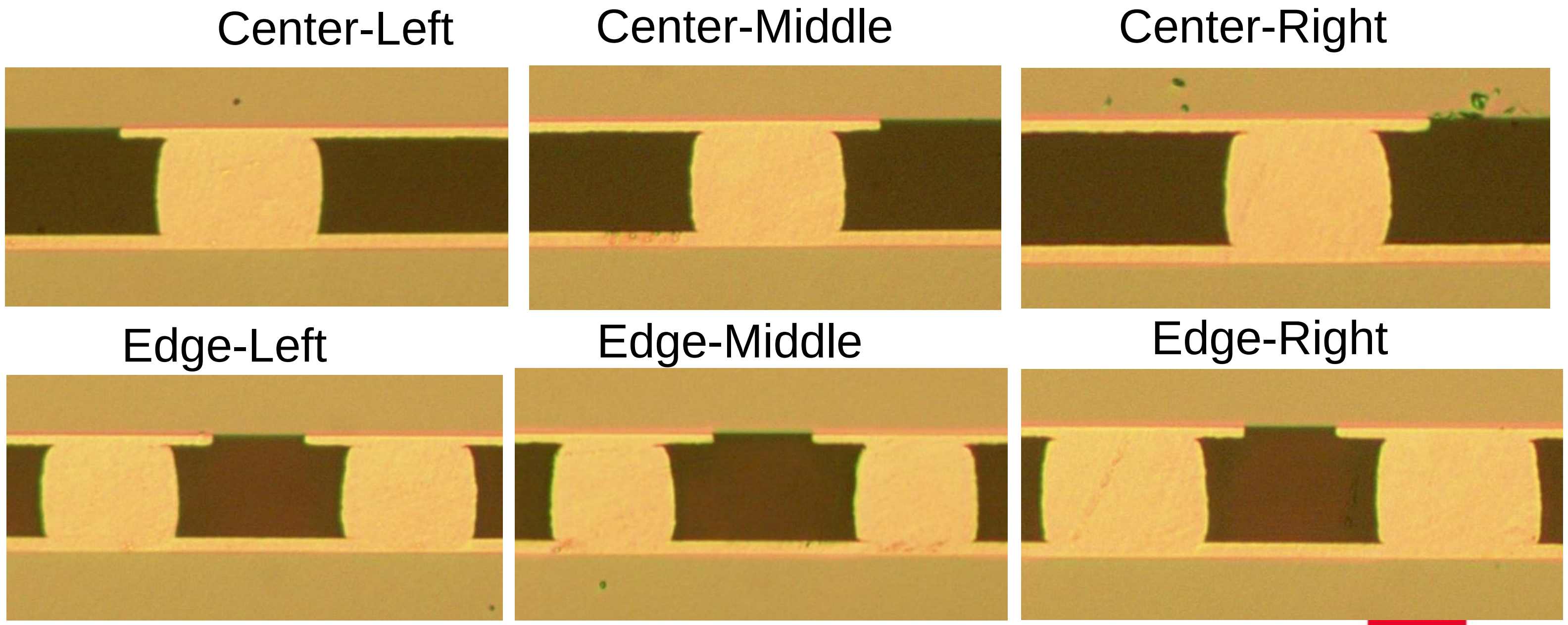
$$\mathrm{Cu(COOH)}_{2(s)} \longrightarrow \mathrm{Cu}_{(s)} + 2\mathrm{CO}_{2(g)} + \mathrm{H}_{2(g)}$$





Die bonded to Wafer

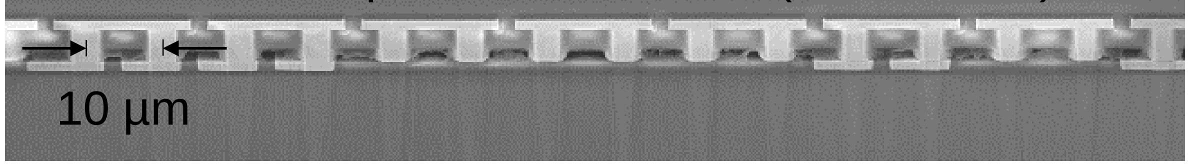




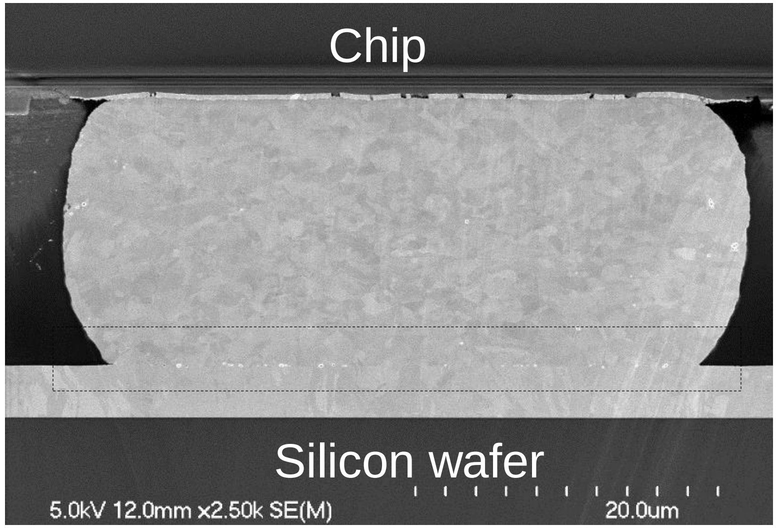
Cu-Cu TCB Summarized

- Applicable to both C2W & C2S applications
- Bonding accommodates all existing Cu-pillar finishes e.g. CMP, Fly-Cut, & As-plated
- Very high bond strength ~ 160 MPa
- Current bond time < 10 sec; Reductions in development

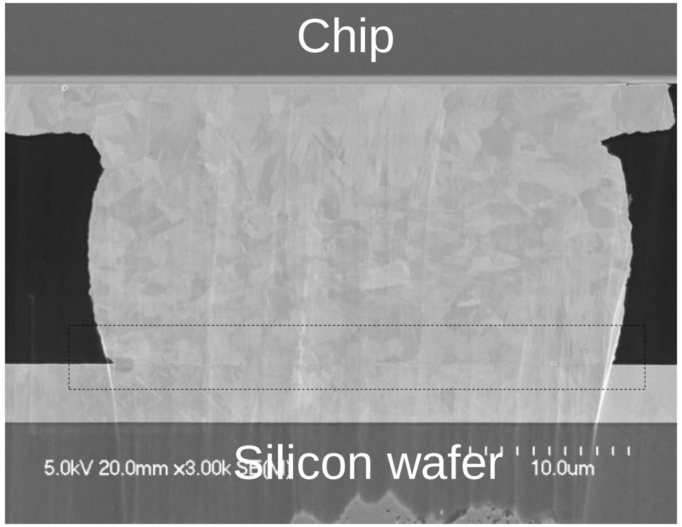
Ultra-fine pitch Cu-Cu bonds (CMP Finish)



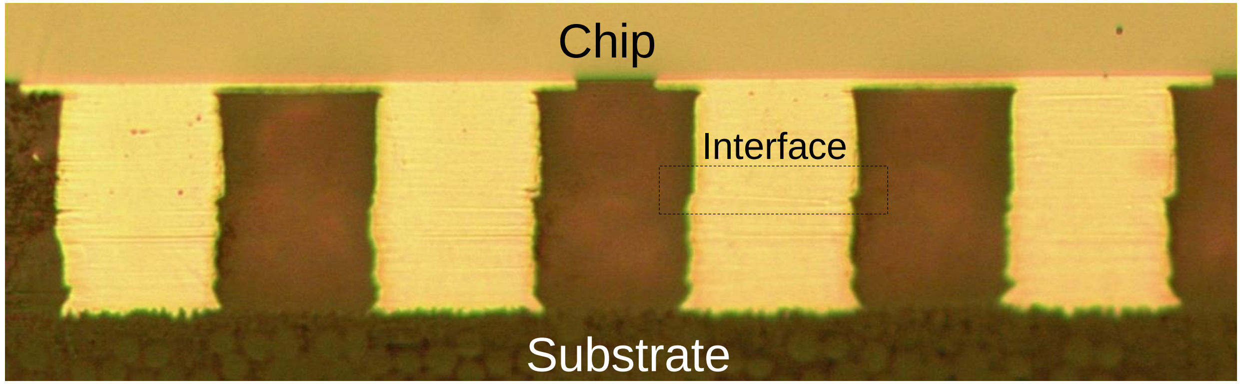
C2W as-Plated Cu pillar



C2W Fly-Cut Cu pillar



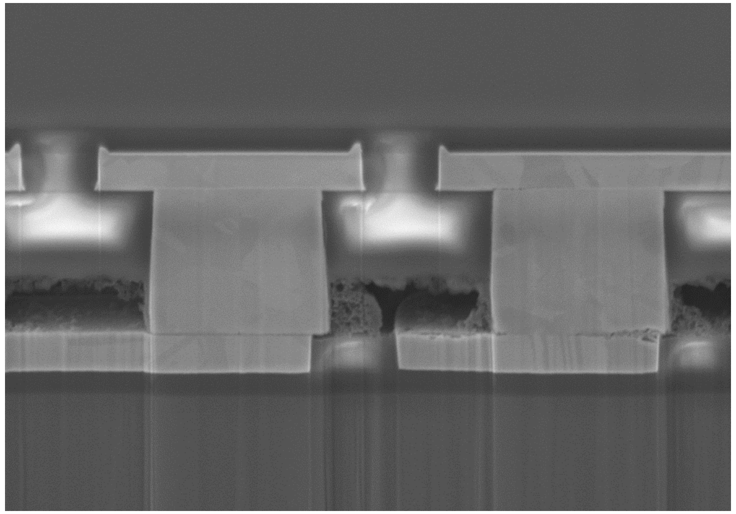
C2S as-Plated Cu pillar

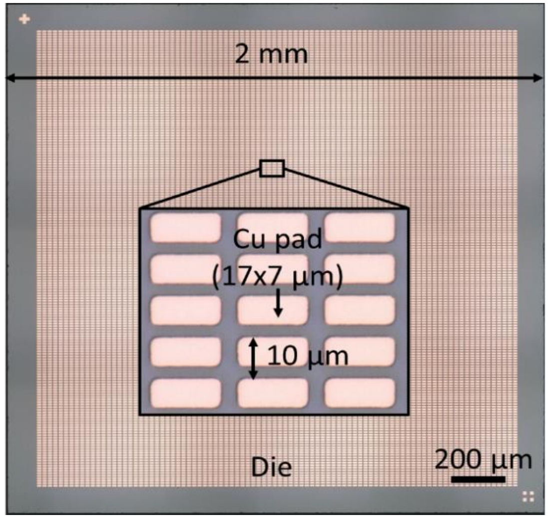


Interconnect Technology	Bond Shear Strength
Cu wire ball bonds	7-8.5 g/mil^2
Cu-pillars	12-15 g/mil^2

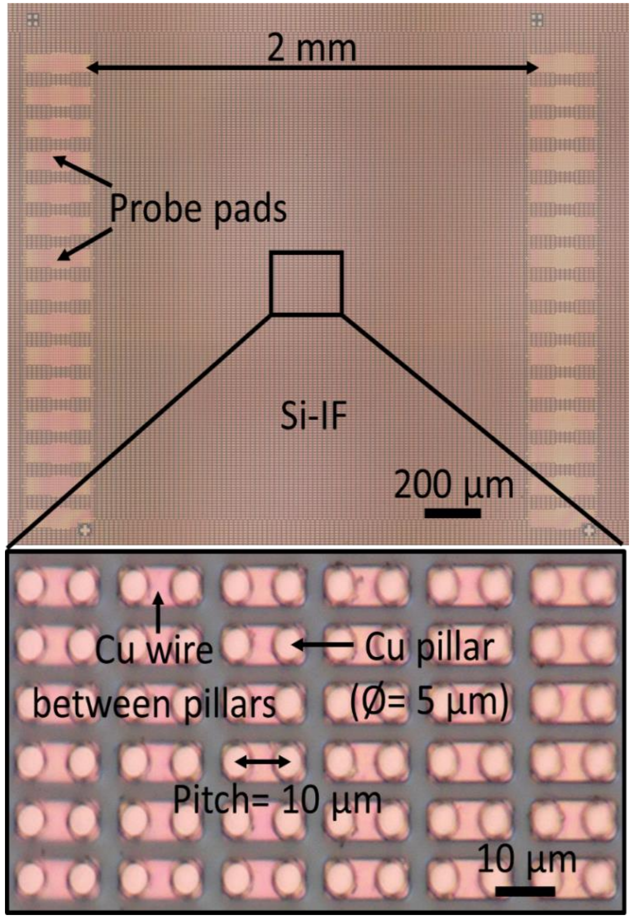
High Density Chiplet Cu-Cu Interconnects

- Research collaboration with UCLA CHIPS
- Substrate with Cu pillars
  - Cu Pillar pitch: 10 µm
- Die with Cu pads
  - Total contacts per chip: 36,000
- Roughness on both pillar & pad after CMP: < 2 nm





Chip with bond pads



Substrate with Cu-pillars

Summary

- Viable C2S & C2W fluxless TCB processes with in-situ tin oxide and copper oxide reduction are presented
- Novel patented shroud design mounts to TCB Bondhead, design by extensive FEA, maintains highest FA concentration over desired region
- Formic acid vapor provides an opportunity to eliminate flux
  - Reduces upstream fluxing process step (lower COO)
  - Eliminates bond head flux contamination and cleaning
- Formic acid vapor enables Cu to Cu interconnect

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