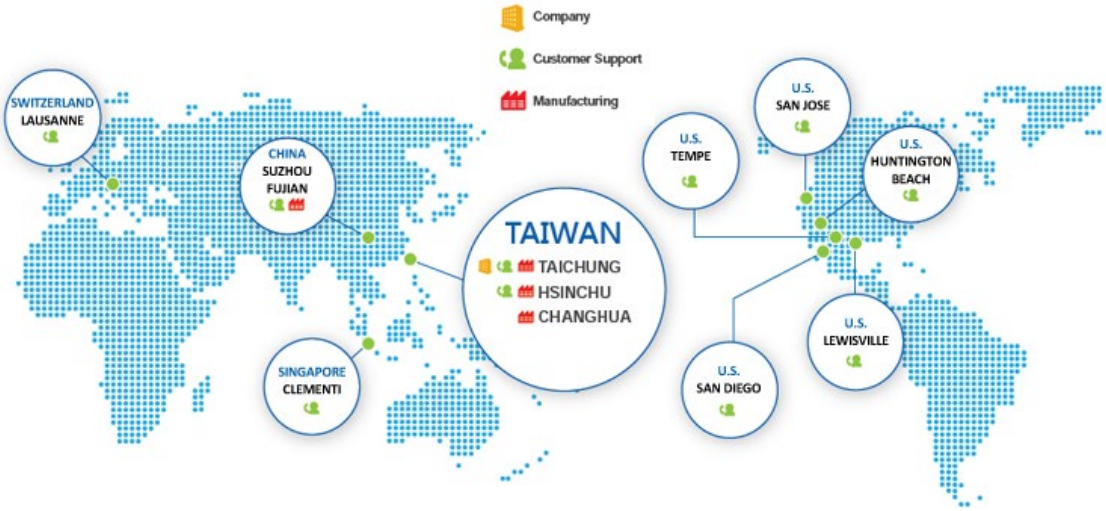
International Microelectronics Assembly & Packaging Society
16th International Conference and Exhibition on
DEVICE PACKAGING

Solution for Accelerator Wall of HPC with HBM Integrated Packages



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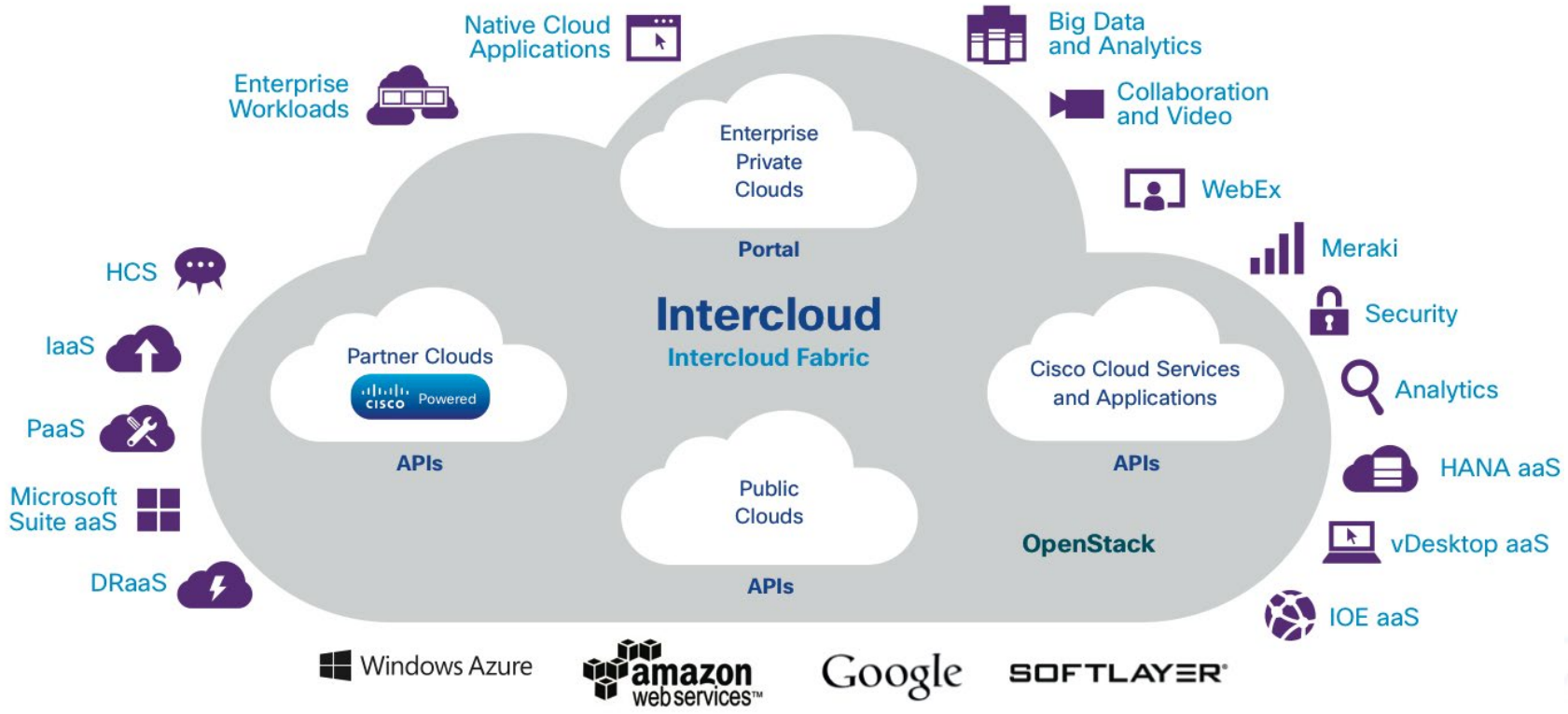
Outline

- Introduction: Accelerator Wall of HPC
- HIP Package Analysis
- Modeling : Insertion loss @ 0.5 – 10 Ghz
- Result & Discussion
- Summary

High performance computing is demand-orient computing infrastructures

- Fast growth of IT industry and transform the economy recently
- The scalable computing ranging from AI-edge to data-center, to increase the central workload of power plant.



Courtesy of Cisco blog

Energy efficiency on HPC infrastructure

- The electrical communication is another 50% cost portion of HPC infrastructure and following by the server, storage, and other elementary
- The electricity usage can be categorized into two segments: powering by IT equipment, and powering by infrastructure.

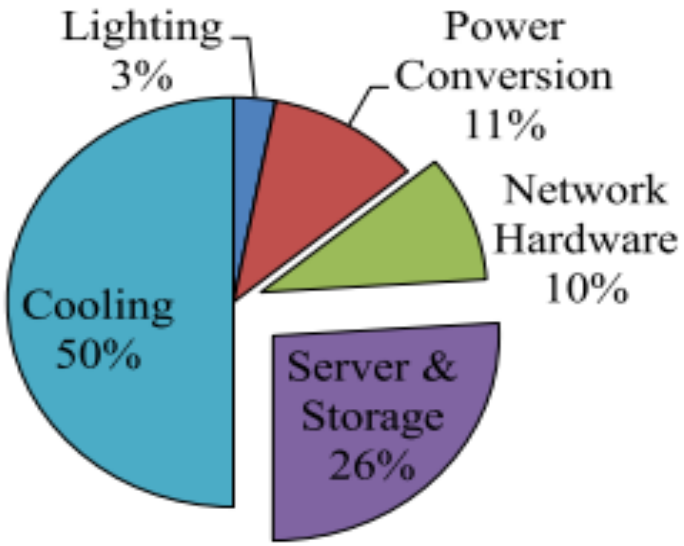


Fig.1 A holistic segment of energy consumption by subcomponent of HPC infrastructure [1].

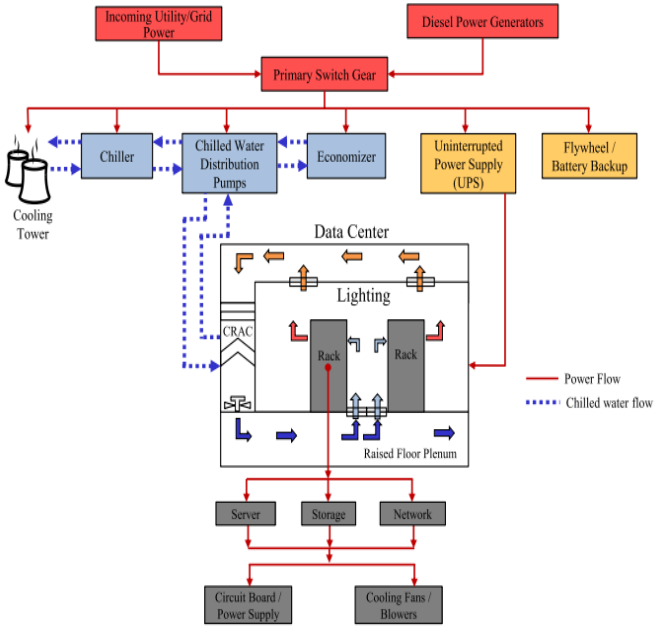
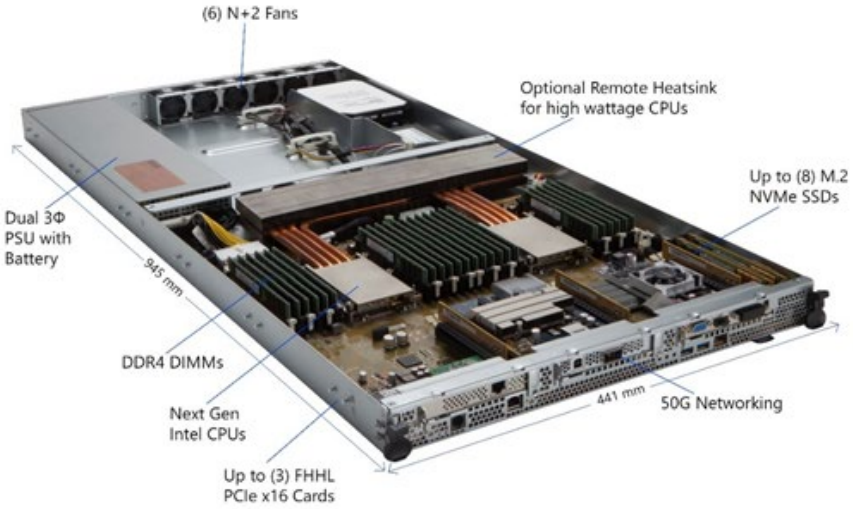


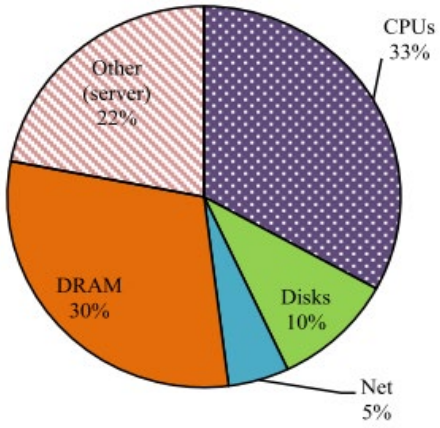
Figure 2. Diagram of cooling system with in-and-out bound energy flow in HPC infrastructure deployed [2].

[1] Info-Tech, "Top 10 energy-saving tips for a greener data center," Info-Tech Research Group, London, ON, Canada, Apr. 2010. [Online]. Available: http://static.infotech.com/downloads/samples/ 070411_premium_oo_greendc_top_10.pdf
[2]Y. Joshi, "Introduction to data center energy flow and thermal management," in Energy Efficient Thermal Management of Data Centers, Y. Joshi and P. Kumar, Eds. New York, NY, USA: Springer-Verlag, 2012, pp. 1–38.

Peak powering of rack-HPC deployed

- CPU/DRAM is consuming majority workload in the powering distribution.
- The factor of insertion loss is now considered as design index to fulfill the balance power efficiency and performance at peak workload.





An example for approximate distribution of peak powering of a warehouse scale HPC deployed at Google in 2007[3].

[3] L. A. Barroso and U. Hölzle, "The datacenter as a computer: An introduction to the design of warehouse-scale machines," in Synthesis Lectures on Computer Architecture, 1st ed., vol. 4. San Rafel, CA, USA: Morgan & Claypool, 2009, pp. 1–108

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- **HIP Package Analysis**
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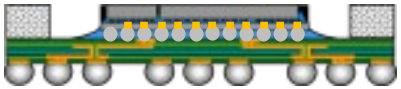
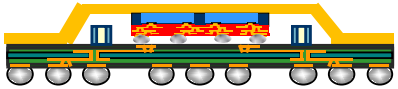
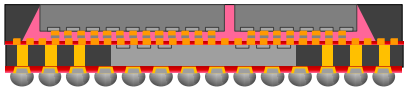
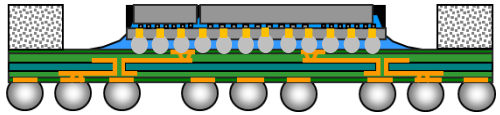
Advanced Packaging Evolution in SPIL

2015	2017	2018	2019
2.5D Technology enabling	2.5D Ramp up and mass production	FO technology enabling and tech qualification	FO product ramp/ FO-EB, FO-POP tech qual
 2.5D		 FO MCM	 Silicon Bridge

• 3 customers engaged, 5 products
• Standard BOM defined
• Design rule development
	• 4 products qualified and ramp
	• **Achieve >99% production yield**
	• New technology exploration
	  • FO-MCM
	  • Vertical stack (3D)
	  • **FO-POP**
		• **4 new products qualified and ramp** (FO-MCM, 2.5D)
		• Product driven technology extension
		  • 2.5D Thin chip (<1.7mm)
		• New technology exploration
		  • FO-EB
			• **Product ramp target +1** (FO-EB)
			• Product driven technology extension
			  • 2.5D thin chip + large package
			  • Multi bridge FO-EB
			  • Large FO-MCM
			• New technology exploration
			  • Si Pho using FO integration

2017 1st 2.5D production in SPIL
2018 1st product qualified using FO-MCM platform
2019 targeting 1st product qualification using FO-EB platform

2.5D T/K Floor Plan



HVM | Qualified | Develop

TSI Size (mm²)

1400
1200
800
600
400

1 + 4 HBM

2x (1 + 4 HBM) modules

(1 + 2HBM) + Chiplet

2 ASIC

3 ASIC

1 + 4 HBM

1 + 2HBM

1 + 4HBM

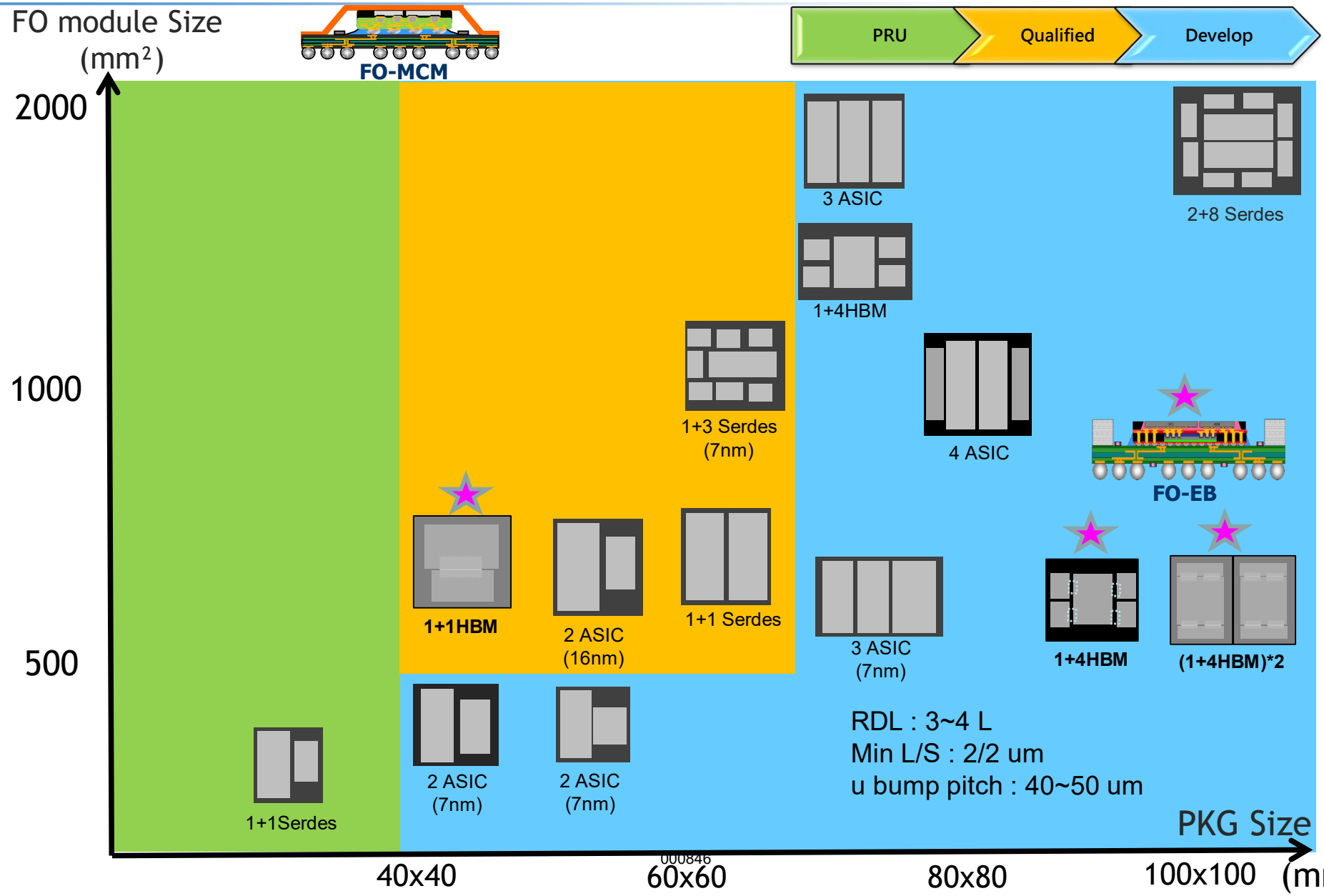
1 + 2HBM

1 + HBM

PKG total thickness : 1.6 ~ 3mm
ASIC thickness 400~1200 um
TSI thickness 100 um
Substrate core 400~1400 um

30x40 50x50 60x60 80x80 (mm)

FO-MCM & FO-EB Floor Plan



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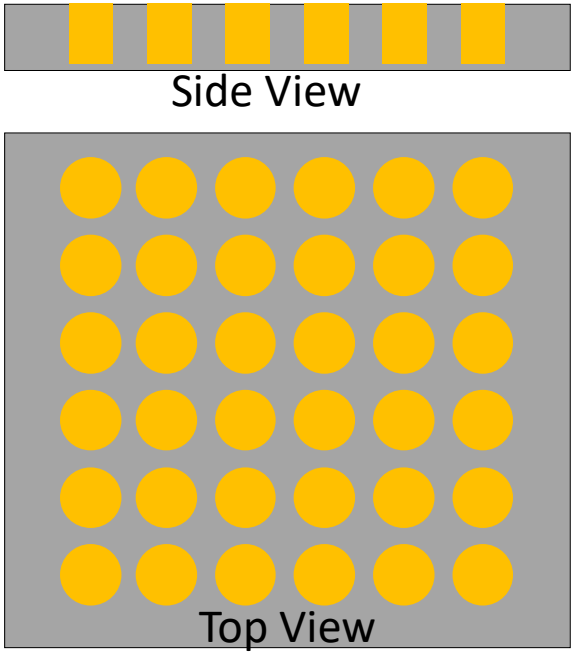
MODELING AND MECHANISM (1/2)

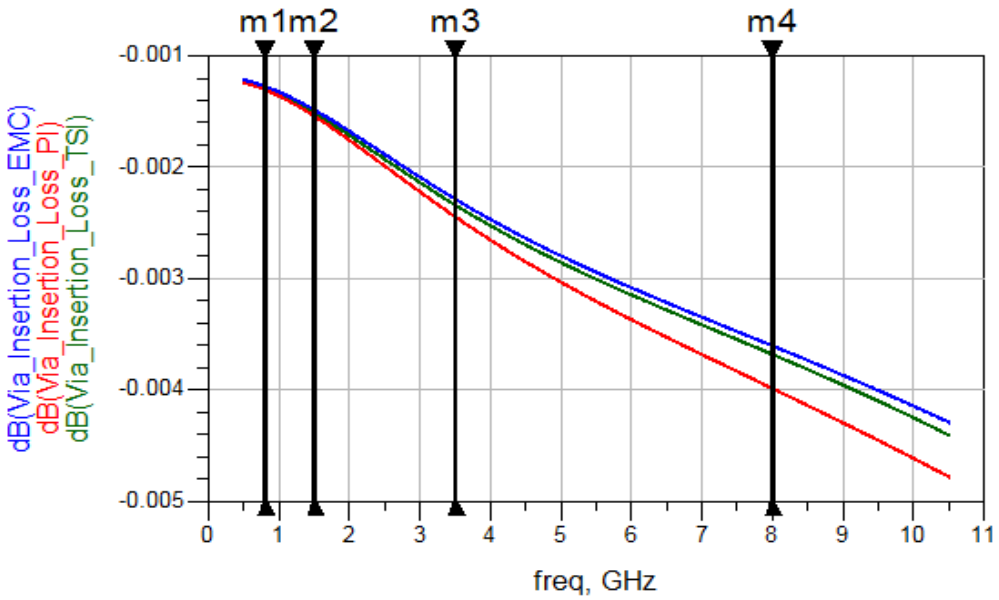
- Numerical model prep.:
  - Commercial software application, ANSYS HFSS
  - Finite differential modeling (FDM)
- Model I (Via deployed) for numerical analysis

Legend	*Description*
Carrier	◆ 1000 x 1000 um square model ◆ 50 um Thickness ◆ Material: TSI, PI, EMC
Via	◆ Width/Depth: 10/ 25 um ◆ Space: 10 um ◆ 40 x 40 count



The matrix in model I aims for vertical signal identified.

RESULTS AND DISCUSSION (1/2)



Legend	Description
Carrier	◆1000 x 1000 um square model ◆50 um Thickness ◆Material: TSI, PI, EMC
Via	◆Width/Depth: 10/ 25 um ◆Space: 10 um ◆40 x 40 count

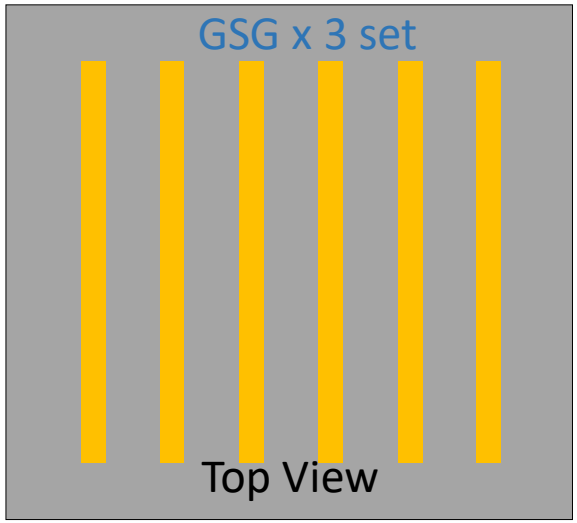
Item (Via =10 um) (Depth = 25 um)	Insertion loss @ 1.5 Ghz	Insertion loss @ 3.5 Ghz	Insertion loss @ 8 Ghz
TSI (dk=3.9 / df=0.004 @1Ghz)	0.00152 dB	0.00234 dB	0.00368 dB
EMC (dk= 3.2 / df =0.004 @1Ghz)	0.00149 dB	0.00229 dB	0.00361 dB
PI (dk=3.3 / df=0.01 @ 1Ghz)	0.00154 dB	0.00245 dB	0.00399 dB

- In Via deployed model, the numerical analysis is ranging from 0.5 Ghz to 10 Ghz
- Three material rendering the siginal loss. TSI (2.5D) and EMC (FO-EB) is no sigificant loss due to df value is similar.

MODELING AND MECHANISM (2/2)

- Numerical model prep.:
  - Commercial software application, ANSYS HFSS
  - Finite differential modeling (FDM)
- Model II (Wire Through) for numerical analysis

Legend	*Description*
Carrier	◆ 1000 x 1000 um square model ◆ 50 um Thickness ◆ Material: TSI, PI
Line	◆L/W/S/T: Designed ◆GSG x 3set



The matrix in model II aims for horizon signal identified.

RESULTS AND DISCUSSION (2/2)

Item	Material	Length (um)	Width/Space/Thickness (um)		
			0.4/0.4/0.8	2/2/4	8/8/16
Insertion loss @ 1.5 Ghz	TSI	200	0.99324 dB	0.05420 dB	-
	PI		-	0.05456 dB	0.00483 dB
Insertion loss @ 3.5 Ghz	PI	200	-	0.06119 dB	0.00803 dB
		700	-	0.21836 dB	0.03149 dB
Insertion loss @ 8 Ghz	PI	200	-	0.07255 dB	0.06308 dB

- In wire through model (HBM-ASIC path), TSI-2.5D & PI-FO-EB gap observed.
- To identify the individual gap scalability, the dimension factor of wire routability is observed with GSG deployed. The insertion loss is performed better. The length is inverse the performance with arbitrary unit.

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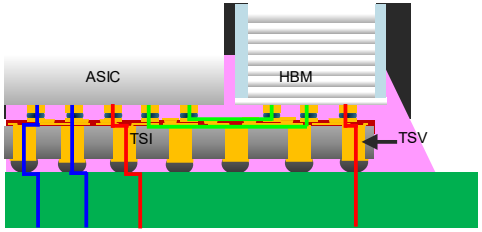
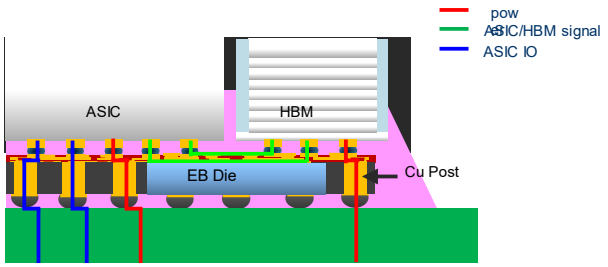
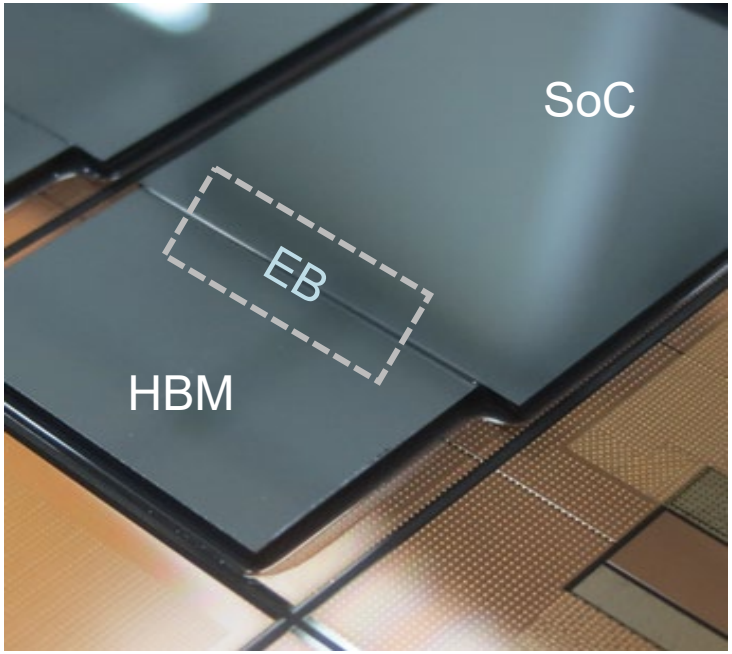
Application (1/2)

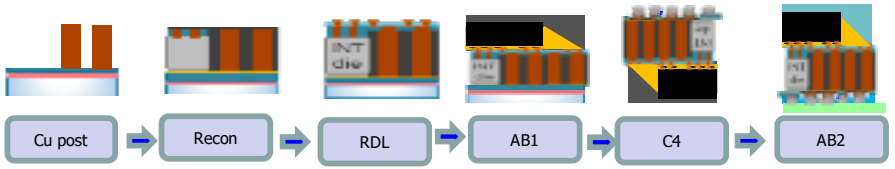


2.5D

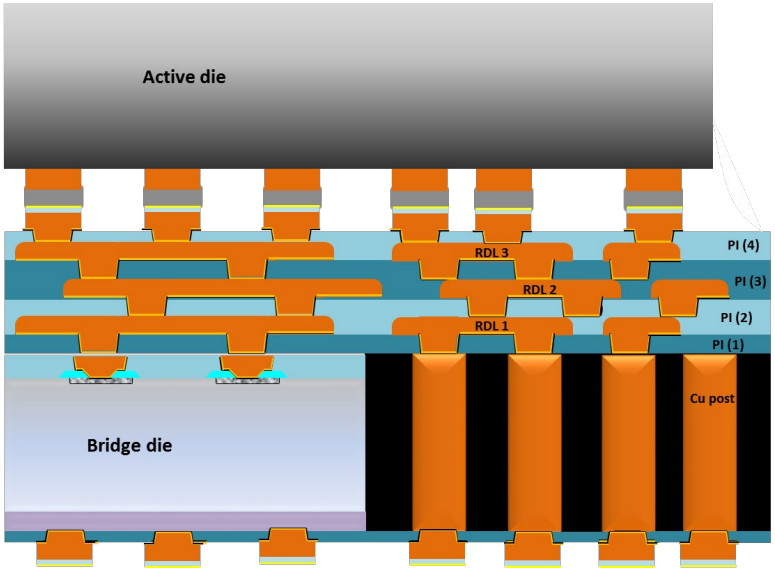


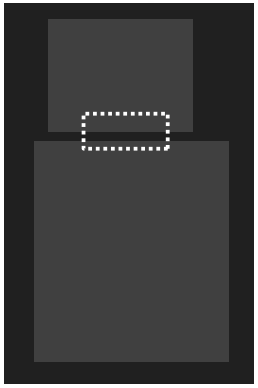
FO-EB
(Embedded Bridge)

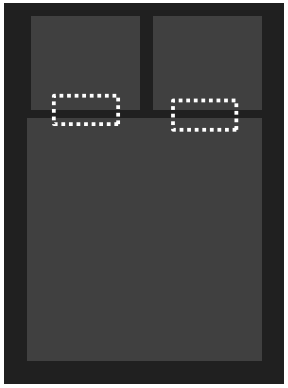


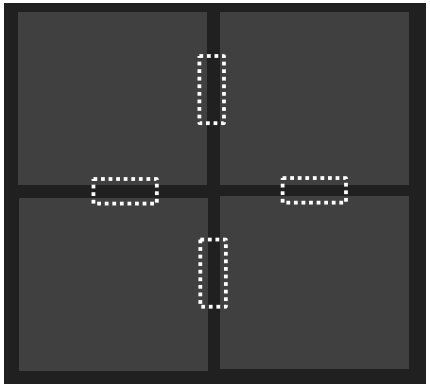


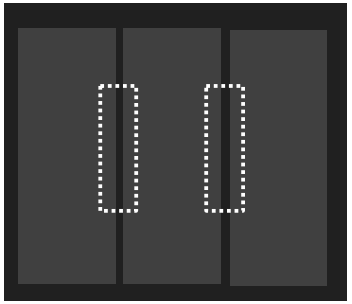
Application (2/2)

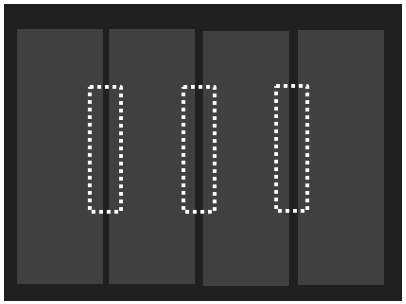


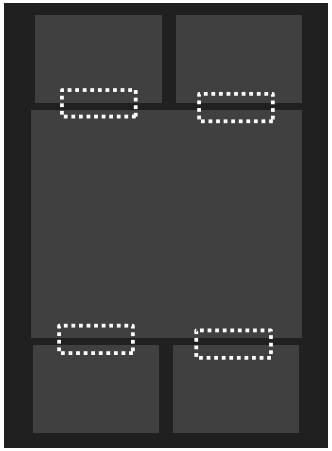


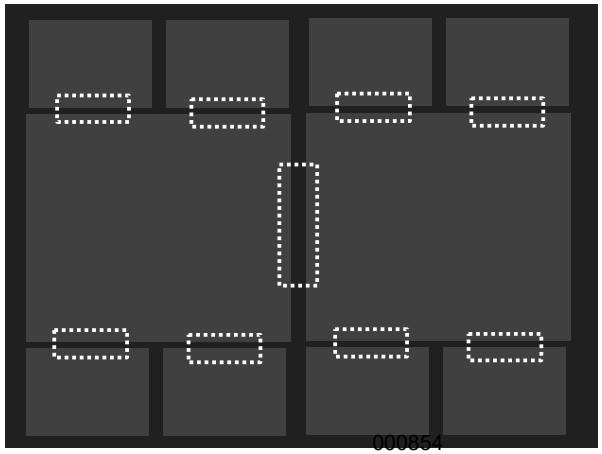


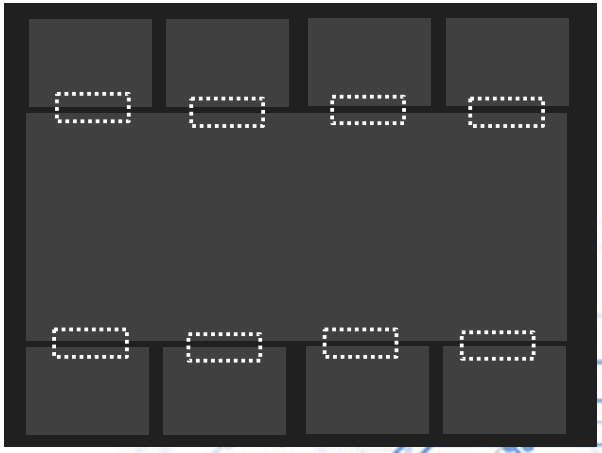








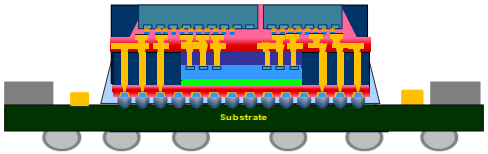




Works (1): 31x45 mm FO-EB (1 SoC+1 HBM)

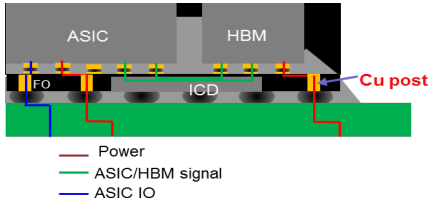
PKG information

- PKG size (mm^2): 1400
- Module size (mm^2): 450
- HBM size (mm^2): 100
- ASIC size (mm^2): 240
- Si Bridge (mm^2): 40



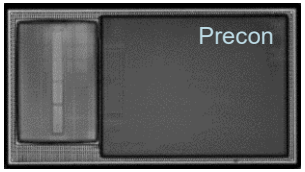
Si Bridge position:

- High speed channel connection
- No TSV underneath the bridge die

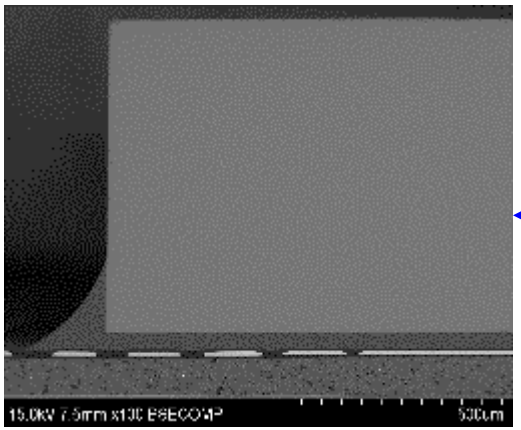


Performance verification:

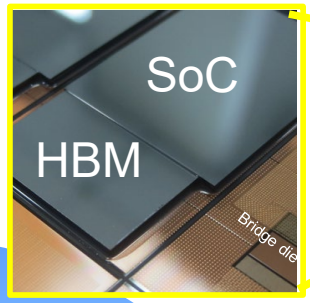
- RT pass TCG1200x, uHAST 264hrs, HTST1000hrs

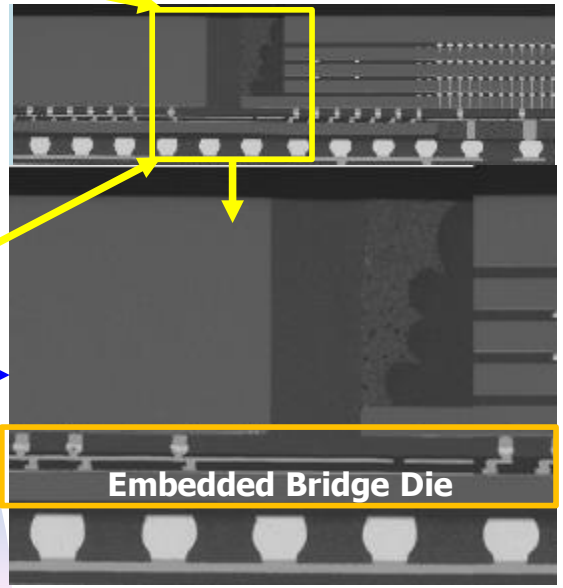


Featured (1/2): FO-EB Platform

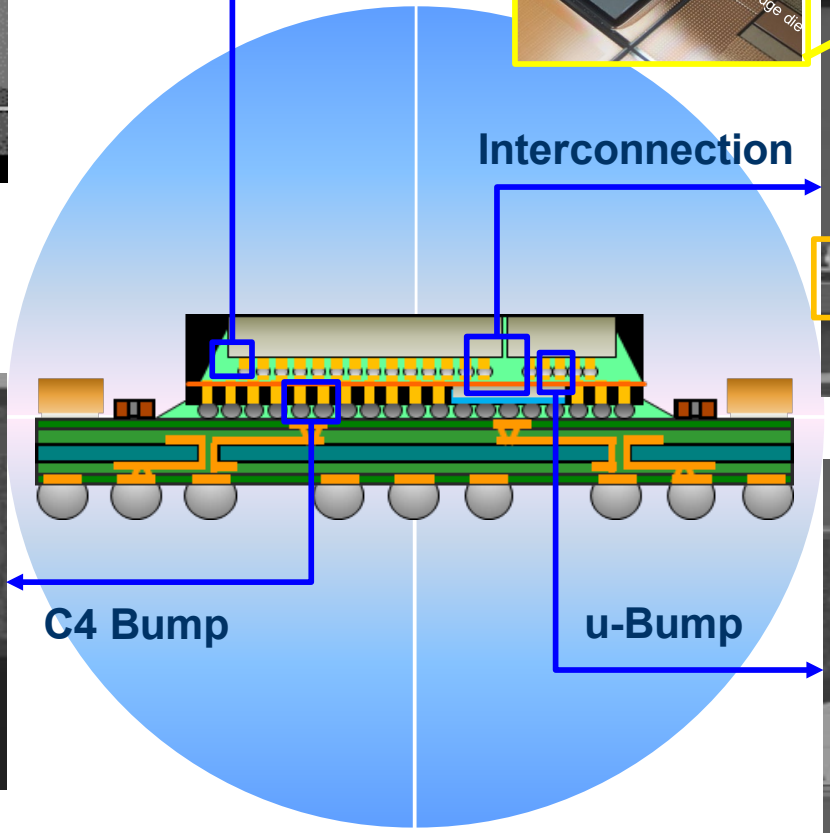


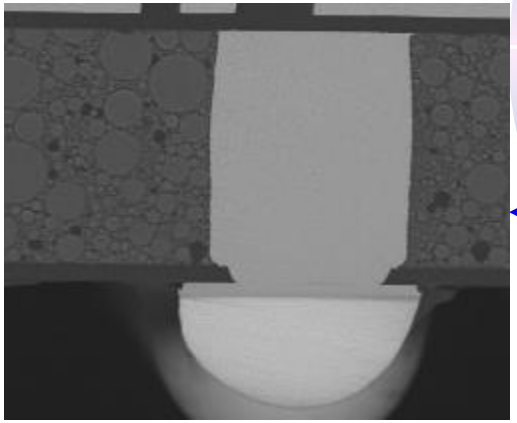
Chip / ELK Check





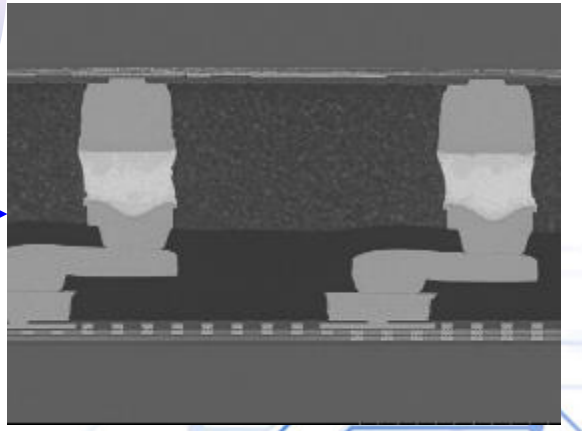
Interconnection



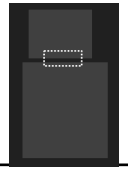
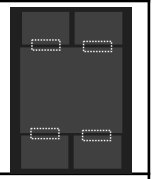
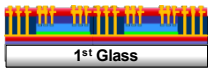
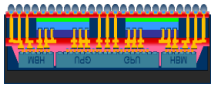
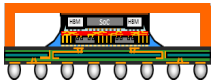


C4 Bump

u-Bump



Featured (2/2): Process Review Index

Stage		Structure	MTS	
			1+1	(1+4) *2
1	Cu post+ Recon		1. Mold THK: 85um 2. Cu post pitch: 150um 3. ICD q'ty-1pcs 4. ICD size: 40 mm^2 	1. Mold THK: 85um 2. Cu post pitch: 150um 3. ICD q'ty-4pcs 4. ICD size: 40 mm^2 
2	RDL+ uPad		1. Min RDL L/S: 10/10 2. Stud/Via Size: 30/13 3. Via vs ICD Q'ty: 1pcs	1. Min RDL L/S: 10/10 2. Stud/Via Size: 30/13 3. Via vs ICD Q'ty: 4pcs
3	Wafer form		1. Die gap 2. ASIC size 3. MG2 thk	1. Die gap 2. ASIC size 3. MG2 thk
4	C4		1. Min Bump pitch 2. Bump dia 3. LF solder	1. Min Bump pitch 2. Bump dia 3. Cu pillar
5	Unit form		1. CM size: 450 mm^2 2. Pkg size: 1400 mm^2 3. Stiffener ring	1. CM size: >1000 mm^2 2. Pkg size: >5000 mm^2 3. Stiffener ring

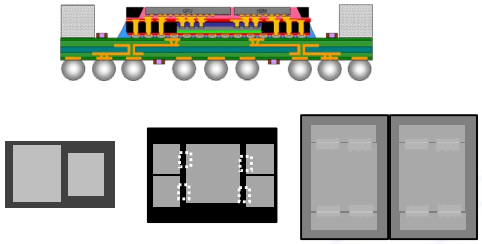
Summary

- Breakthrough the accelerator wall : index of HPC with HBM integrated path.
  → FO-EB is better than 2.5D at 3.5Ghz/8Ghz.

- Breakthrough the powering communication : index of Via deployed
  → FO-EB featured: Thru EMC and PI. (TSI for 2.5D).
  → Both of HIP package is effectivity of dynamic workload with df value.

- The result is to achieve for via deployed and wire through at numerical analysis.

- FO-EB Platform
  - Availability: Platform is certificated. FT result will be ready by Q2'2020
  - Benefit on chiplet module (2 SoC +8HBM floor plan).



Q & A

Siliconware Precision Industries Co. Ltd.