XPERI

Cu Interconnect Scaling with Hybrid Bonding for 2.5 and 3D Integration

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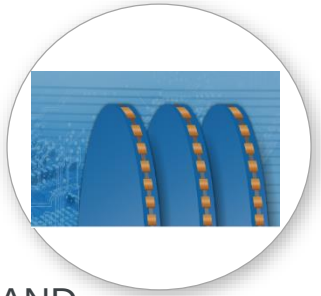
Outline

- Direct Bond Interconnect (DBI®) Platform Technology and Advantages
- DBI® Ultra Die to Wafer Hybrid Bonding
- Criteria for a HVM Compatible Process
- Test Vehicle Results
- Summary

DBI: Wafer to Wafer Bonding Applications

Wafer to Wafer (W2W) Bonding

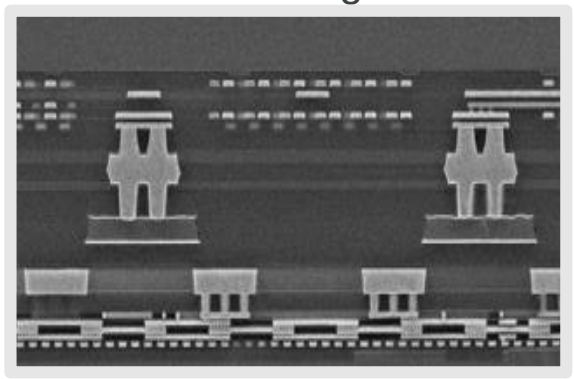
Image Sensor



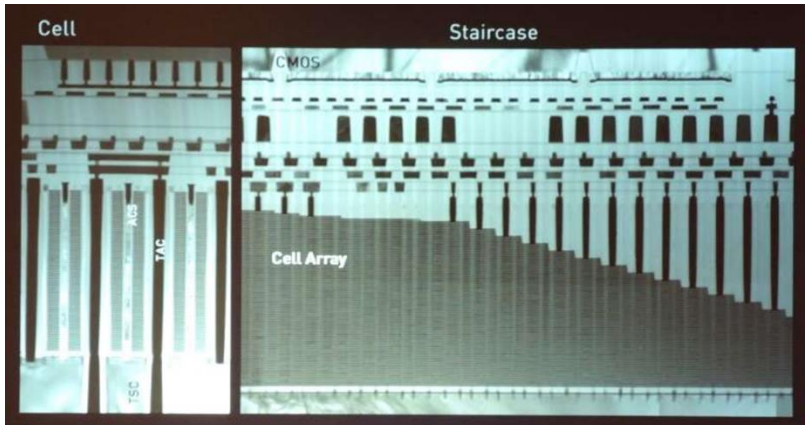
3D NAND

Examples

DBI Enabled Image Sensors



NAND



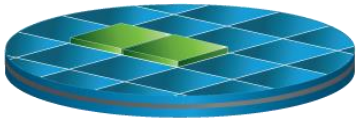
YMTC presentation at Flash Memory Summit August 2018; Xtacking™

Advantages

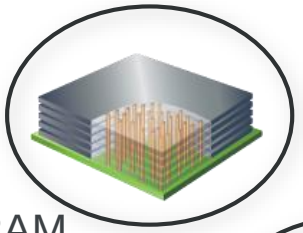
- Image Sensor Applications
  - In high volume manufacturing
  - Increased market share of early adopter
  - Enhanced and flexible product portfolio
- Future Applications in NAND
  - Enhanced performance:
    - Monolithic die density increases
    - Avoid NAND/Logic thermal budget constraints
  - Bit density increase:
    - Layout efficiency through stacking
  - Time to market reduction:
    - Modular, parallel processing of logic and memory reduces R&D cycle time

DBI® Ultra n-Die Stack Applications

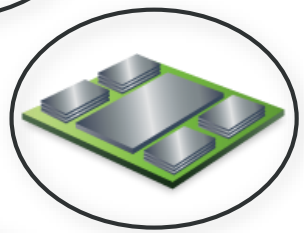
Die to Wafer (D2W) Bonding



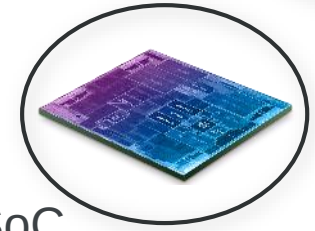
Applications



DRAM

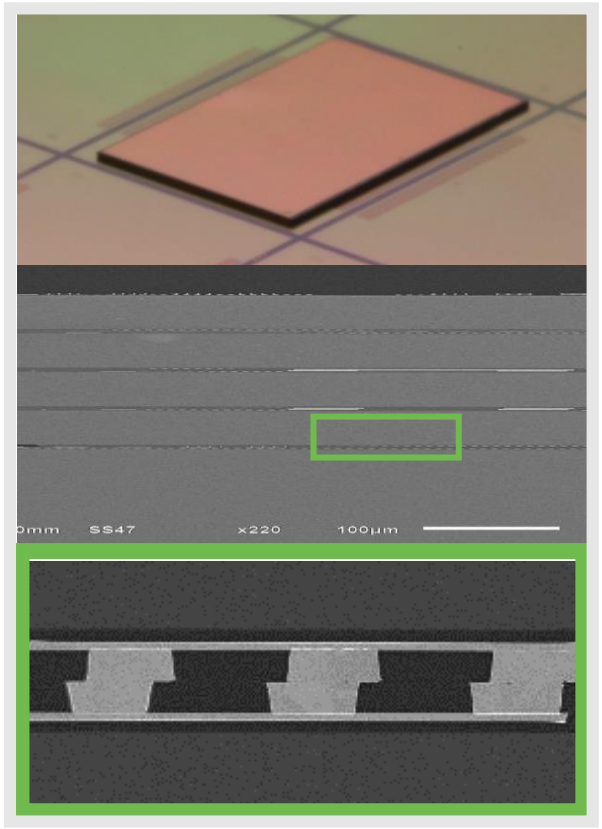


2.5D Logic + Memory



SoC

4-Die Stack Example
(5 um Pad / 10 um Pitch)



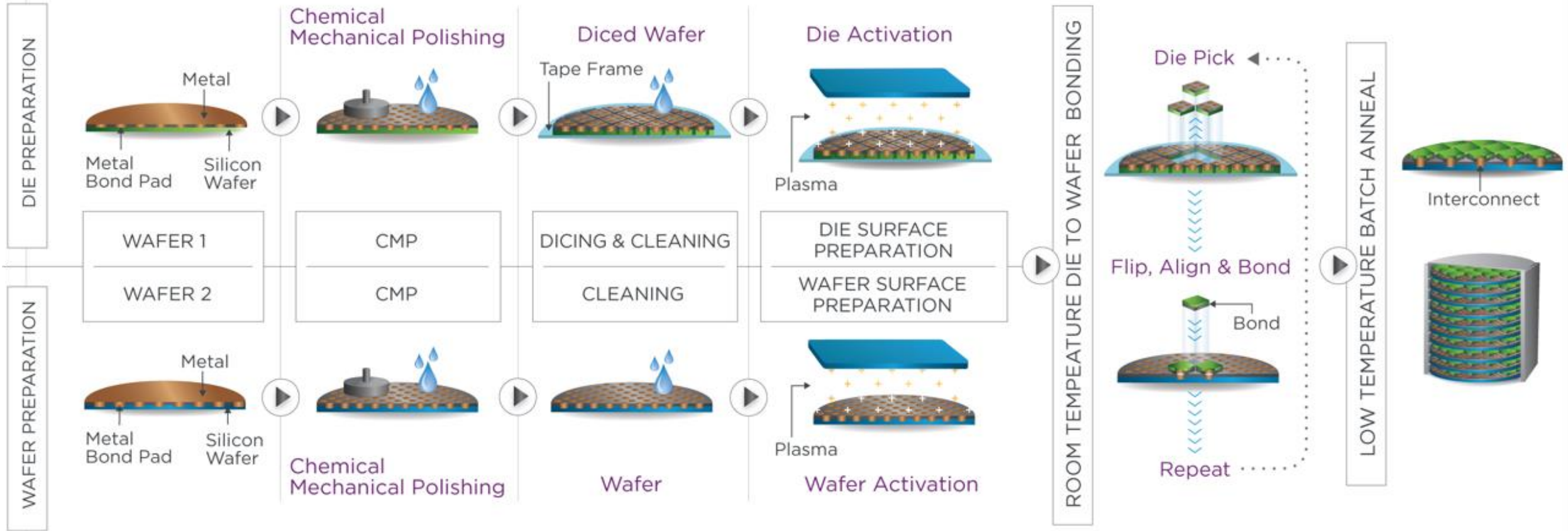
Advantages

- Enhanced memory performance
  - Improved RLC characteristics[1]
  - Superior thermal performance[1]
  - Interconnect pitch scales to ~ 1um
  - No added standoff height
  - Better overall reliability
    - Organic materials eliminated
    - Cu-Cu bond improves with thermal cycling
- Potential lower process cost
  - Solder and underfill eliminated
  - High throughput bonding
  - Pathway to fewer mask steps[2]

[1]A. Agrawal et al. “Thermal and Electrical Performance of DBI Interconnect for 2.5 and 3D Interconnect” ECTC 2016.
[2]G. Gao et al. “Low Temperature Cu Interconnect with Chip to Wafer Hybrid Bonding” ECTC 2019.

DBI® Ultra Process Flow

Die to Wafer Hybrid Bonding

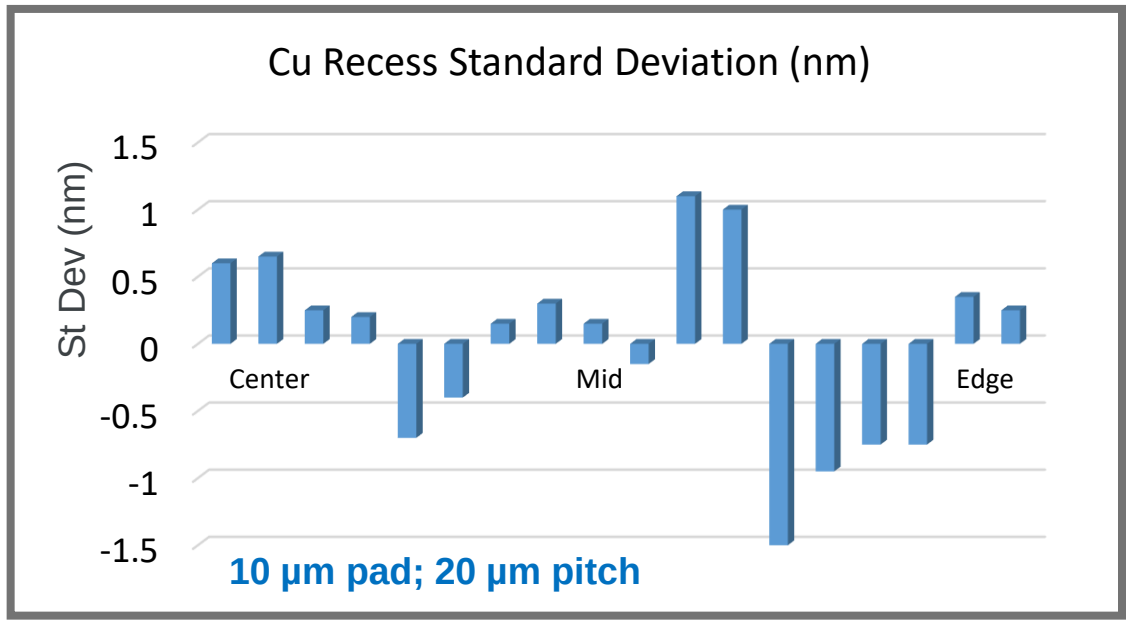


Requirements For an HVM Compatible Die to Wafer Process

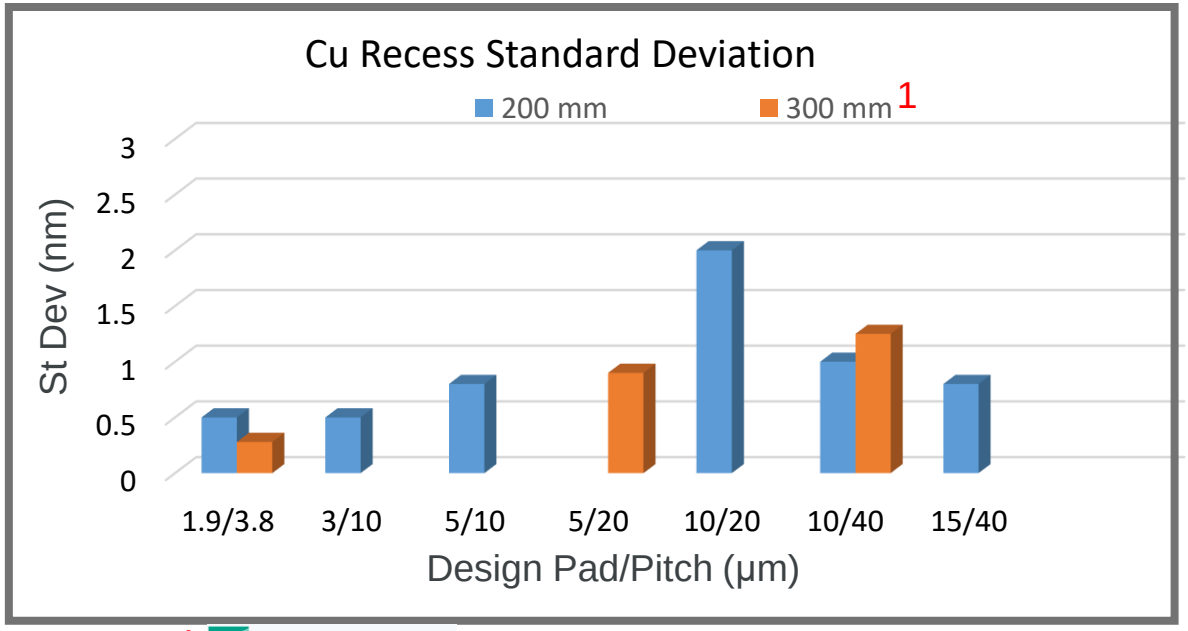
- Robust nanoscale engineering (CMP)
- Dicing and die handling must be compatible with industry supply chain
- Pick and place bonder design must be compatible with hybrid bonding

Robust CMP Process for DBI

Within Wafer Uniformity



Within Lot Uniformity



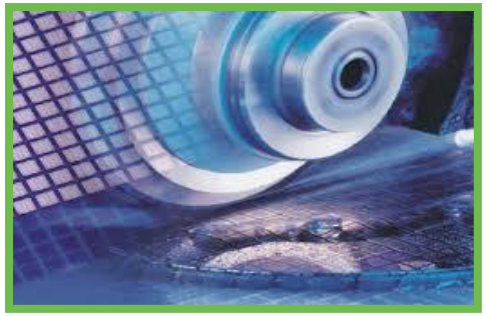
1 Fraunhofer IZM ASSID – All Silicon System Integration Dresden

- Excellent surface topography uniformity across wafer
  - Demonstrated for pad sizes of <2 µm to 15 µm
- Process reproducibility has been qualified
- Recipe on 200 mm transferred to 300 mm tools

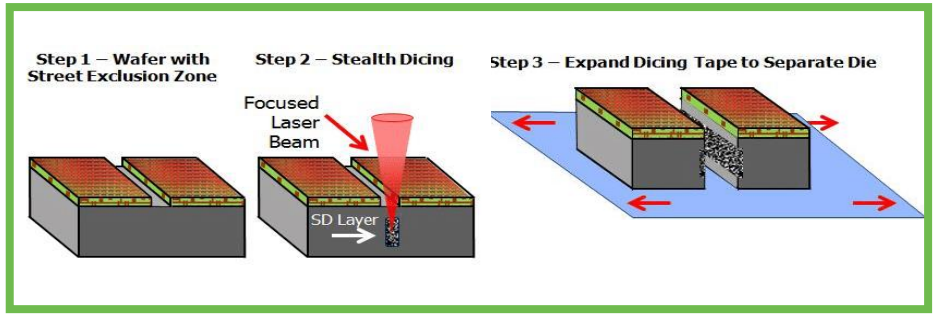
Dicing and Die Handling Compatibility with Industry Supply Chain

- Compatible with all dicing techniques

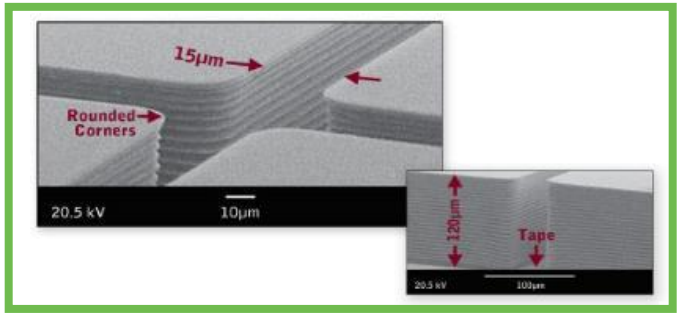
Sawing



Stealth



Plasma

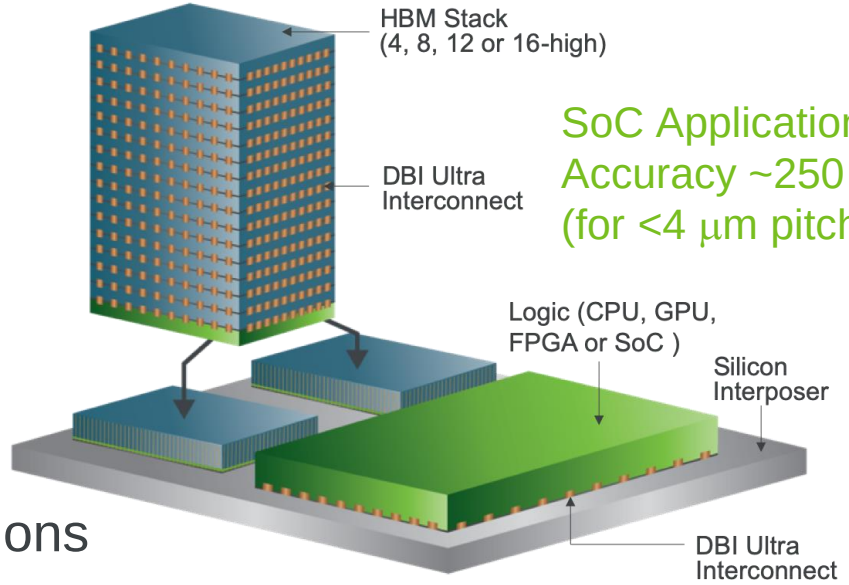


  - All three techniques demonstrated. Mechanical saw dicing and stealth most common.
- Die handling on tape is the industry standard
  - Xperi DBI Ultra qualified process is die on tape
- Standard inventory management
  - No queue time issues across entire process flow
  - Host wafer and die on tape: No issues for storage up to 12 months

Pick and Place Bonder Must Be Compatible with Hybrid Bonding

- Next generation pick and place tool requirements
  - Pick die from tape frame
  - Clean bonding environment:
    - Pathway to ISO 4/3 (Class 10/1)
  - Alignment accuracy per application
  - Bonding process considerations for HVM
    - In-situ inspection
    - Process parameters specific for hybrid bonding

3D Stacking
Accuracy ~ 3-5 μm
(for 20 μm pitch)



SoC Applications
Accuracy ~250 nm
(for <4 μm pitch)

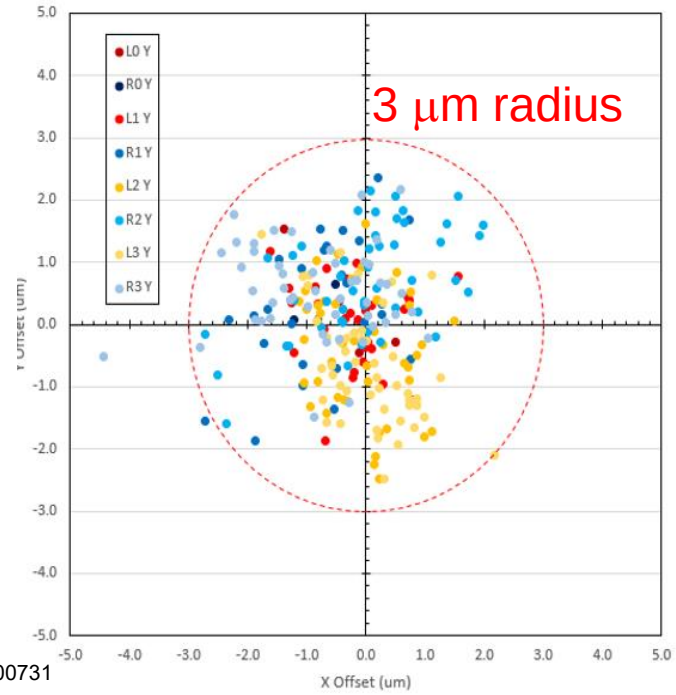
- Suppliers are re-designing for hybrid bonding applications
  - BESI[1], K&S, ASM Amicra, and more

[1]Ruud Boomsma, “Advanced Bonding Technologies for Next Generation 3D and SIP Devices”, 3D &Systems Summit 2020.

Improved In-house Bonder Capability – Besi Chameo Advanced

Improved Features for DBI Ultra Bonding:

- Alignment Accuracy +/- 3 μm (3σ) demonstrated
  - Potentially capable of bonding 5 μm pad on 10 μm pitch
  - Improved accuracy (especially rotation) for large die
- ISO 3 (Class 1) Clean Kit installed
  - Reduced risk of bonder-related particle contamination
- Increased throughput
  - 2,000 UPH / gantry x 2 gantries



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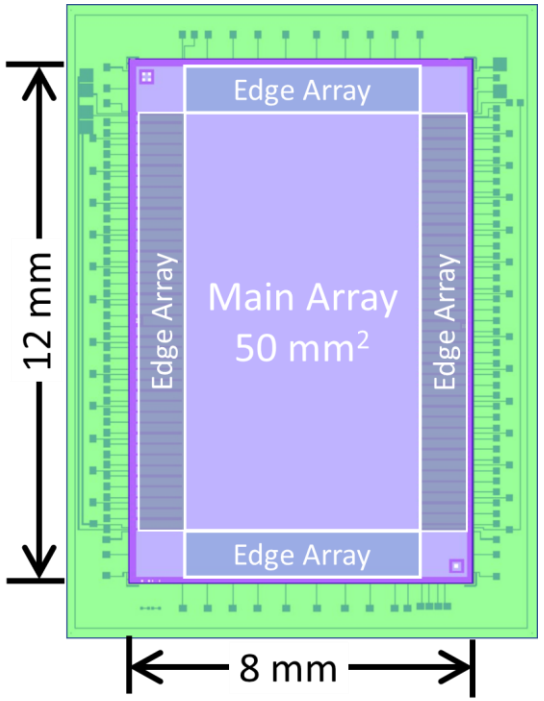
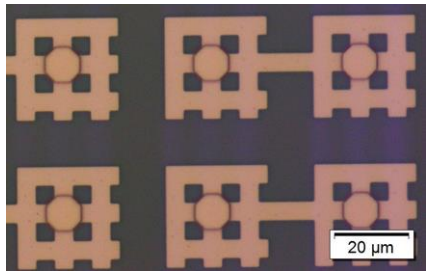
DBI® Ultra Die to Wafer Test Vehicle Results

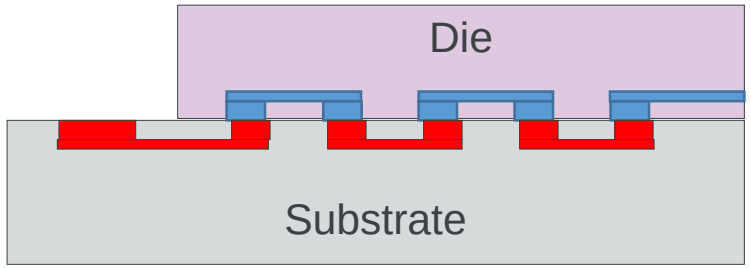
- Test vehicle design
- Reliability performance
- Low thermal budget compatibility
- Assembly process yield / defects
- Sensitivity to misalignment
- Yield improvement
- Stacking results

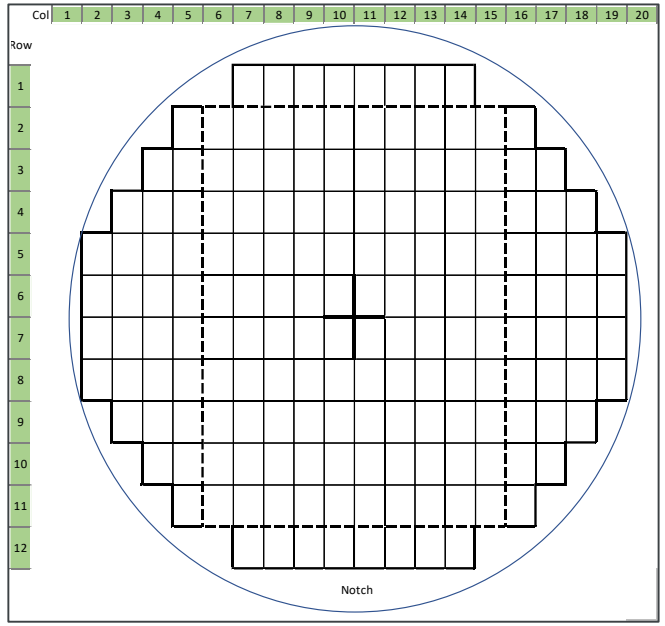
DBI® Ultra Test Vehicle Parameters





Link Structure



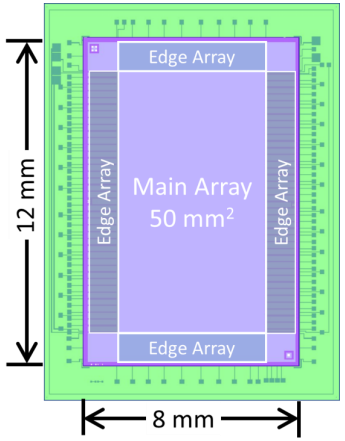


200 mm Wafer Layout

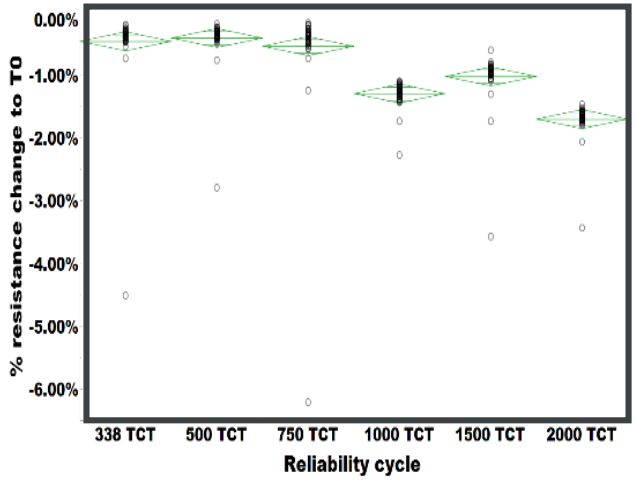
- 8 x 12 mm Test Chip
- 2 Layer Metal Pattern: RDL + DBI Bond Pads
- 10 µm pad on 40 µm pitch
- Main Center Array: 50 mm² with 31,356 daisy chain links
- Edge Arrays: 3400 – 5000 links, with links within 200 µm of die edge
- Low Resistance Link: allows evaluation of interconnect quality
- Both 200 mm and 300 mm substrates and component die

DBI® Ultra Interconnect Reliability Performance

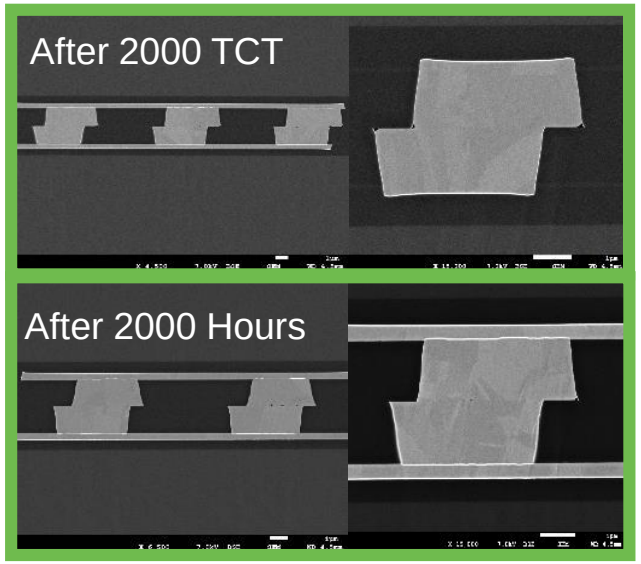
Test Vehicle



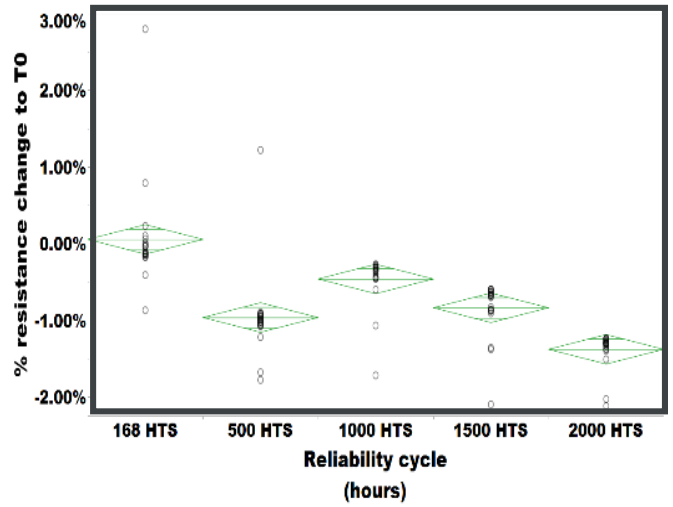
Temperature Cycle Test (TCT)



XSEM of Interconnects



High Temp Storage Test



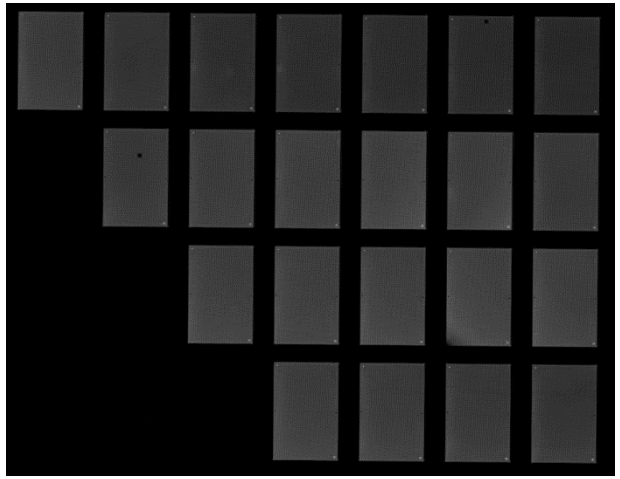
Test	Standard	Automotive Test Condition	# Parts	Cycle / Hours	Result
Temp. Cycling[1]	JESD22-A104D (M)	-40°C to 150°C, 1000 cycle	45	2000 cycles	100% pass
High Temp. Storage[2]	JESD22-103D	225°C / 275°C, 1000 hours	22	2000 hours	100% pass

[1] Test structure had 5 μm pad sizes
[2] Test structures had 5 & 10 μm pad sizes

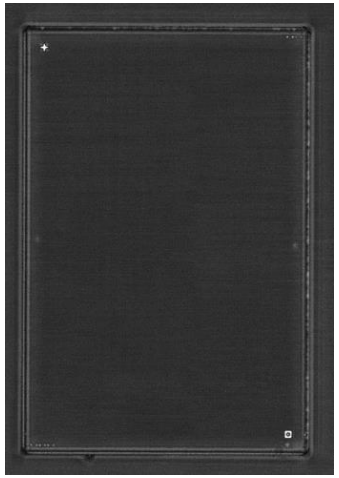
Thermal Budget Compatibility: Low Temperature Anneal Results

- E-test Results for DBI Ultra Test Vehicle: Yield vs Anneal Profile[1]
  - Temperature-skew split lots show 100% yield for anneals at 200°C for 1 hour
  - Attractive for memory applications and temperature sensitive devices

CSAM Image



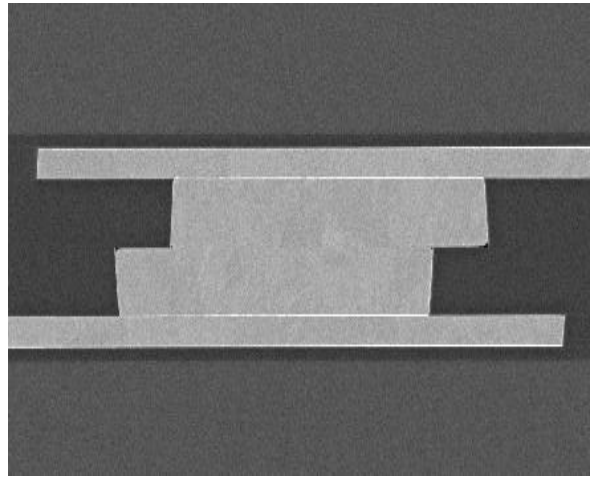
High Mag CSAM



Electrical Test Results

Build	Anneal Temperature (°C)	% Pass E-test
1	200	100
2A	200	100
2B	200	100
2C	200	100

Cross Sectional SEM

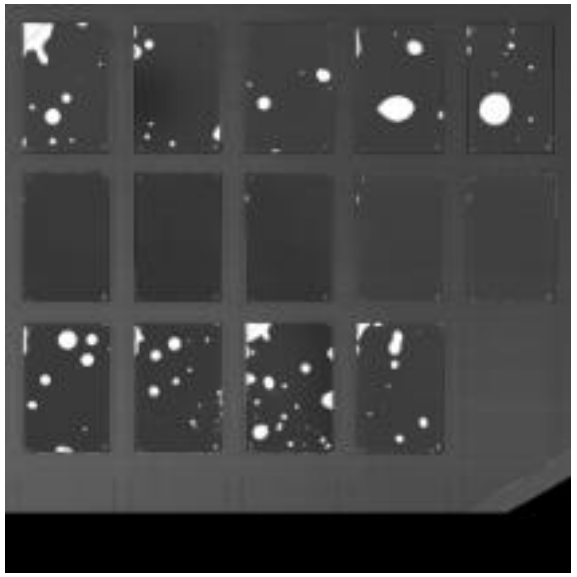


[1]G. Gao et al Xperi; C. Rudolph et al ASSID-IZM; "Low Temperature Cu Interconnect with Chip to Wafer Hybrid Bonding" ECTC 2019.

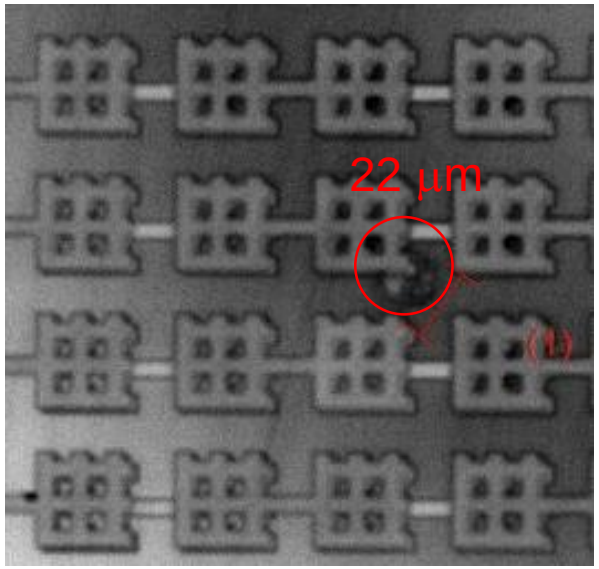
E-test Failure Modes

- Electrical failures are correlated ~100% to voids in the array
- IR optical inspection of voids predominantly shows a particle at the void center

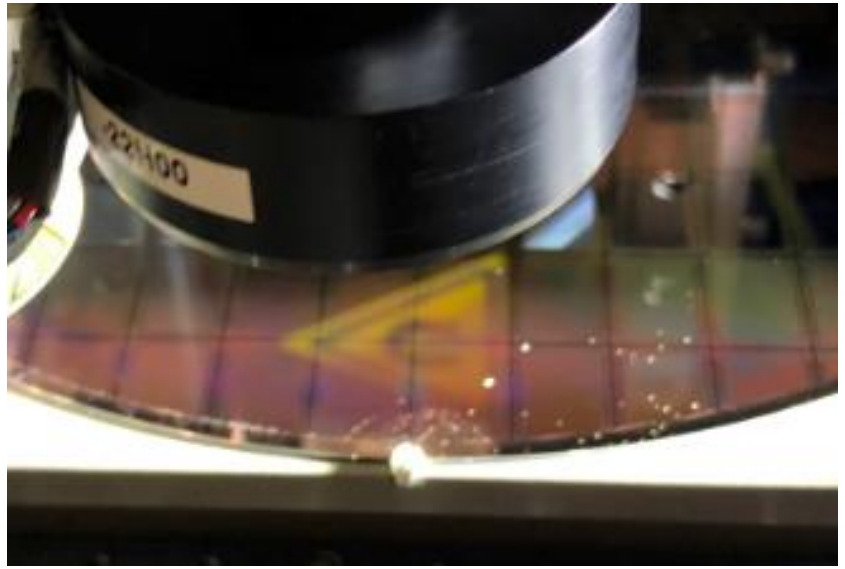
Example of yield excursion due to particulate



CSAM image of voids



IR Image of particle at center of void



Particles from bonder components

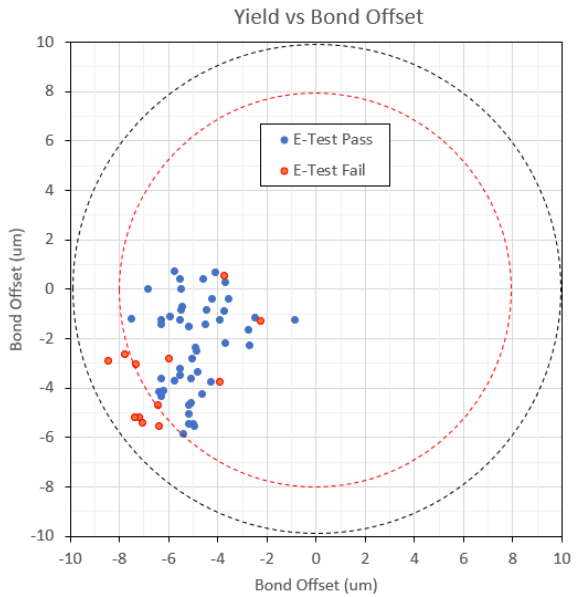
Effect of Misalignment on Electrical Yield and Resistance

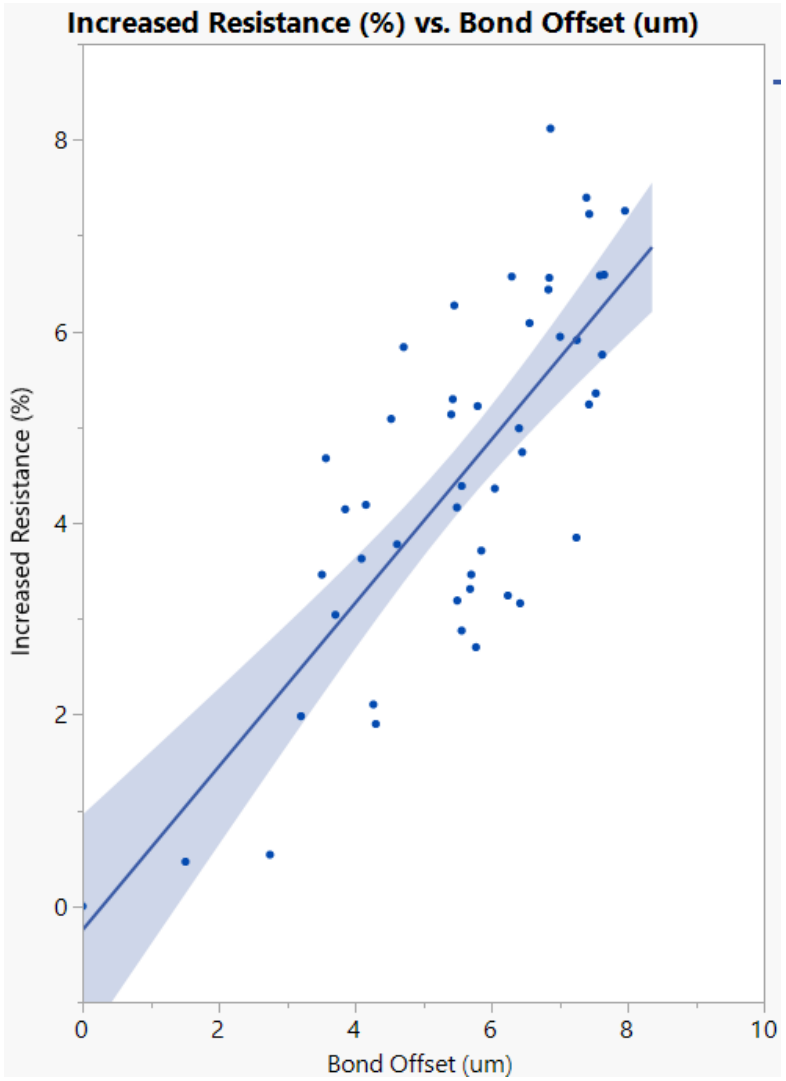
Process

- Introduce bond offset of 1 – 10 μm for 10 μm bond pad
- Observe yield and chain resistance of main array vs. offset

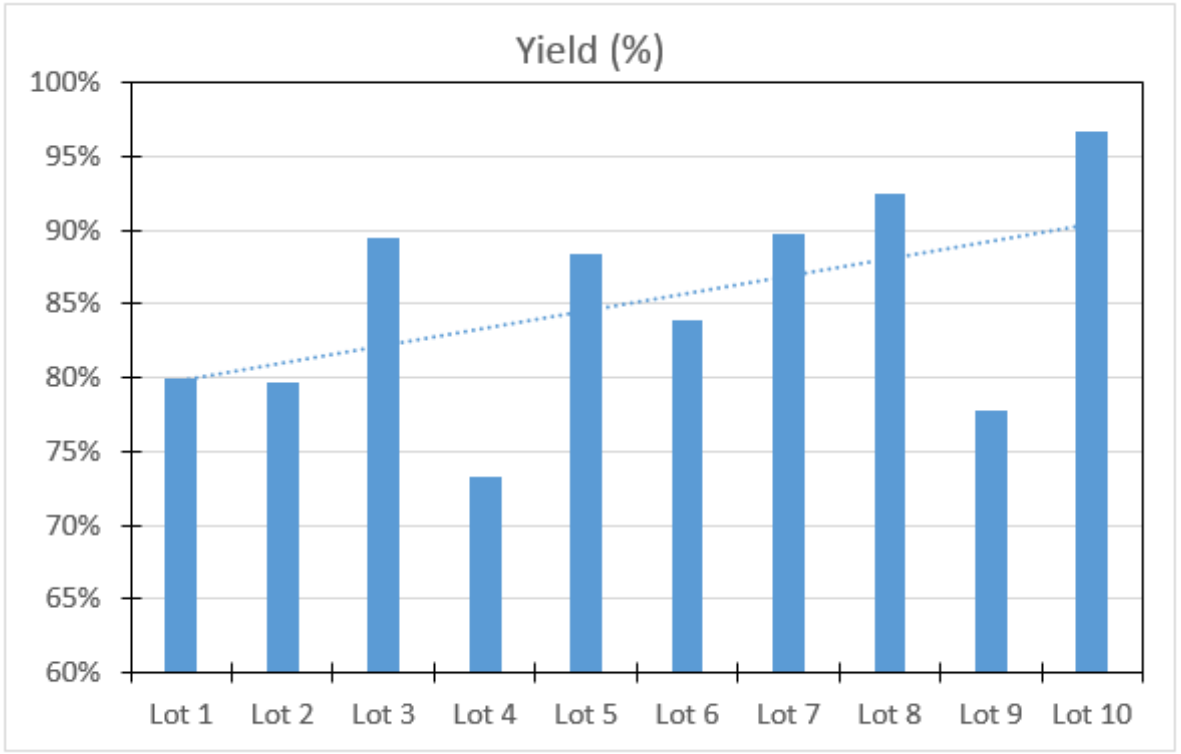
Results

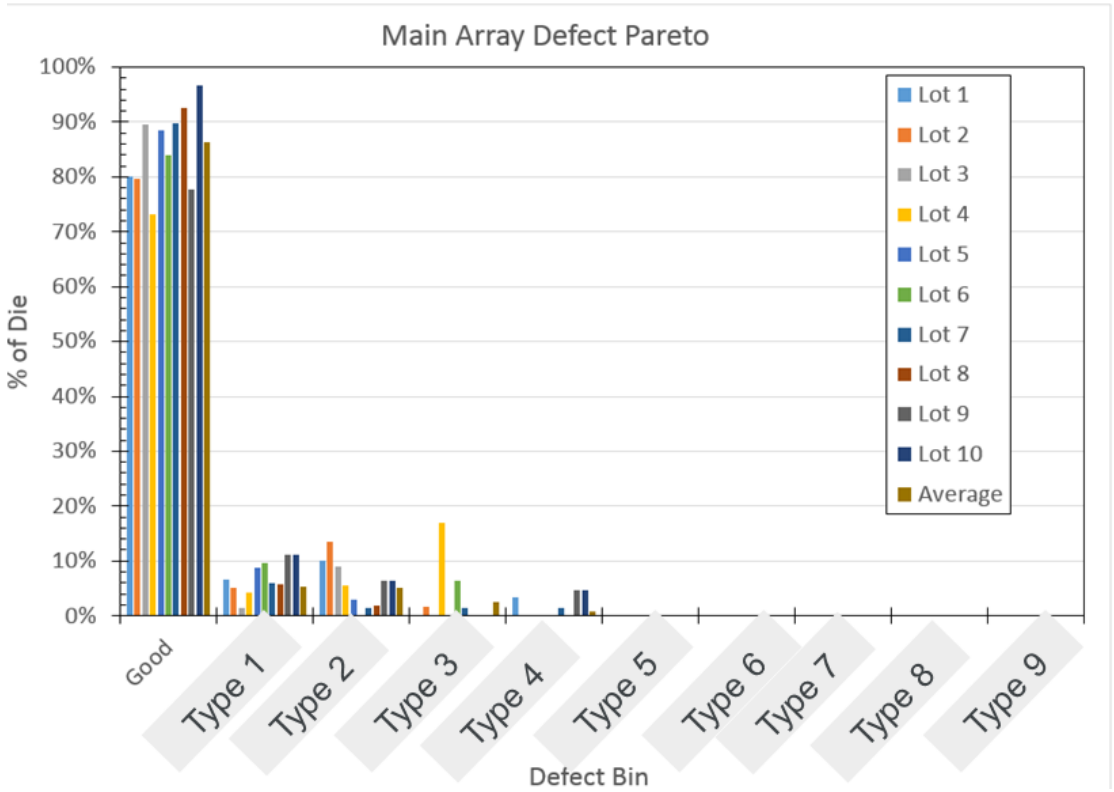
- No drop in yield for offsets up to 8 μm
- Increase in resistance:
  - Linear increase with offset
  - ~7% resistance increase at 8 μm offset
- Bonding is tolerant to significant offsets (80% of pad diameter)





Bond Yield Improvement for 200 μm Thick Die





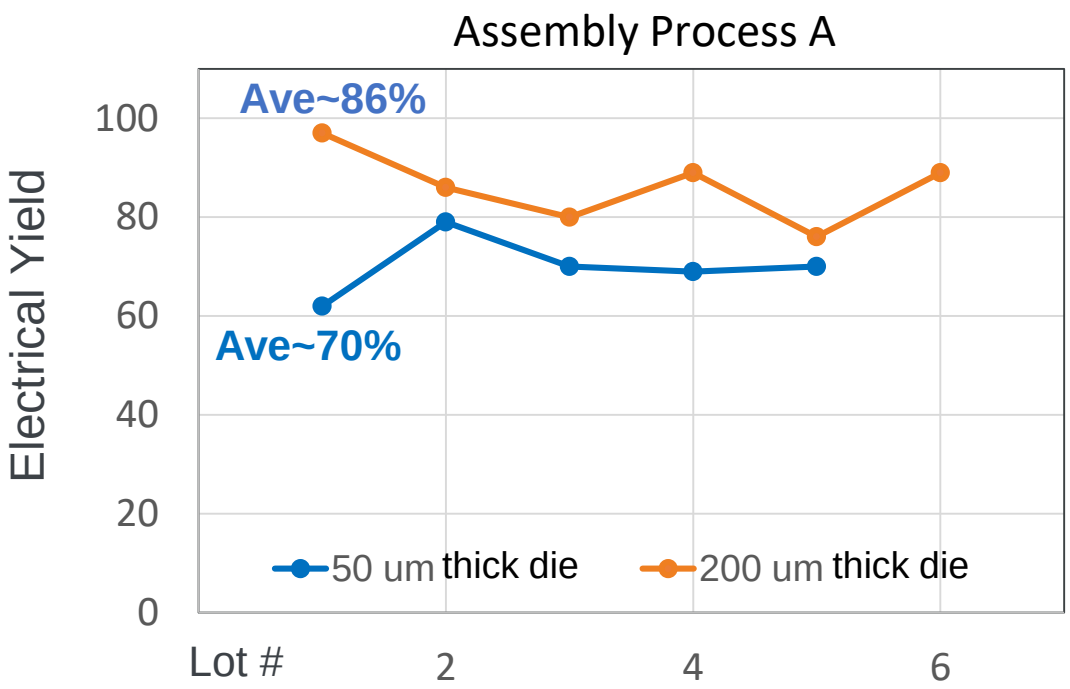
Process and Results

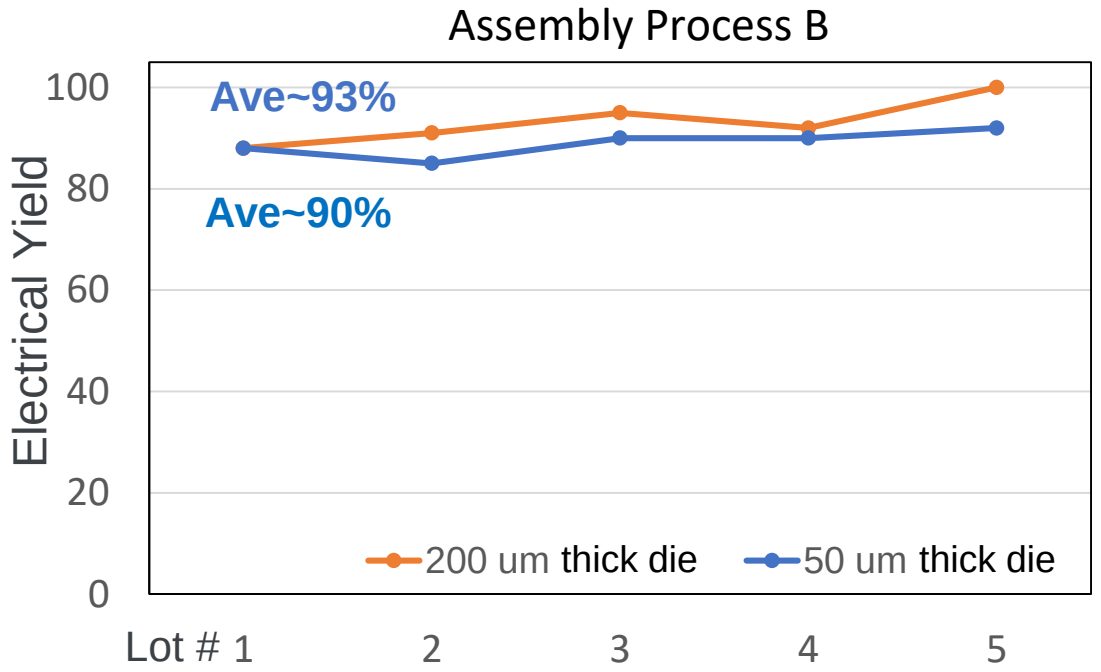
- E-test yield of 10 lots shown in time sequence
- Yield as high as 97% has been achieved in class 1K clean room with prototyping equipment

Learning – Key factors for yield improvements:

- Cleaning protocol
- Tooling design
- Equipment design and bond process

Bond Yield Improvement for Single Die Stack





Process and Results

- Categorize the new defect pareto for 50 μm thick die
- Understand root cause
- Find inventive solutions to reduce defects
- Yields as high as 100% achieved
- Closed the yield gap for thin die from 16 % to 3%

Die Stacking Yield Evaluation

Goal

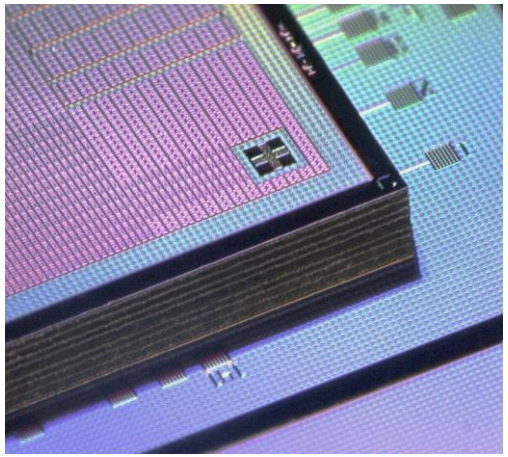
- Equivalent yield for each layer within the stack

Results:

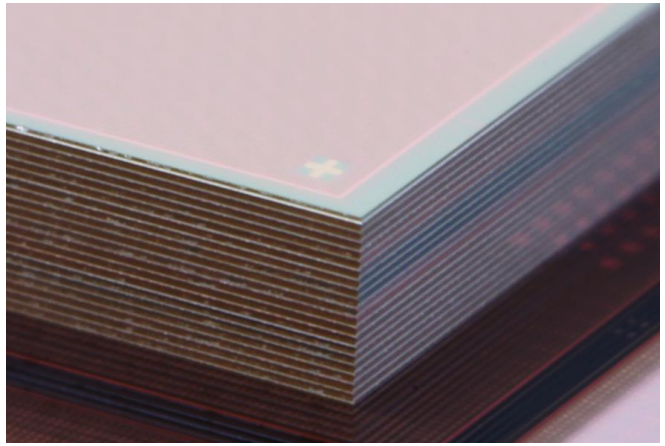
- Yield per layer of the 4-die stacks is roughly constant.
- Process improvements increase yield at each layer
- 20-die stack demonstrated

No show stoppers for stacking have been identified.

4-die stack



20-die stack



Summary

HVM Compatibility of DBI Ultra process has been demonstrated:

- CMP capability at bond pad sizes up to 15 μm
  - Uniform flatness and recess control
- Bond capability for 10 μm pad on 40 μm pitch
  - Thin die handling on tape (50 μm thick die)
  - Alignment and cleanliness support high yield (>90%)
  - All-Cu interconnect at 200˚C for 1 hour.
- All-Cu interconnects meet automotive reliability specifications

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