IN-PROCESS WARPAGE PREDICTION AND OPTIMIZATION FOR HETEROGENEOUSLY INTEGRATED PACKAGES USING A THERMO-MECHANICAL MODELING SCHEME

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Advanced Packaging

IMAPS DEVICE 2020

PACKAGING

Revolution of chiplets

Moore's law is slowing down

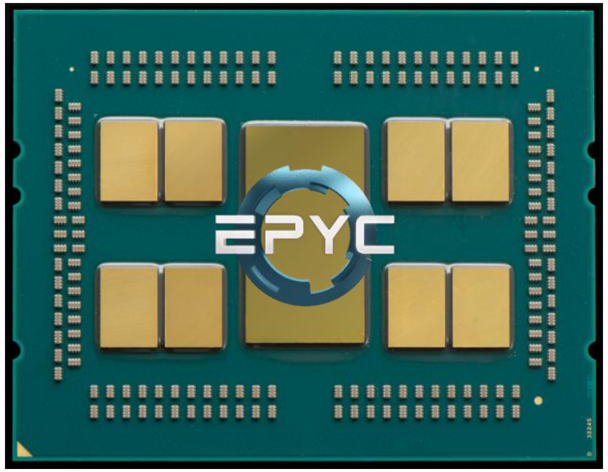
50 um
⋮
1 um
⋮
130 nm
⋮
14 nm
10 nm
7 nm
5 nm
3 nm
?

Gain in performance/cost is not promising

More than Moore

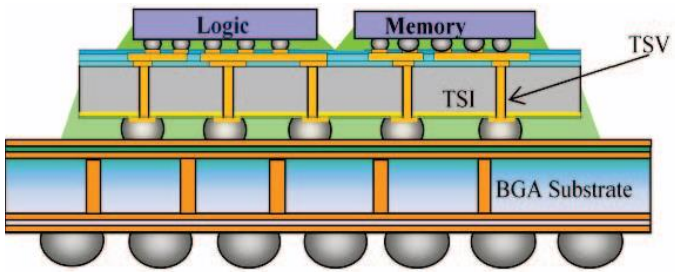
Chiplets of diverse technologies, functionalities

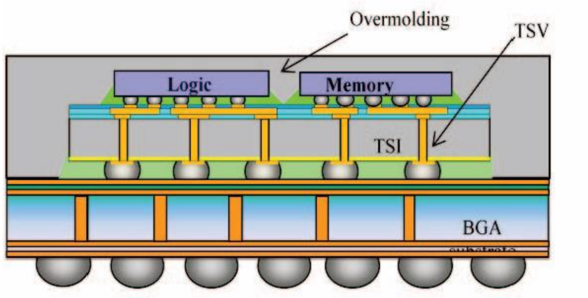
Heterogeneous integration

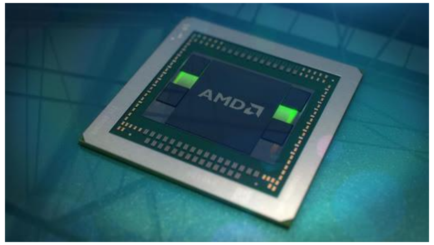


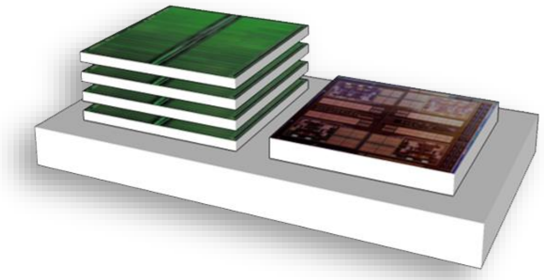
Chiplet integration requires efficient packaging schemes

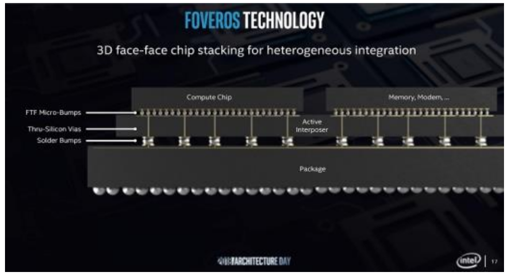
2.5D/3D packages





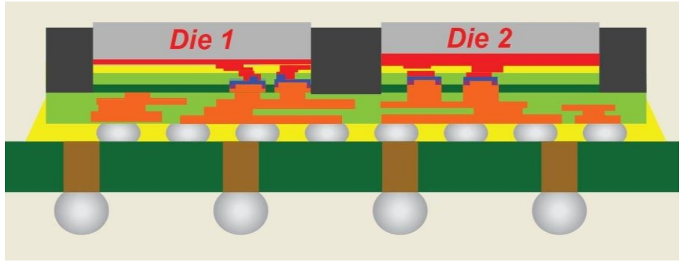


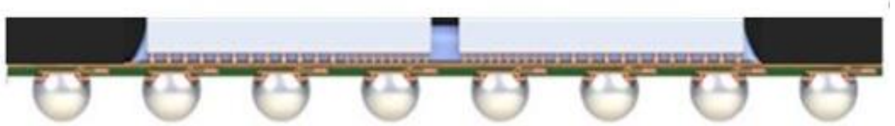



FOVEROS TECHNOLOGY

3D face-face chip stacking for heterogeneous integration

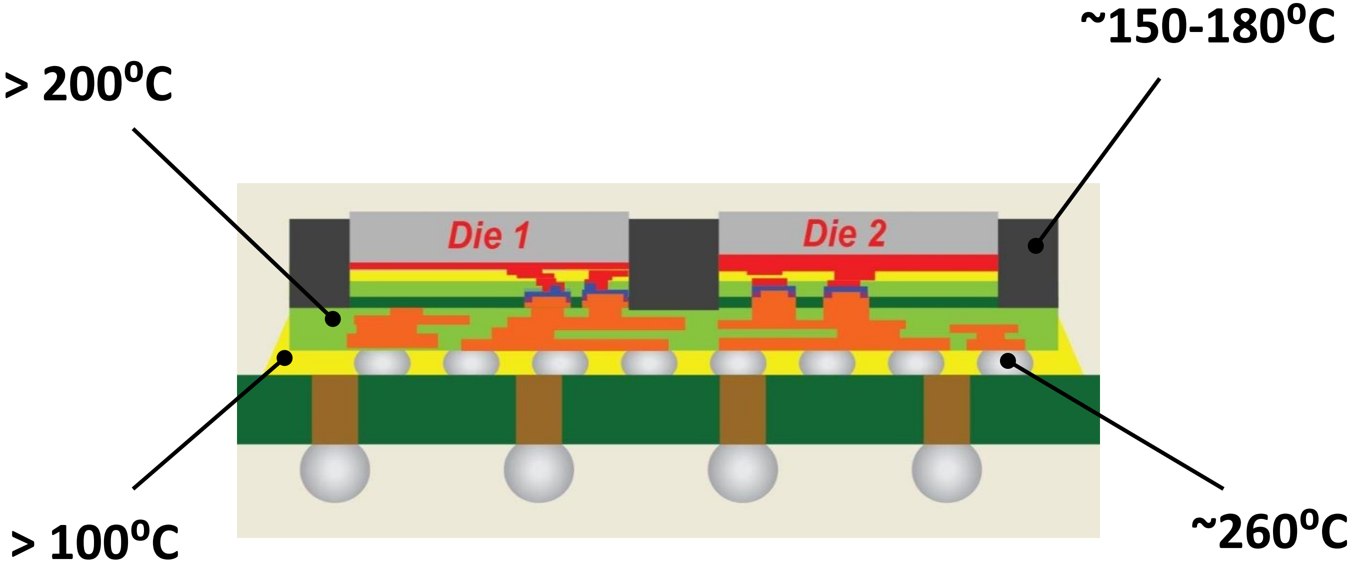
Fan-out packages





Source: online public platforms

Warpage control during package fabrication is a challenge



> 200^{o}C

~150-180^{o}C

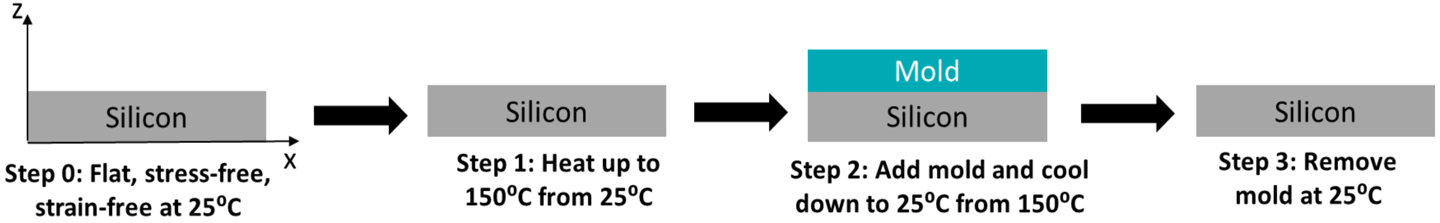
> 100^{o}C

~260^{o}C

- **Different processing steps have different thermal budgets**
- **Both wafer-level and package-level warpage is a challenge**

A reasonably accurate thermo-mechanical modeling could be helpful in process optimization

Thermo-mechanical modeling scheme for warpage prediction

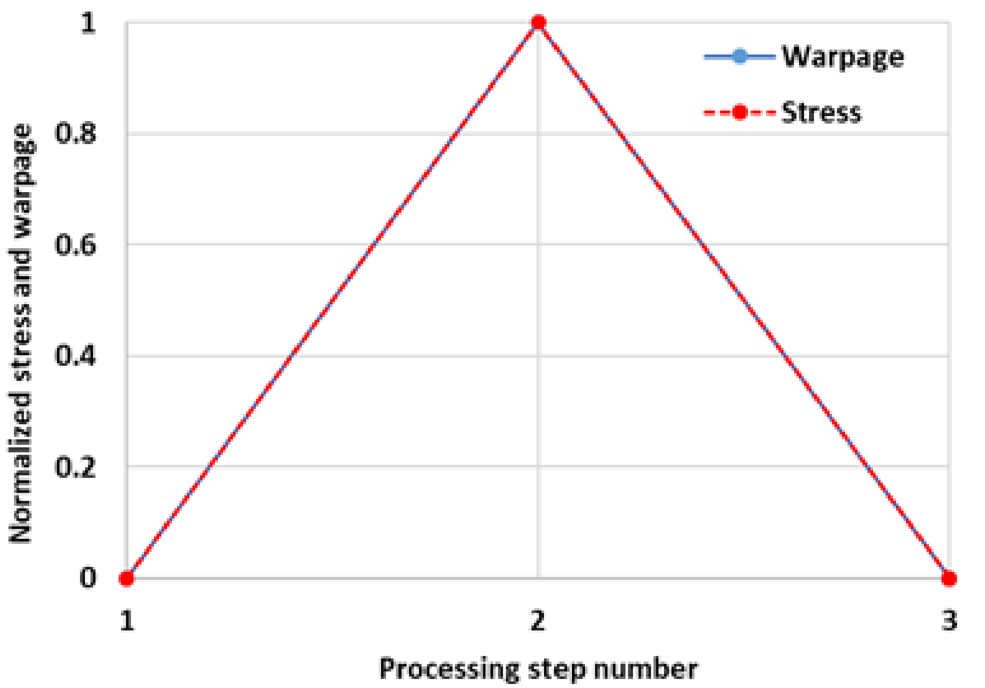


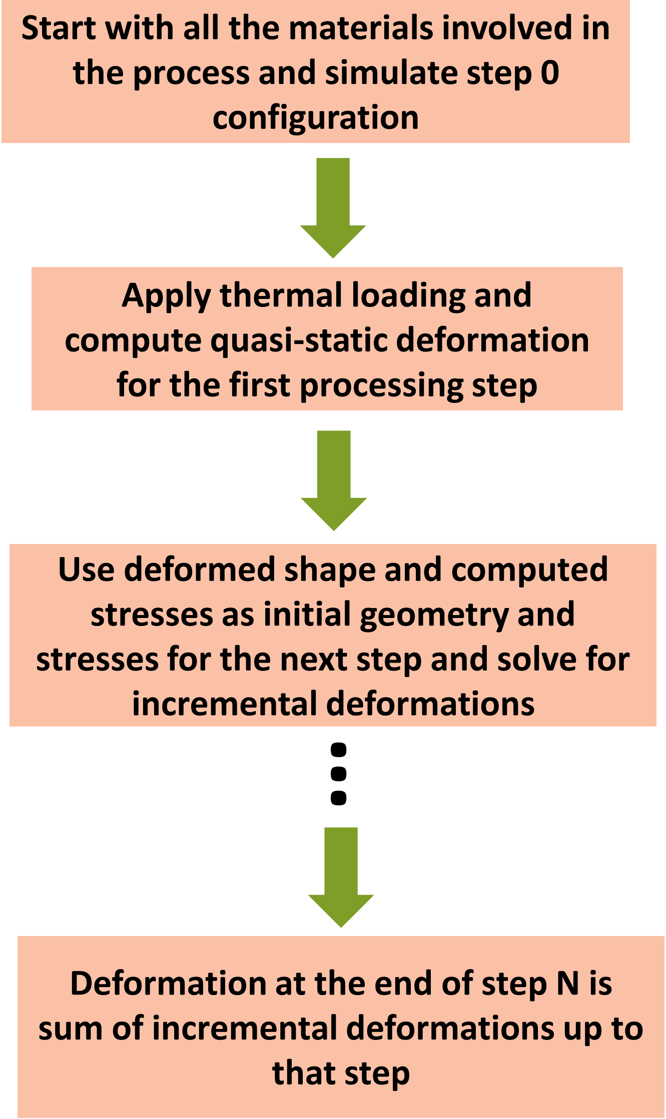
Step 0: Flat, stress-free, strain-free at 25°C

Step 1: Heat up to 150°C from 25°C

Step 2: Add mold and cool down to 25°C from 150°C

Step 3: Remove mold at 25°C





Start with all the materials involved in the process and simulate step 0 configuration

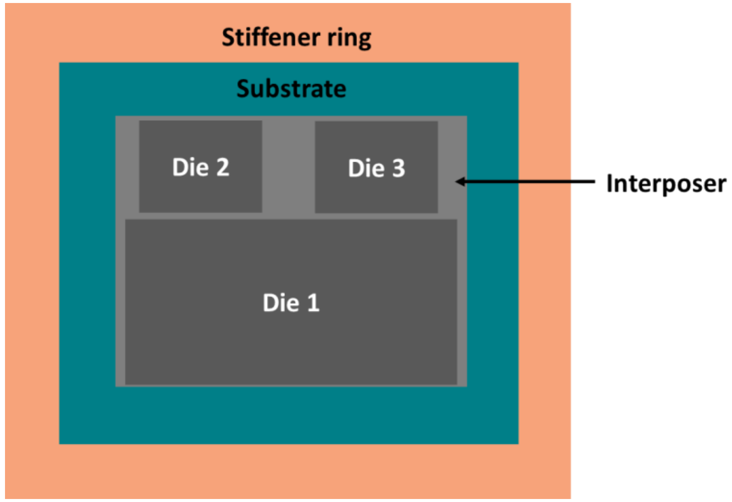
Apply thermal loading and compute quasi-static deformation for the first processing step

Use deformed shape and computed stresses as initial geometry and stresses for the next step and solve for incremental deformations

⋮

Deformation at the end of step N is sum of incremental deformations up to that step

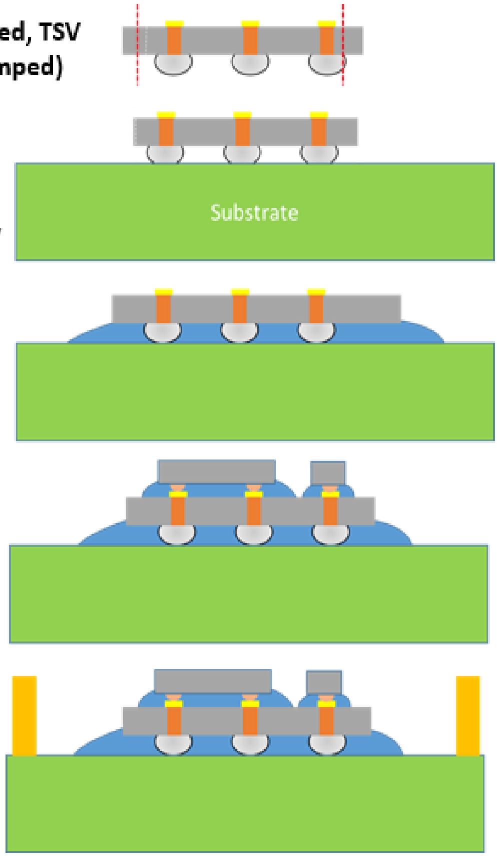
Example: 2.5D packaging



A typical 2.5D package

Objective: to predict and optimize warpage during the process

Chip on Substrate



Interposer (diced, TSV revealed, bumped)

Solder reflow for substrate assembly

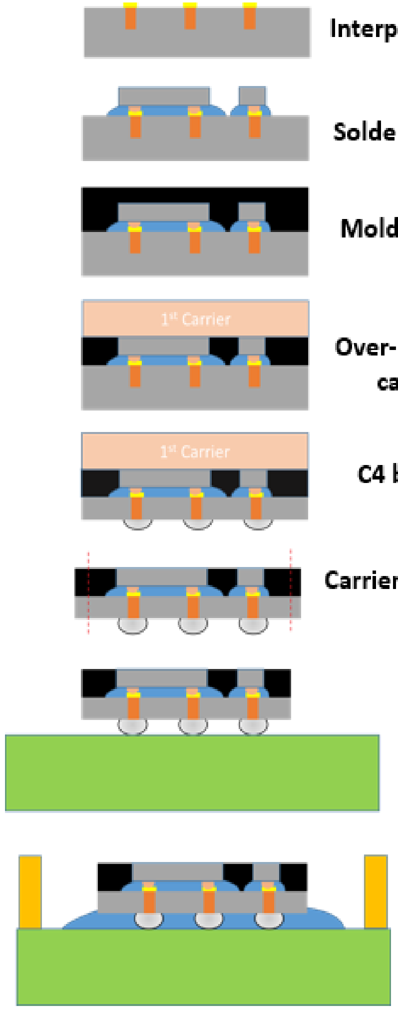
Under-filling

Solder reflow for chiplet dies attach

Stiffener ring attach

Ref: Amkor's 2.5D Package and HDFO-Advanced Heterogeneous Packaging Solution

Chip on Wafer on Substrate



Interposer wafer (TSV revealed)

Solder reflow for chiplet dies attach

Mold encapsulation

Over-mold grind and carrier attach

C4 bumping

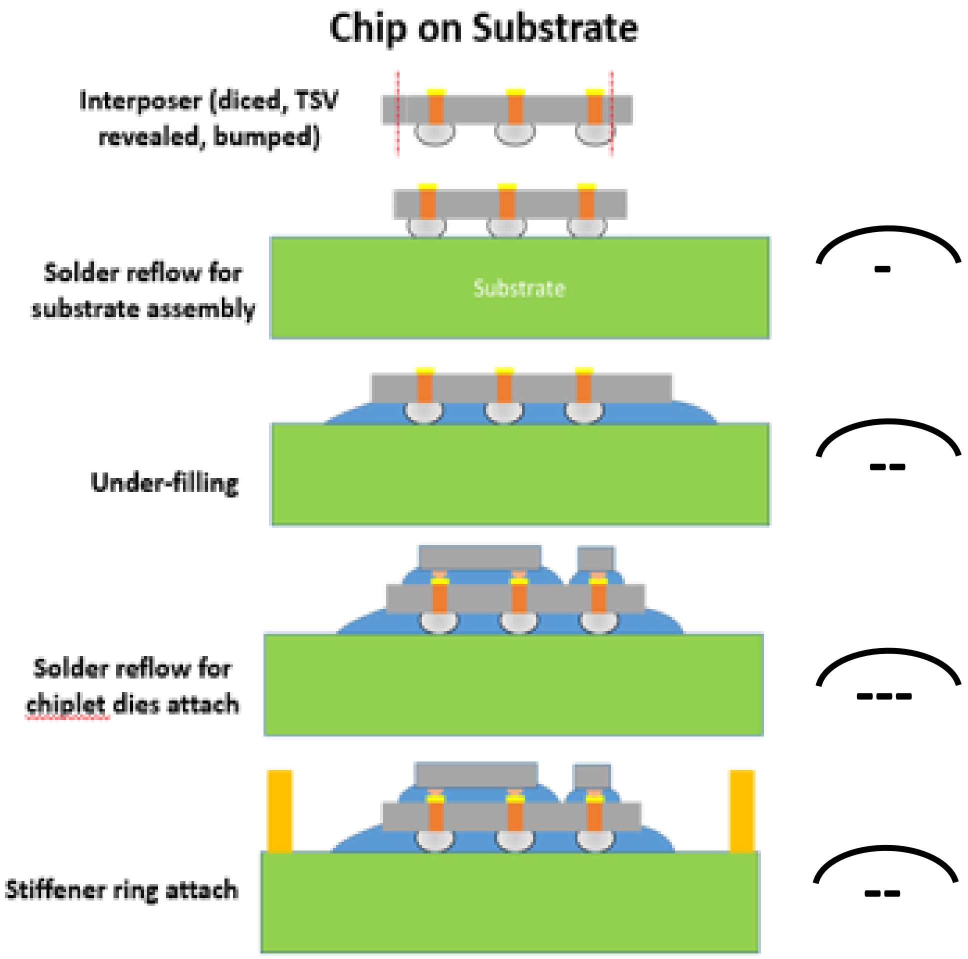
Carrier release and dicing

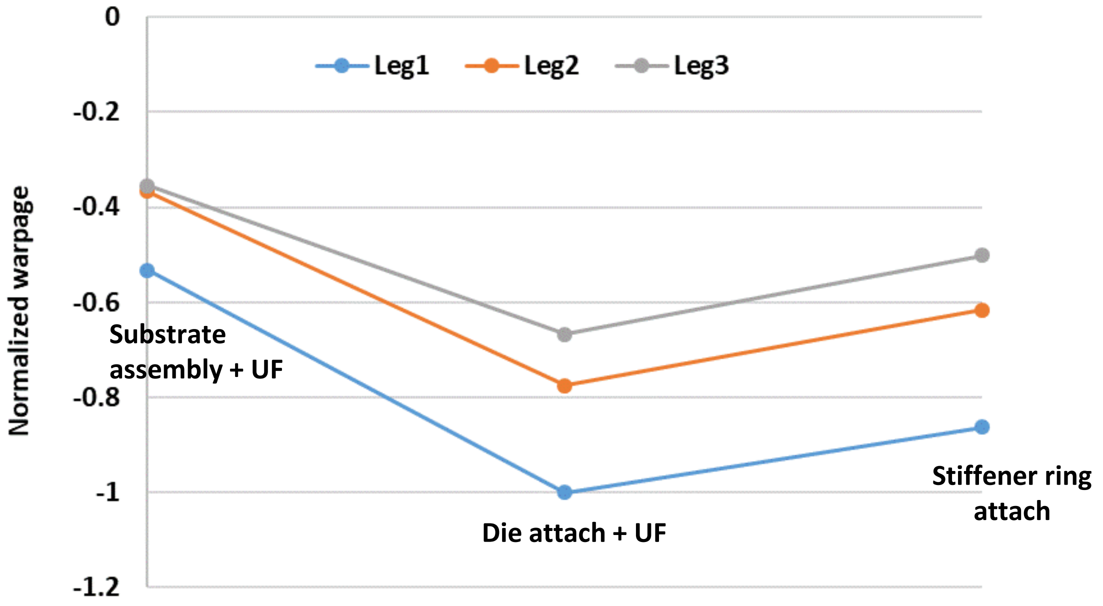
Solder reflow for substrate assembly

Stiffener ring attach

Ref: TSMC, ECTC 2013

CoS warpage





- Legs 1 to 3 involve different combination of substrate core and UF material
- Appropriate selection of material helps minimize warpage

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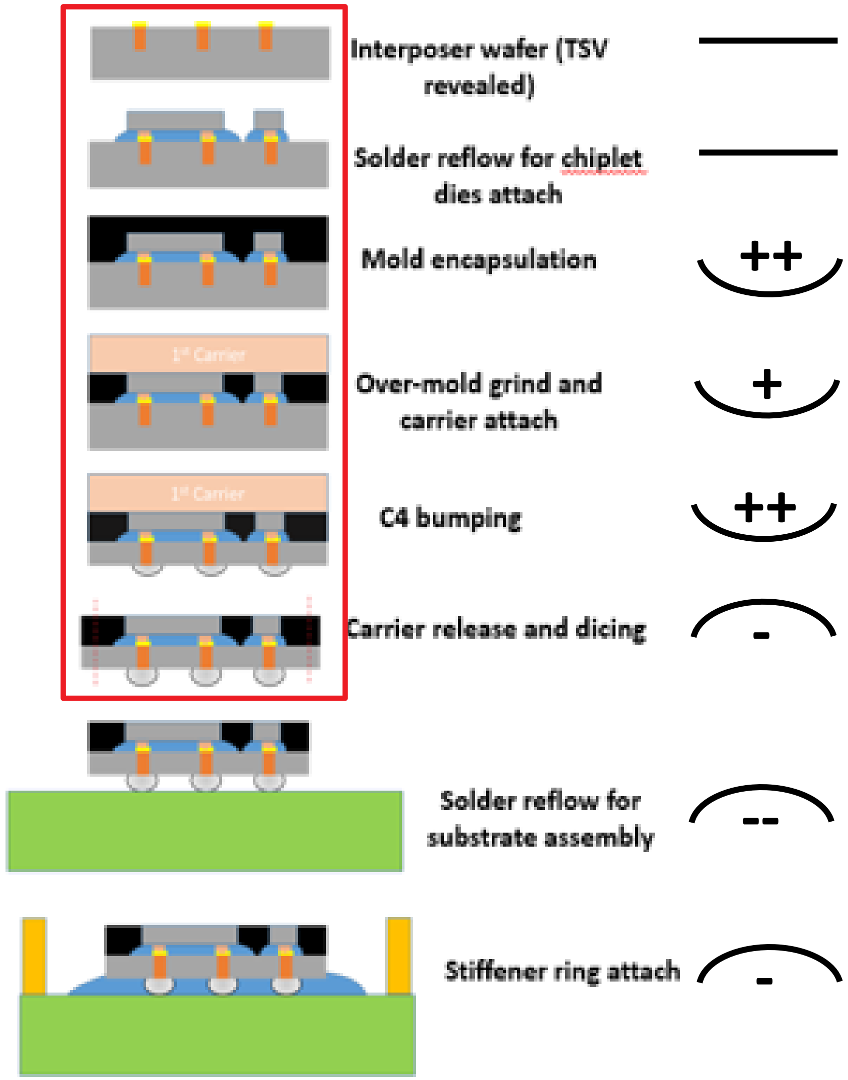
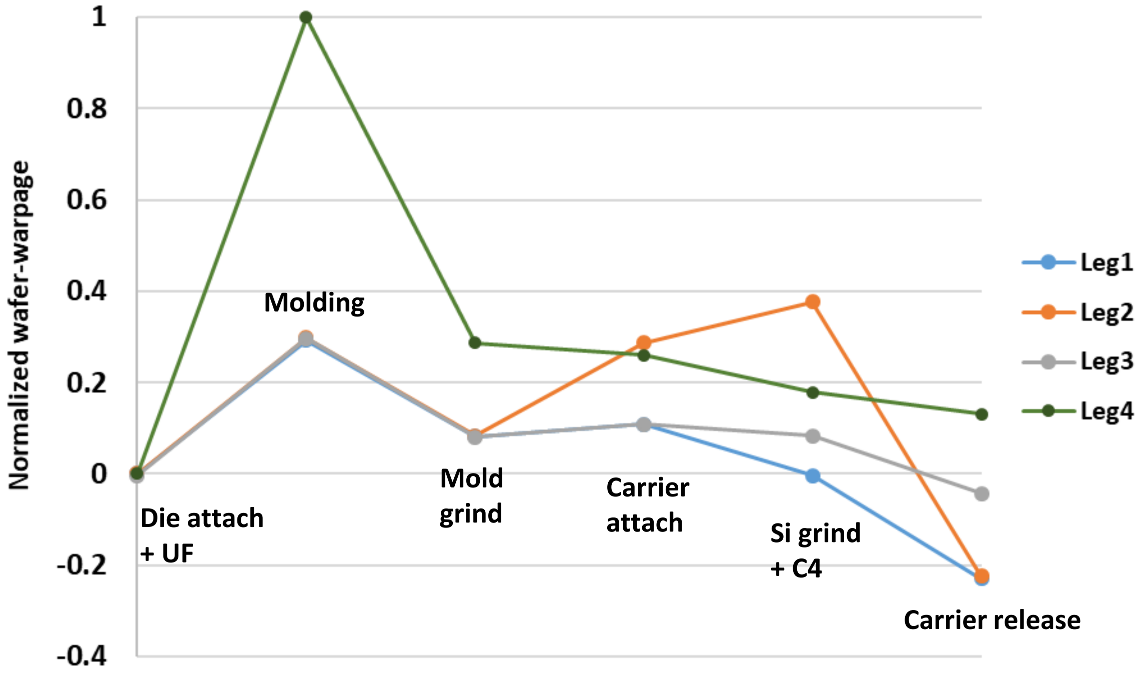
CoWoS warpage

Chip on Wafer on Substrate

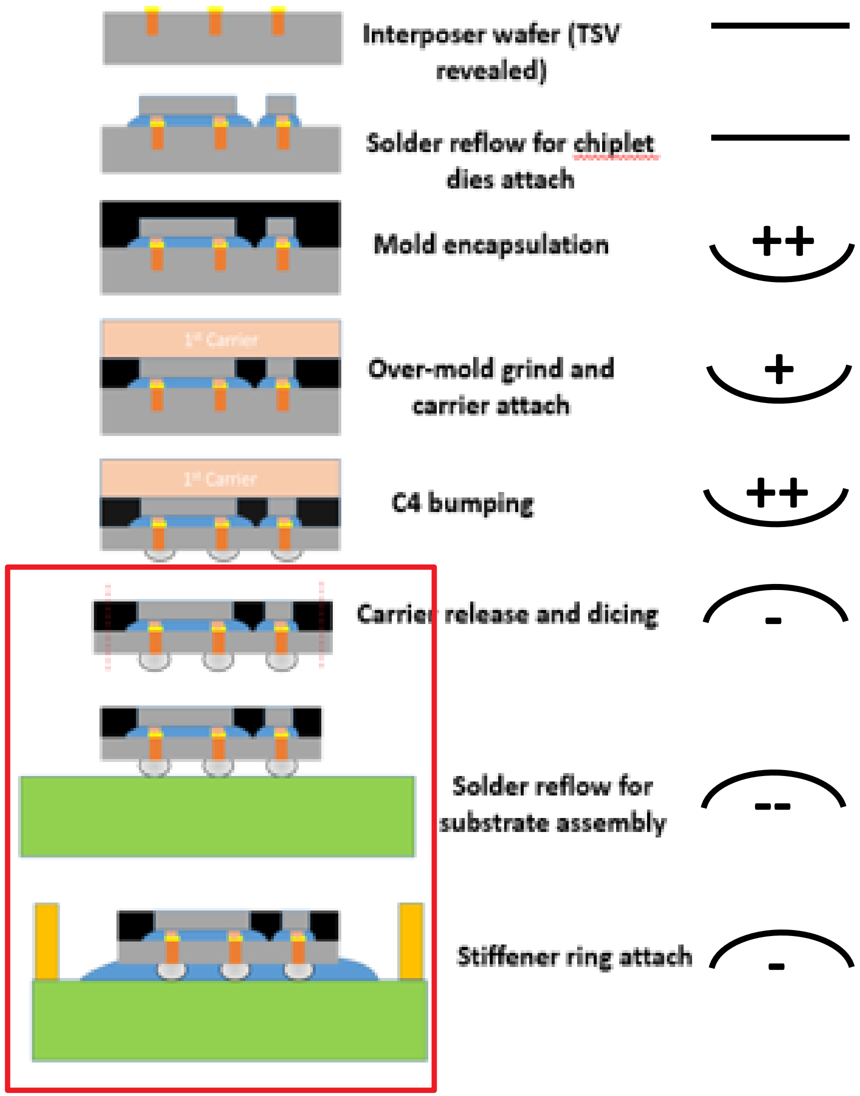


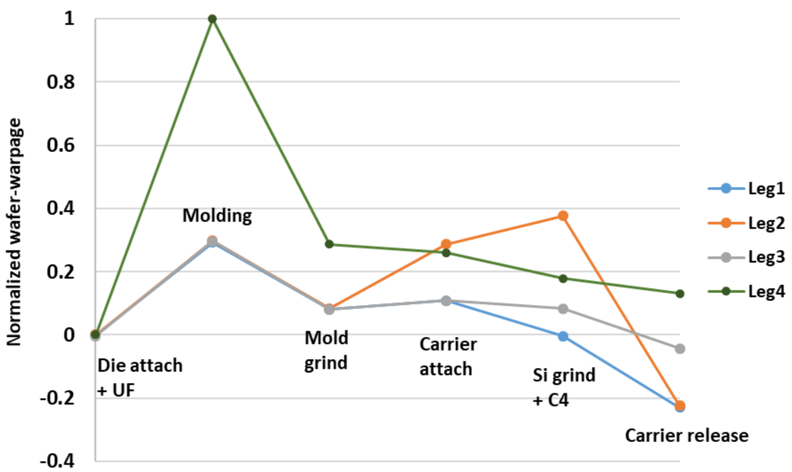


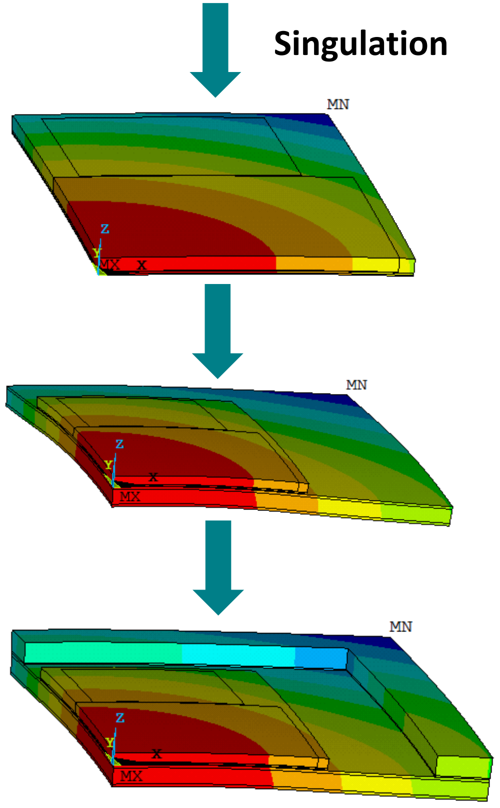
- **Legs 1 to 4 involve different combination of substrate core, UF and mold material**
- **Appropriate selection of material helps minimize warpage**

CoWoS warpage

Chip on Wafer on Substrate


Interposer wafer (TSV revealed)
Solder reflow for chiplet dies attach
Mold encapsulation
Over-mold grind and carrier attach
C4 bumping
Carrier release and dicing
Solder reflow for substrate assembly
Stiffener ring attach




Singulation

Summary

- A reasonably accurate thermo-mechanical analysis can provide useful insights into mechanics of packaging fabrication process
- This can help optimize the process parameters and provide guidelines on selection of appropriate materials for warpage control