Glass Interposers Using Cu-plated Through Glass Vias (TGVs)

Charles Woychik, Justin Borski and Robert Nead
i3 Microsystems, Inc.
9900 16th Street North
St. Petersburg, FL 33716
Email: Charles.Woychik@i3Microsystems.com

Outline

- Introduction
- Benefits of Glass for High Density Interconnects (HDI)
- Semi-Additive Plating (SAP)
- Through Glass Vias (TGVs)
- Glass Interposer
- Diplexer Module Build
- Electrical Characterization
- Thin Glass TGVs using a Cu bottom up fill process
- Summary

Outline

- Introduction
- Benefits of Glass for High Density Interconnects (HDI)
- Semi-Additive Plating (SAP)
- Through Glass Vias (TGVs)
- Glass Interposer
- Diplexer Module Build
- Electrical Characterization
- Thin Glass TGVs using a Cu bottom up fill process
- Summary

i3 Electronics

i3 Microsystems

i3 Microsystems, Inc. St. Petersburg, FL

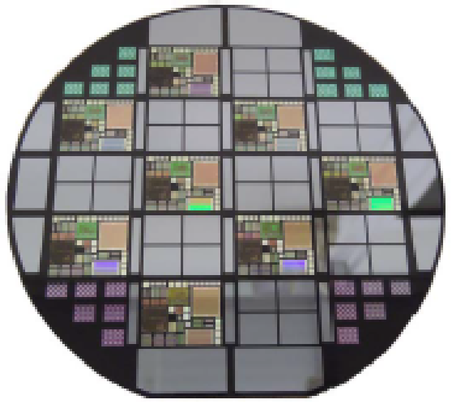
Privately held, electronic manufacturing provider of innovative products and solutions with differentiated technology.

i3 Electronics

i3 Microsystems

Microsystems | Overview

i3 microsystems



Microfabrication Production

- Heterogeneous System-in-Package (HSIP)
- Fan-Out Wafer Level Packaging (FOWLP)
- Die Extraction / Recovery Services

Secure Facility

- Secret level
- DMEA Category 1A Trusted Foundry

40,000 Sq Ft Facility

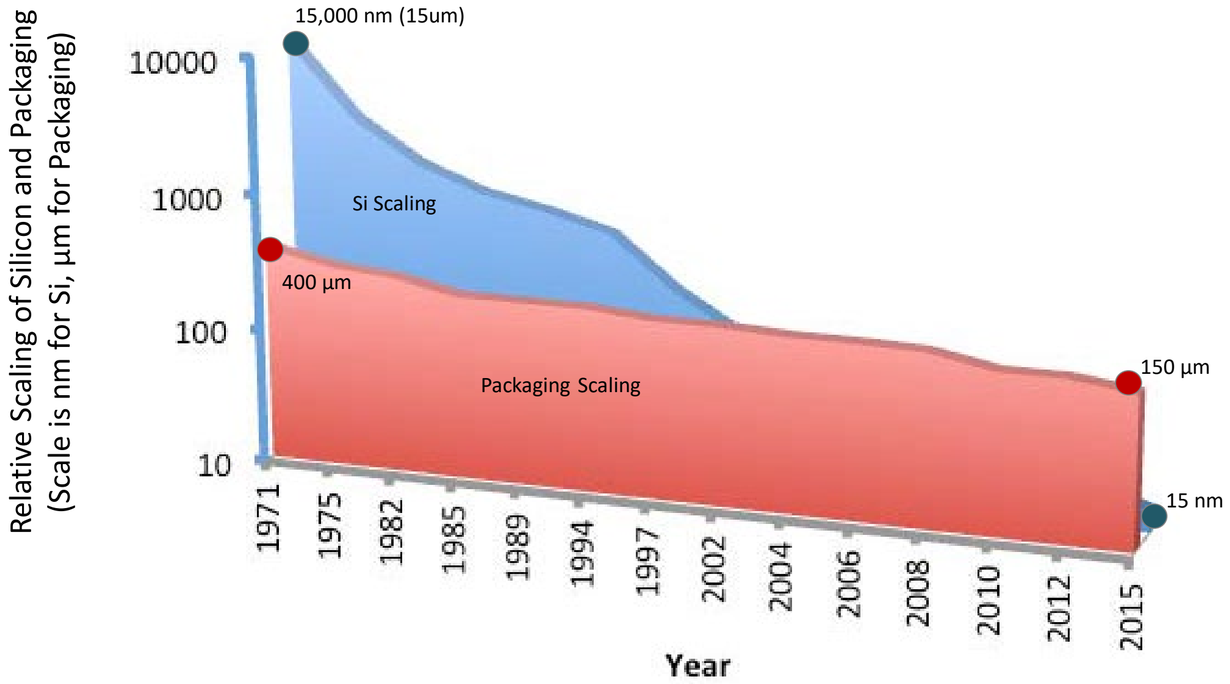
- 600 Sq Ft Class 10 Cleanroom
- 7,000 Sq Ft Class 100 Cleanroom
- 10,000 Sq Ft Class 1000 Cleanroom

Outline

- Introduction
- Benefits of Glass for High Density Interconnects (HDI)
- Semi-Additive Plating (SAP)
- Through Glass Vias (TGVs)
- Glass Interposer
- Diplexer Module Build
- Electrical Characterization
- Thin Glass TGVs using a Cu bottom up fill process
- Summary

i3 Electronics

Drivers for HDI Packaging



Si has scaled by 1000x over time, while packaging features have scaled by only a factor of 3-5x..

Reference: Prof. S.S. Iyer UCLA

i3 Electronics

Comparison of Different Types of Interposers

Ideal Properties of a Package Material

Characteristic	Materials				
	Ideal Properties	Glass	Silicon	Organic	Metal
Electrical	• High resistivity • Low loss				
Physical	• Smooth surface finish • Large area availability • Ultra thin				
Thermal	• High Conductivity • CTE matched to Si				
Mechanical	• High strength • High modulus				
Chemical	• Resistance to process chemicals				
Processability	• Ease of Via formation and metallization				
Cost	• Low cost per I/O at 25um pitch				

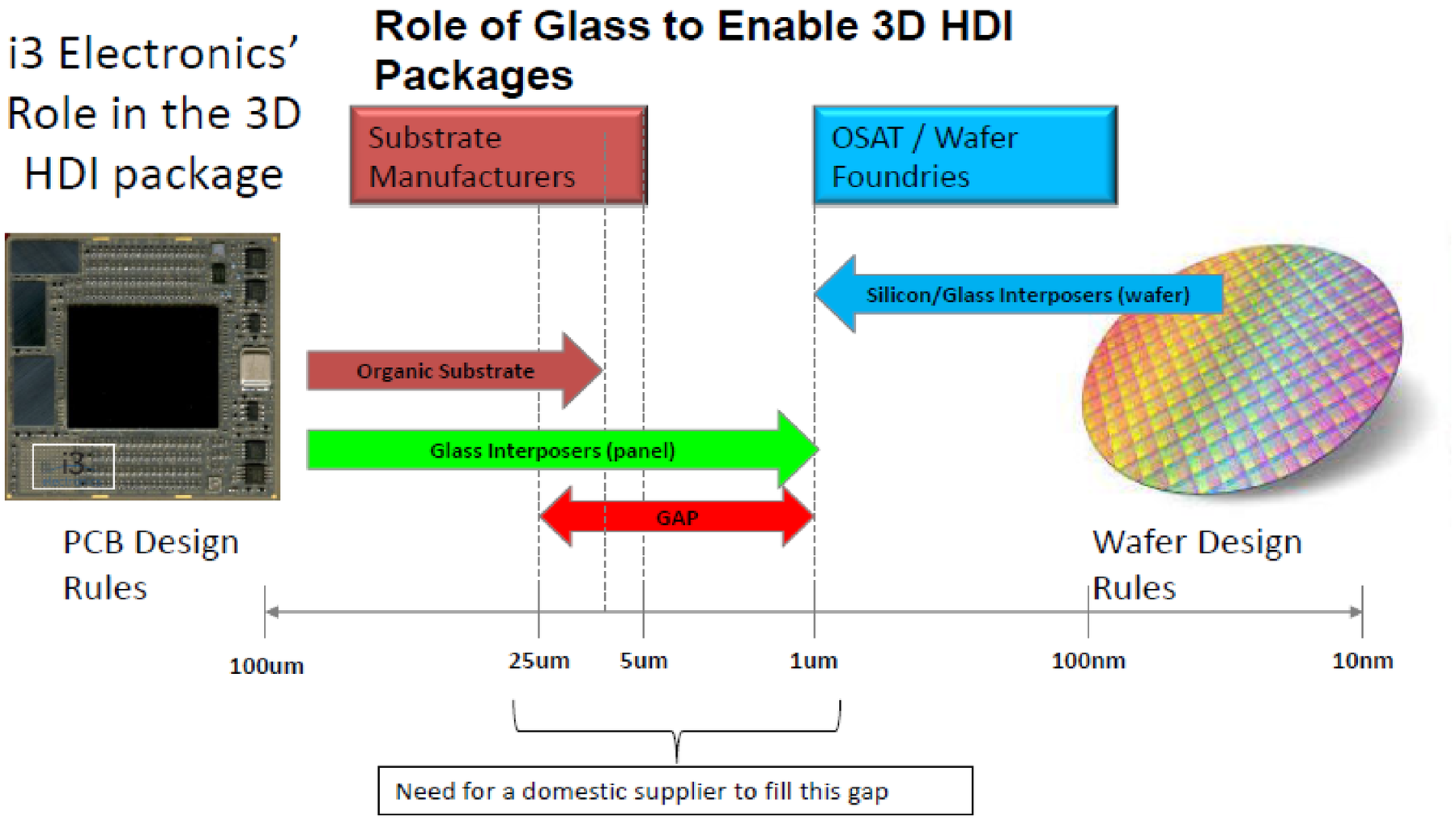
Good Fair Poor

Page 7

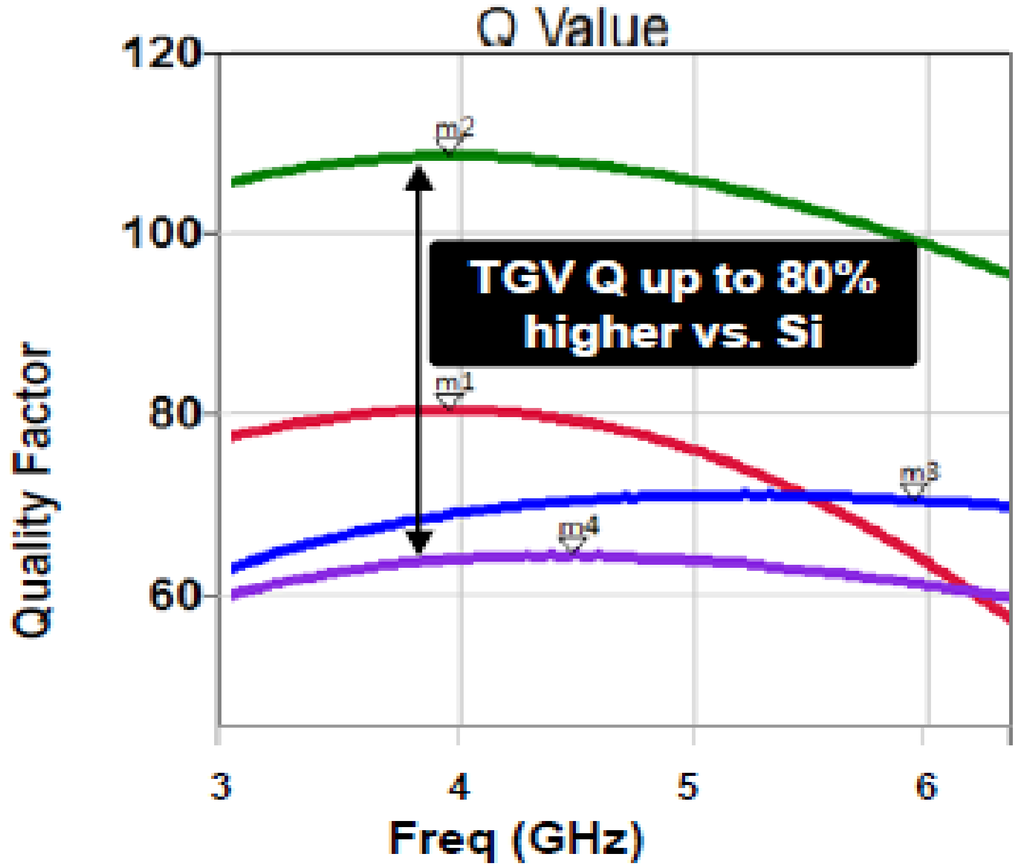
Georgia Institute of Technology

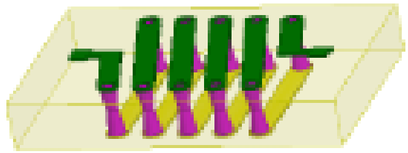
i3 Electronics

Role of Glass to Enable 3D HDI Packages



i3 Electronics

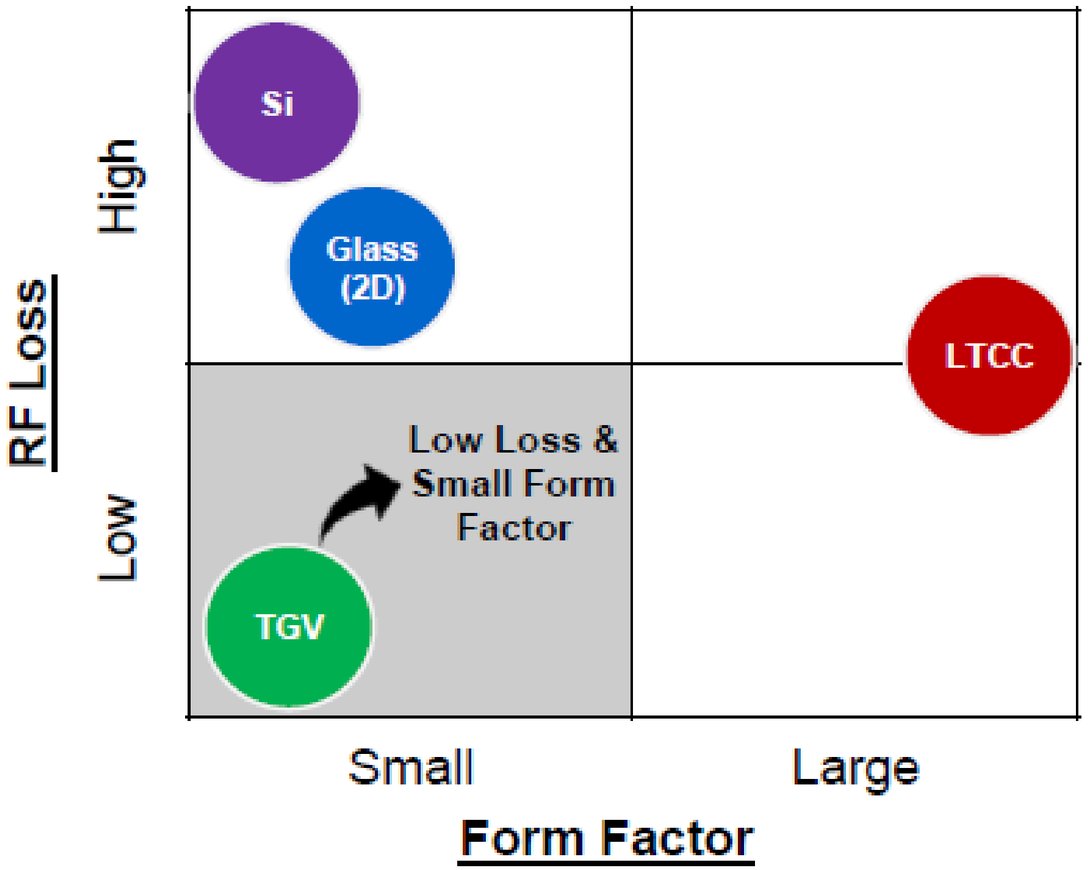




TGV Inductor

80% higher Q (lower RF loss) vs. Si

i3 Electronics



5-10X more components, same footprint

- Smaller thinner components→ slim devices

i3 Electronics

Outline

- Introduction
- Benefits of Glass for High Density Interconnects (HDI)
- Semi-Additive Plating (SAP)
- Through Glass Vias (TGVs)
- Glass Interposer
- Diplexer Module Build
- Electrical Characterization
- Thin Glass TGVs using a Cu bottom up fill process
- Summary

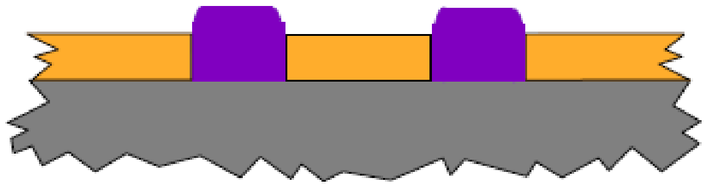
i3 Electronics

Comparison of Substantive Etch vs. Semi-Additive Plating

Wet Chemical Etch Subtractive Process (Isotropic Etching)

Not well suited for fine feature definition.

Semi-Additive Plating (Pattern Plating)



Well suited for fine feature definition.

i3 Electronics

Semi Additive Plating (SAP)

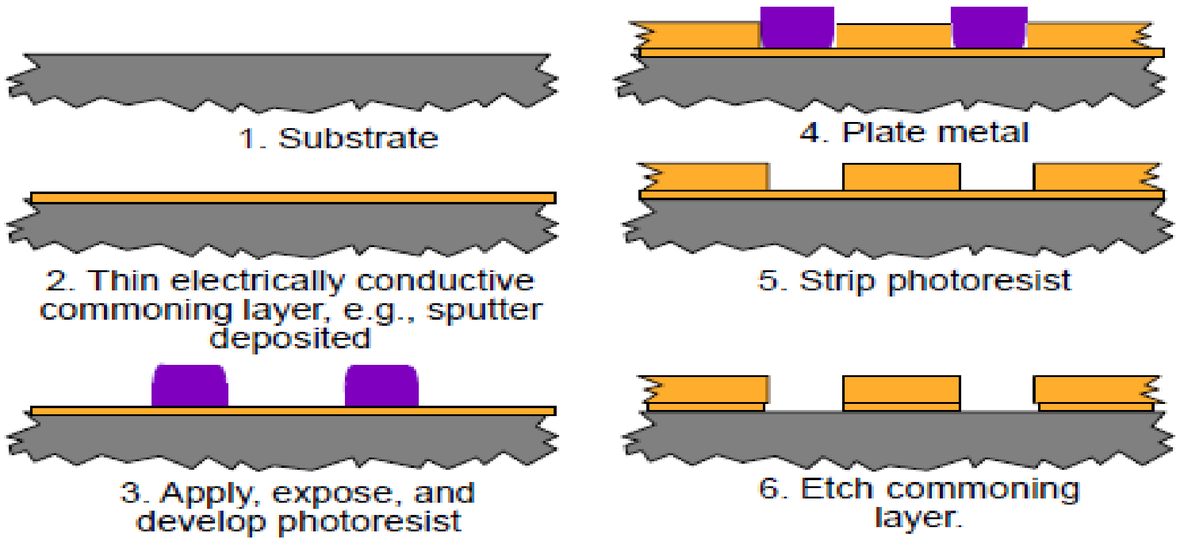


Figure 5(a)

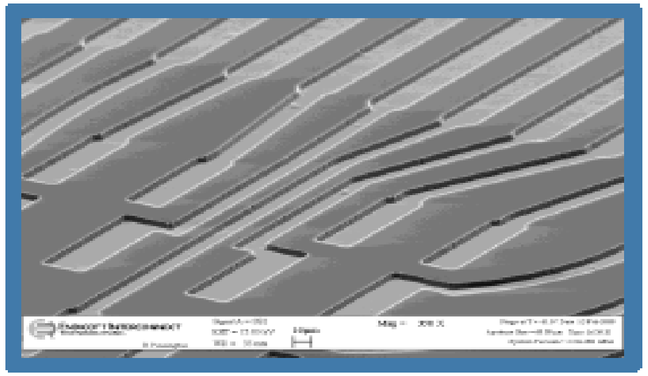


Figure 5(b)

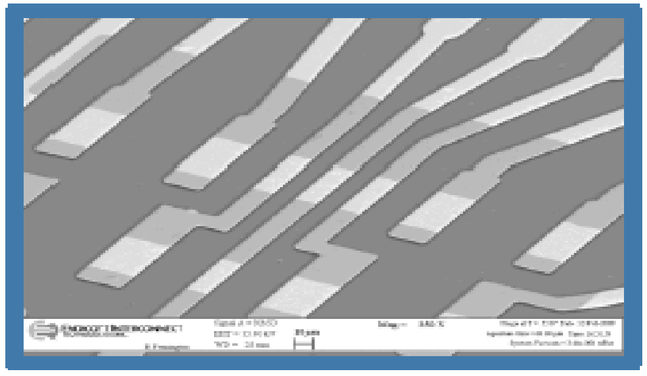


Figure 5(c)

i3 Electronics

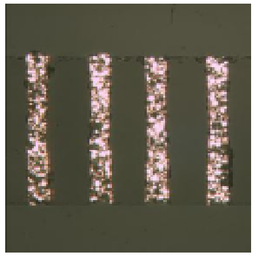
Outline

- Introduction
- Benefits of Glass for High Density Interconnects (HDI)
- Semi-Additive Plating (SAP)
- Through Glass Vias (TGVs)
- Glass Interposer
- Diplexer Module Build
- Electrical Characterization
- Thin Glass TGVs using a Cu bottom up fill process
- Summary

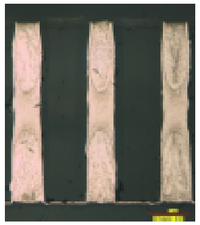
i3 Electronics

Approaches to Create a Conductive TGV

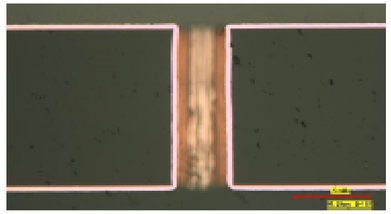
Electrically Conductive
Paste Filled Via



Plated Cu Filled Via



Conformal Cu Plated Via

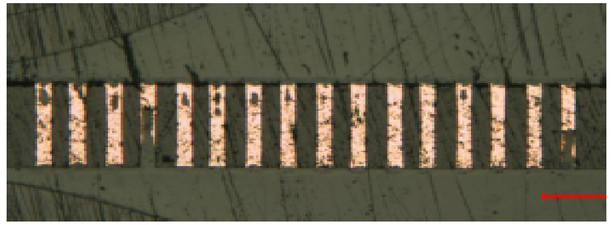


i3 Electronics

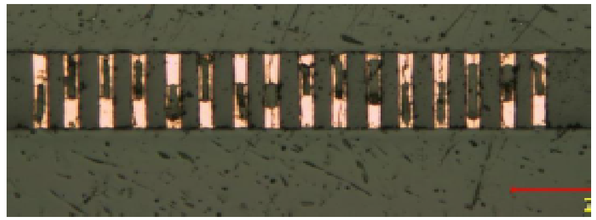
Electrically Conductive Adhesives to form a TGV – Using optimized parameters

Run 1: normal parameters
Run 2 lower paste pressure
Run 3: lower paste pressure, faster speed and 1 pass

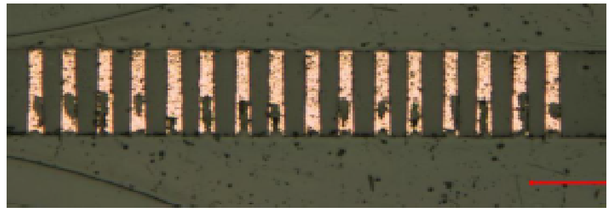
Run 1



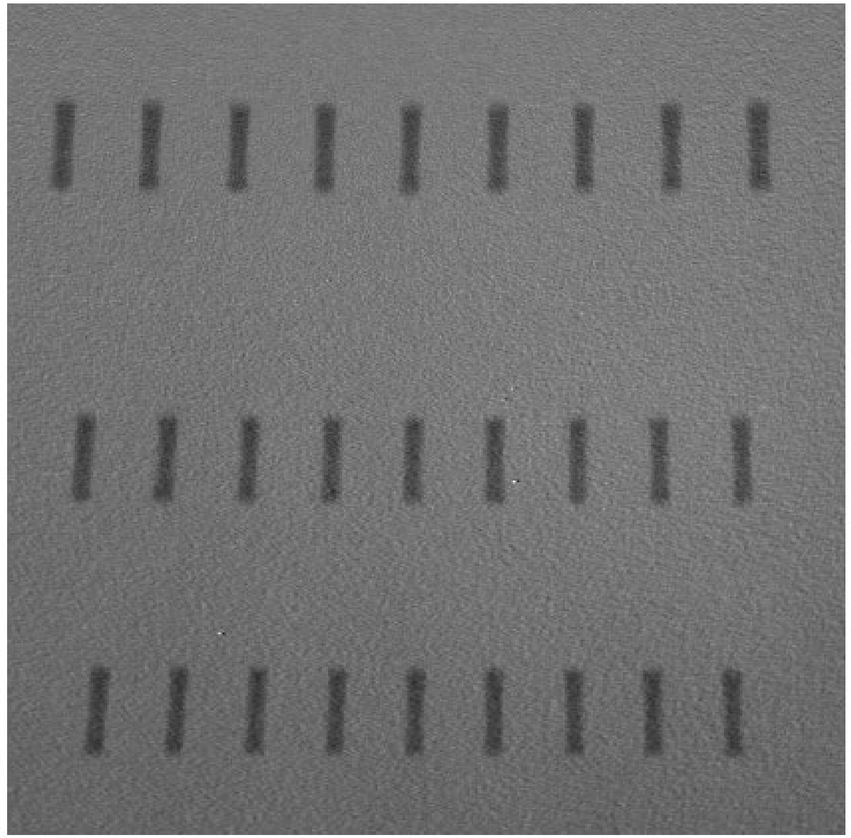
Run 2



Run 3

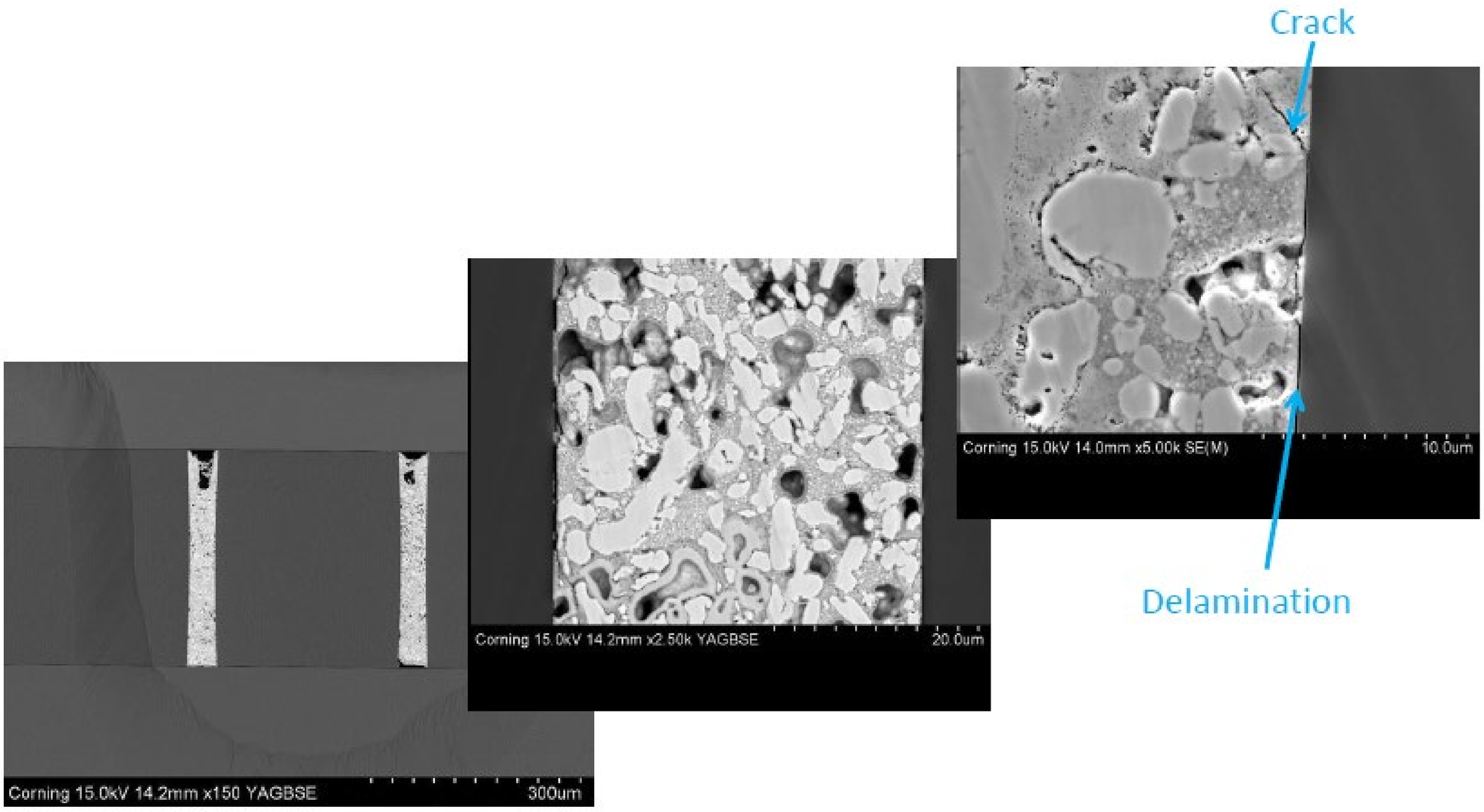


Optimized Parameters



i3 Electronics

ECA Filled Glass Vias

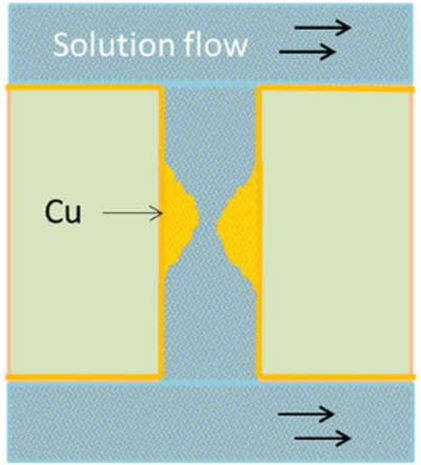


i3 Electronics

Work at Binghamton University on Cu-Filled TGVs

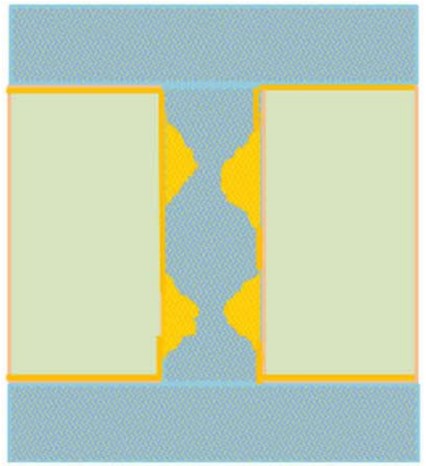
Case 1: desired plug formation.

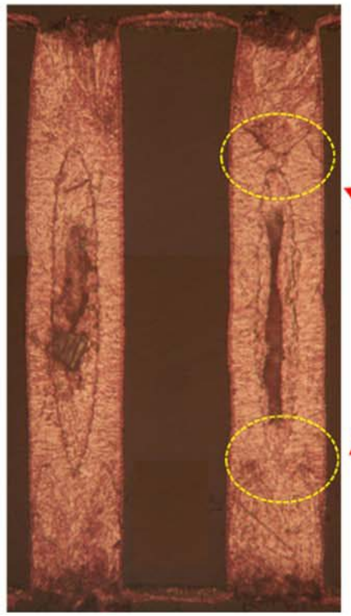
Plating is inhibited except at middle of hole.



Good single plug formation.

Case 2: Void formation when zone of inhibition does not extend far enough into hole, or current density is too high. Plating grows together in two regions creating a void.



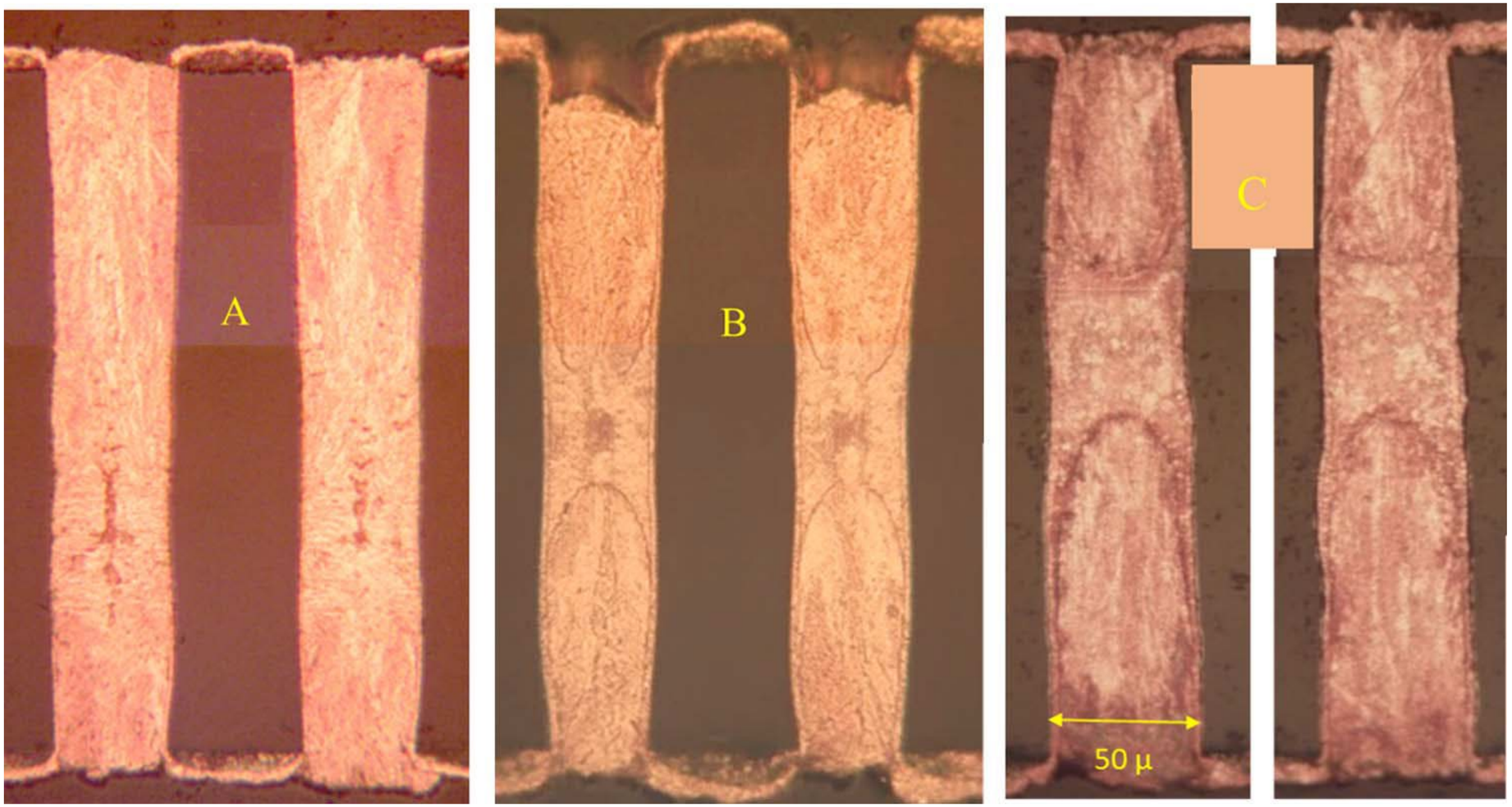


Plating grows together, seals in void.

Reference: Prof. N. Dimitrov – Binghamton University

i3 Electronics

Work at Binghamton University on Cu-Filled TGVs



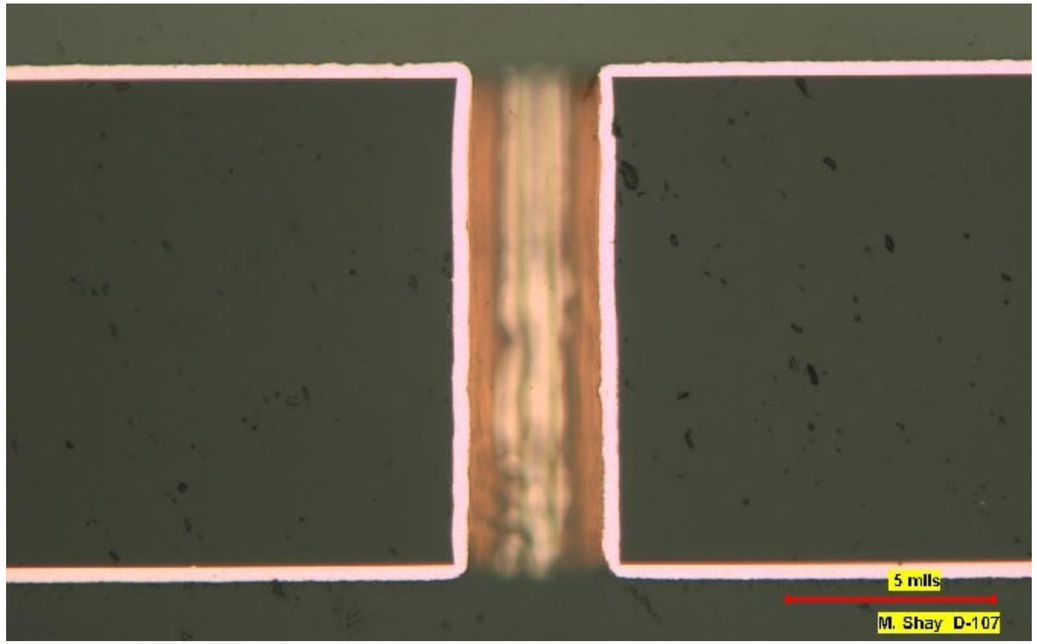
Imperfections in Middle of Via for Cases A and B

Well Plugged Via for Case C

Reference: Prof. N. Dimitrov – Binghamton University

i3 Electronics

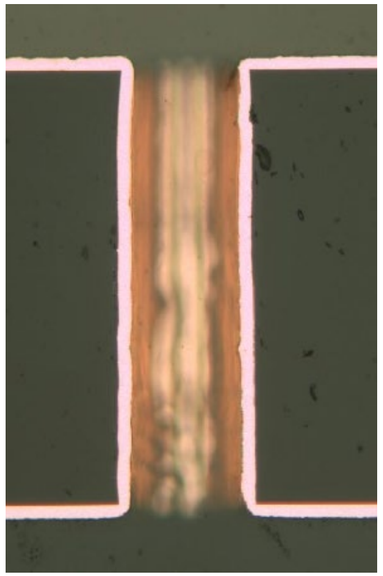
i3's Conformal Cu-Plated TGV

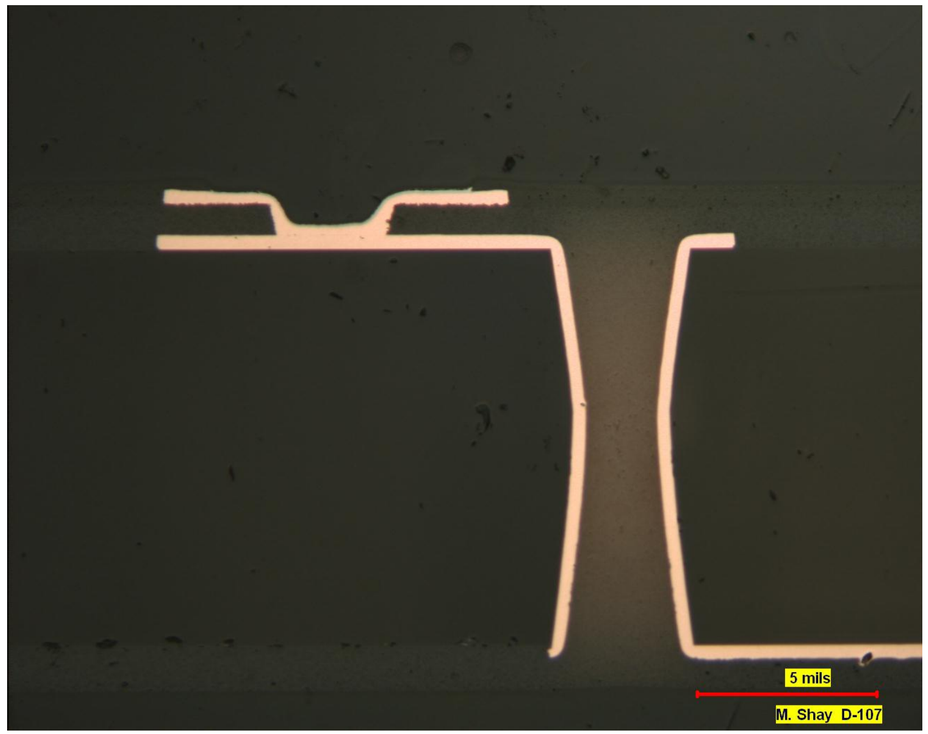


Aspect Ratio 3 Conformal Via

i3 Electronics

i3's Conformal Cu-Plated TGV





Aspect Ratio 3 Conformal Via

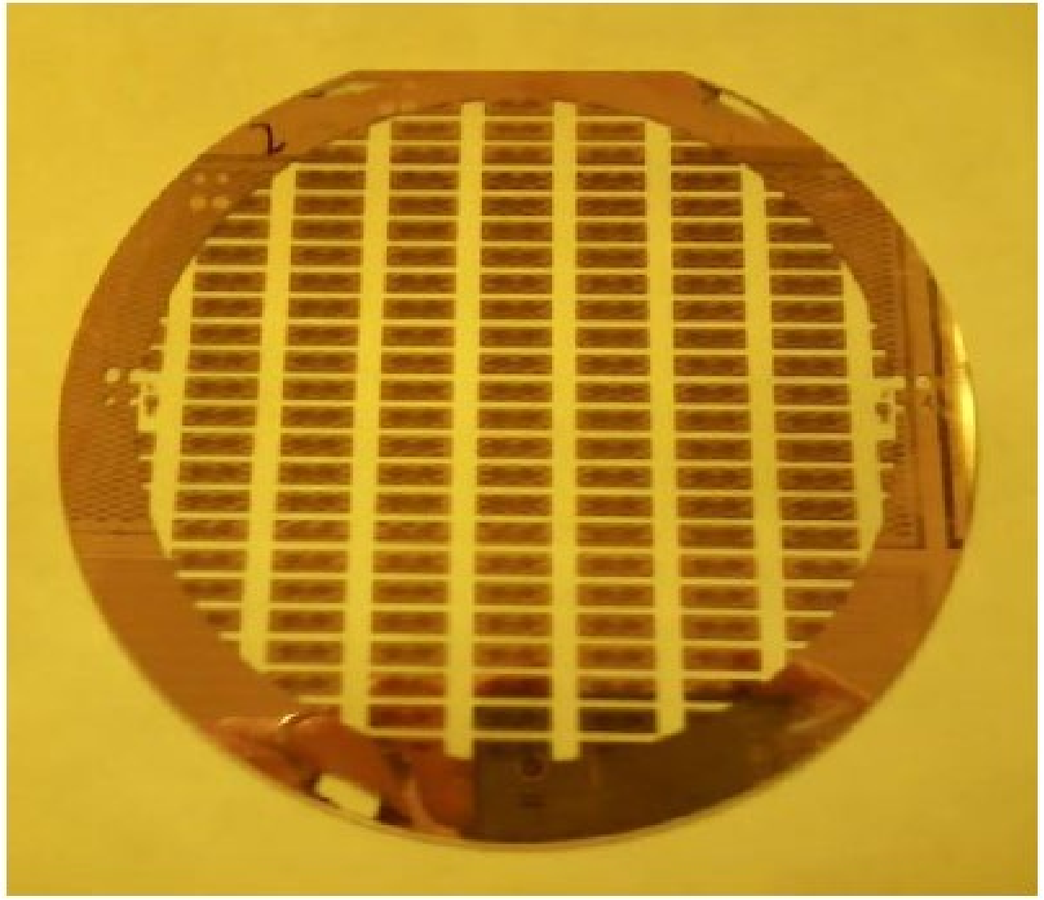
i3 Electronics

Outline

- Introduction
- Benefits of Glass for High Density Interconnects (HDI)
- Semi-Additive Plating (SAP)
- Through Glass Vias (TGVs)
- Glass Interposer
- Diplexer Module Build
- Electrical Characterization
- Thin Glass TGVs using a Cu bottom up fill process
- Summary

i3 Electronics

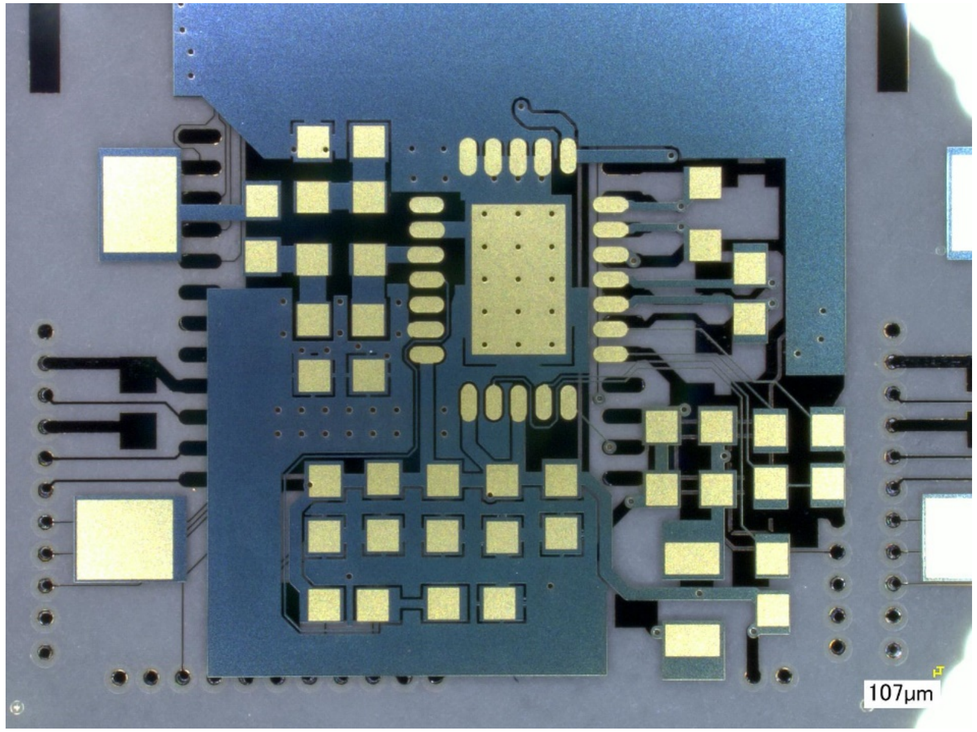
Metallized 6” Glass Wafer



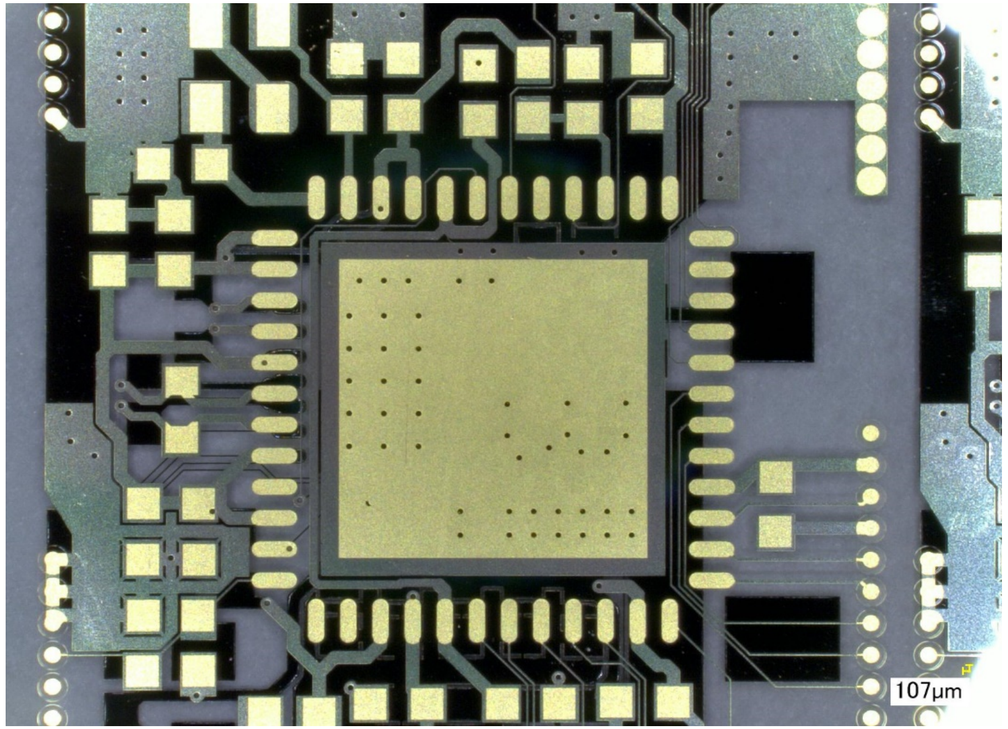
Double-sided Cu Pattern Plating

i3 Electronics

Glass Interposer



Front side of Glass Interposer



Back side of Glass Interposer

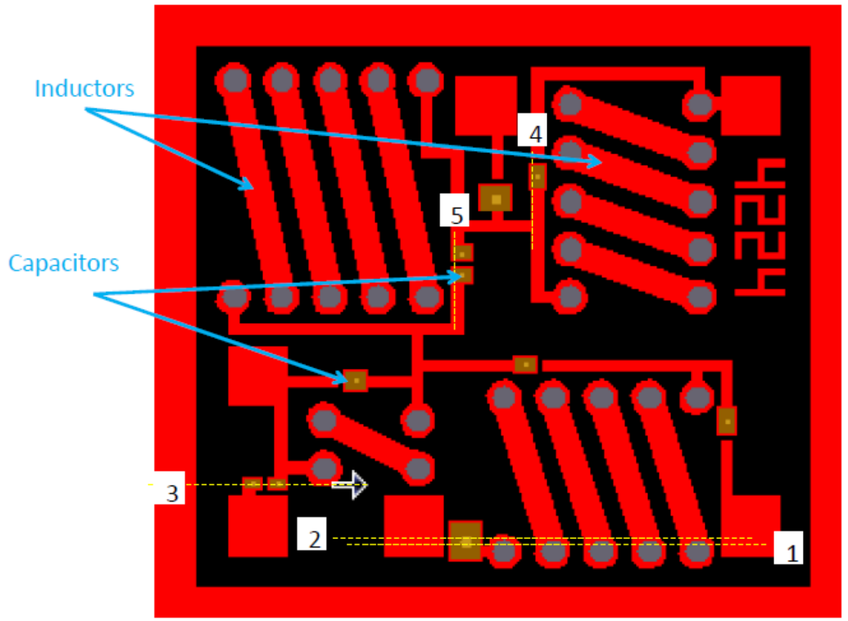
i3 Electronics

Outline

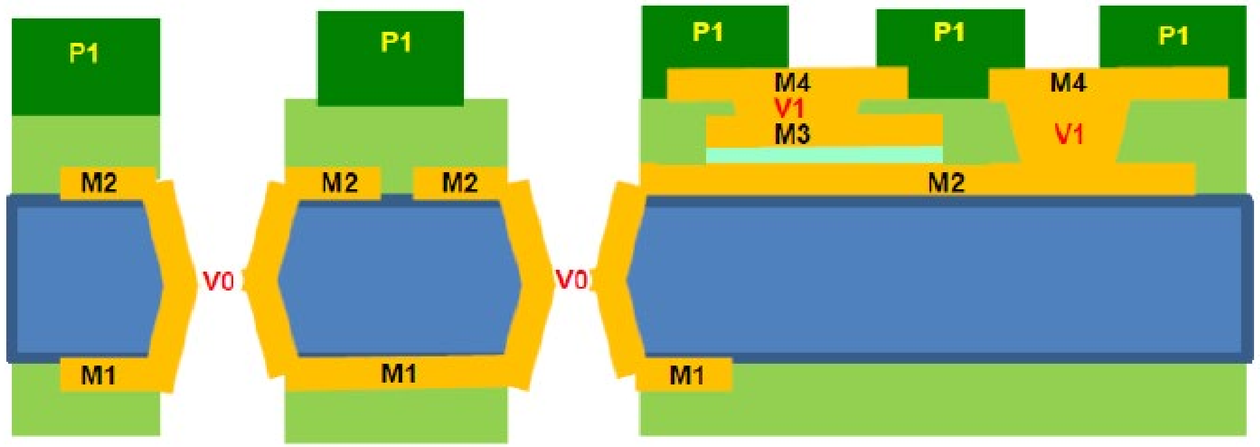
- Introduction
- Benefits of Glass for High Density Interconnects (HDI)
- Semi-Additive Plating (SAP)
- Through Glass Vias (TGVs)
- Glass Interposer
- Diplexer Module Build
- Electrical Characterization
- Thin Glass TGVs using a Cu bottom up fill process
- Summary

i3 Electronics

Diplexer Module



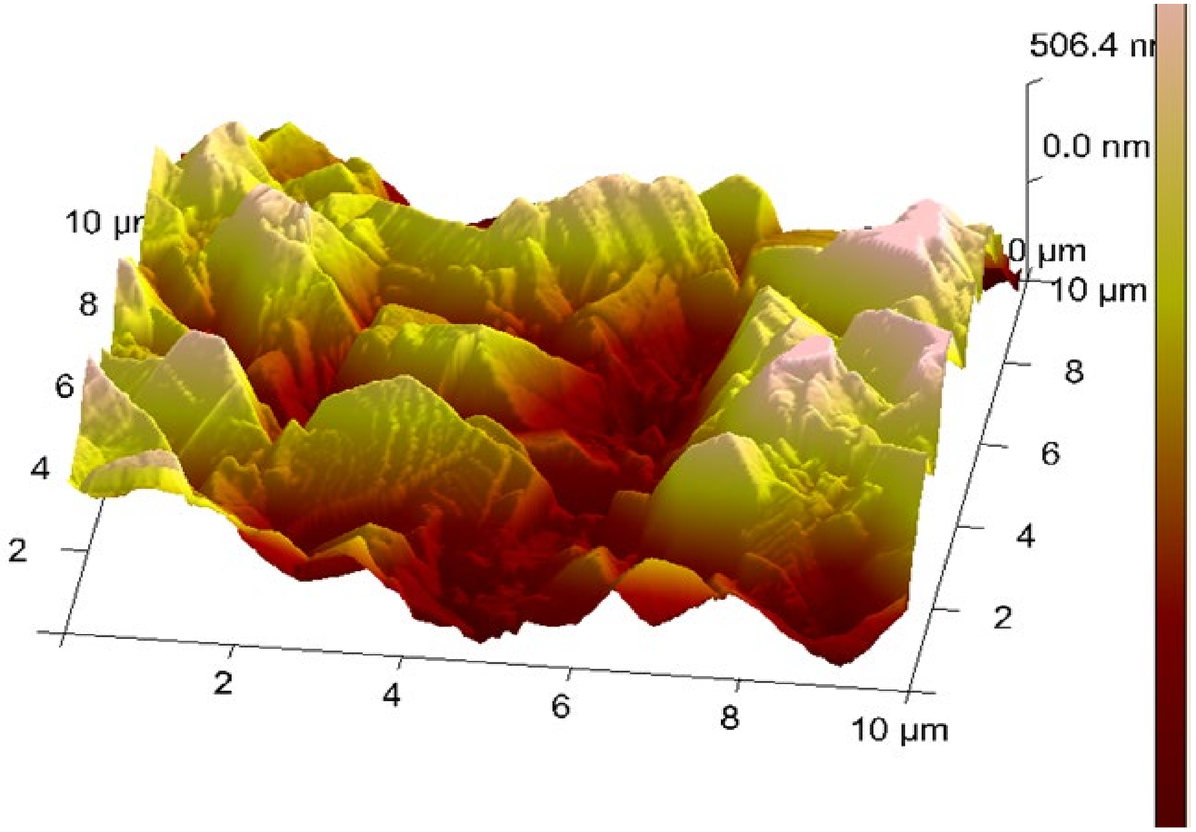
Top View of Diplexer Module



X-section of Diplexer Module

i3 Electronics

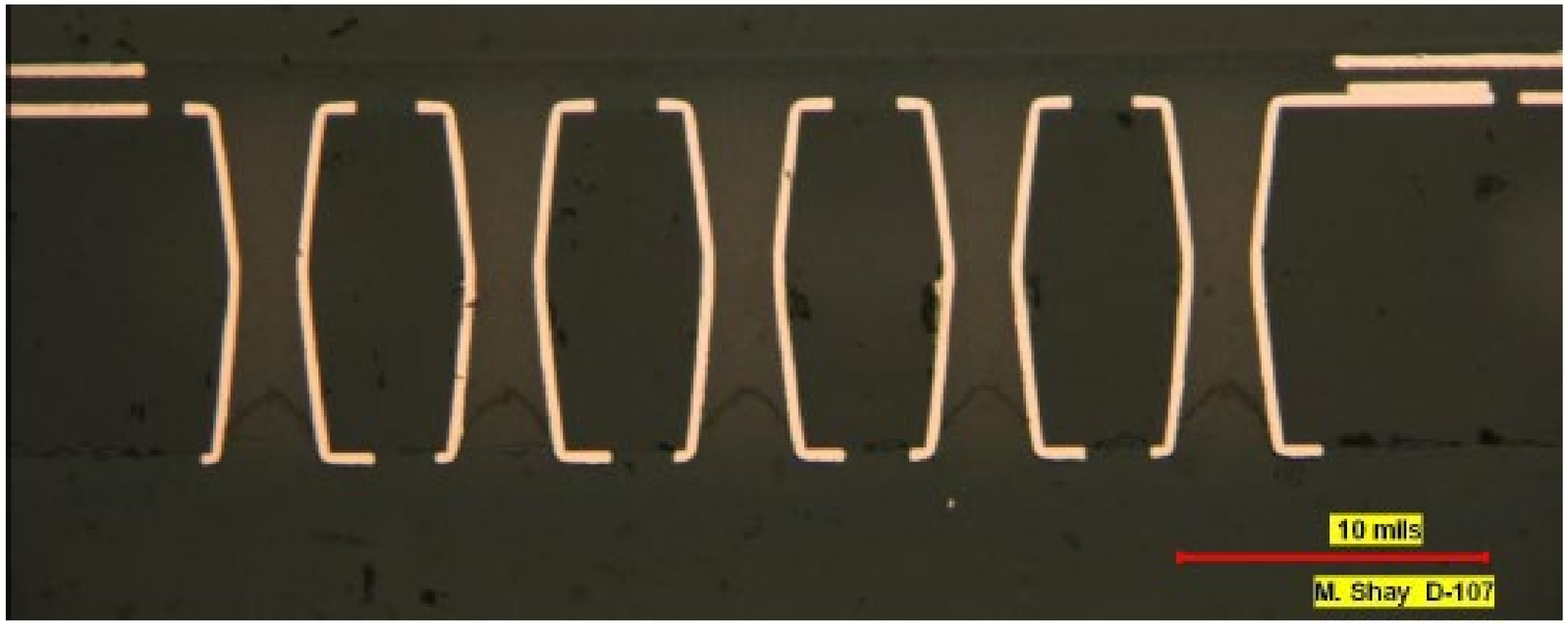
AFM Measurements of M2 Metal Layer



Nominal roughness of Cu on M2 Layer was 200nm

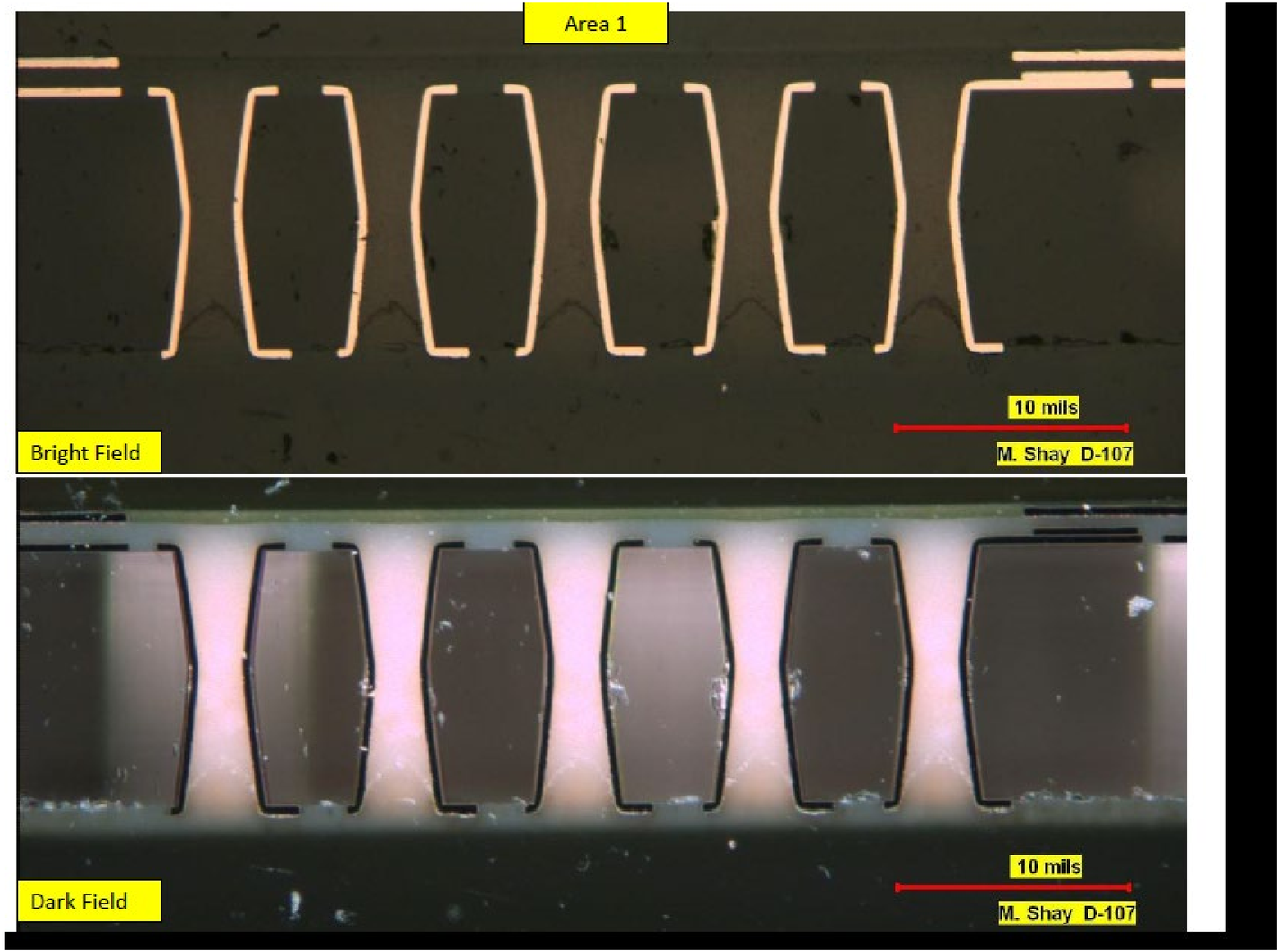
i3 Electronics

Cu-Plated Conformal Vias



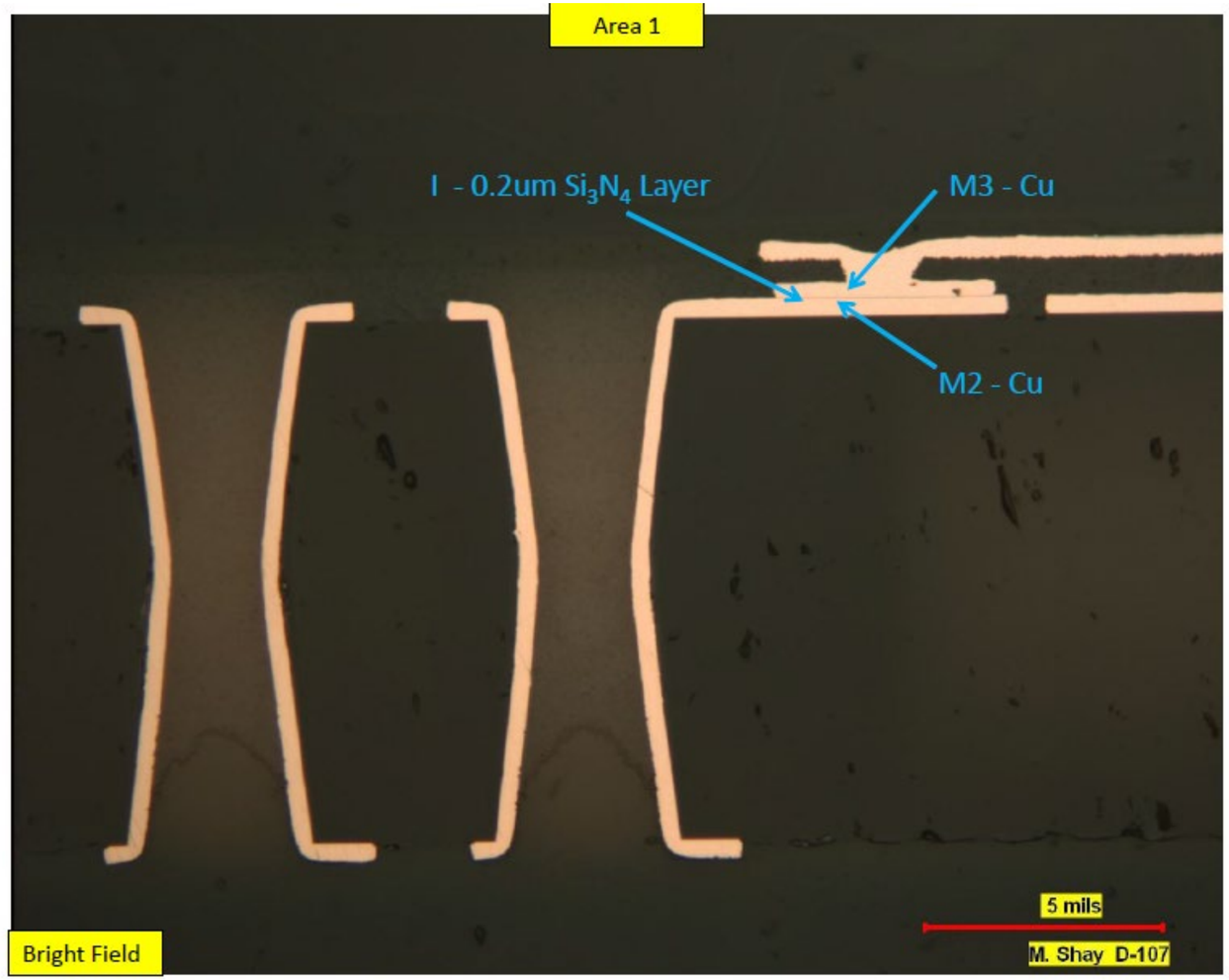
i3 Electronics

Diplexer Module



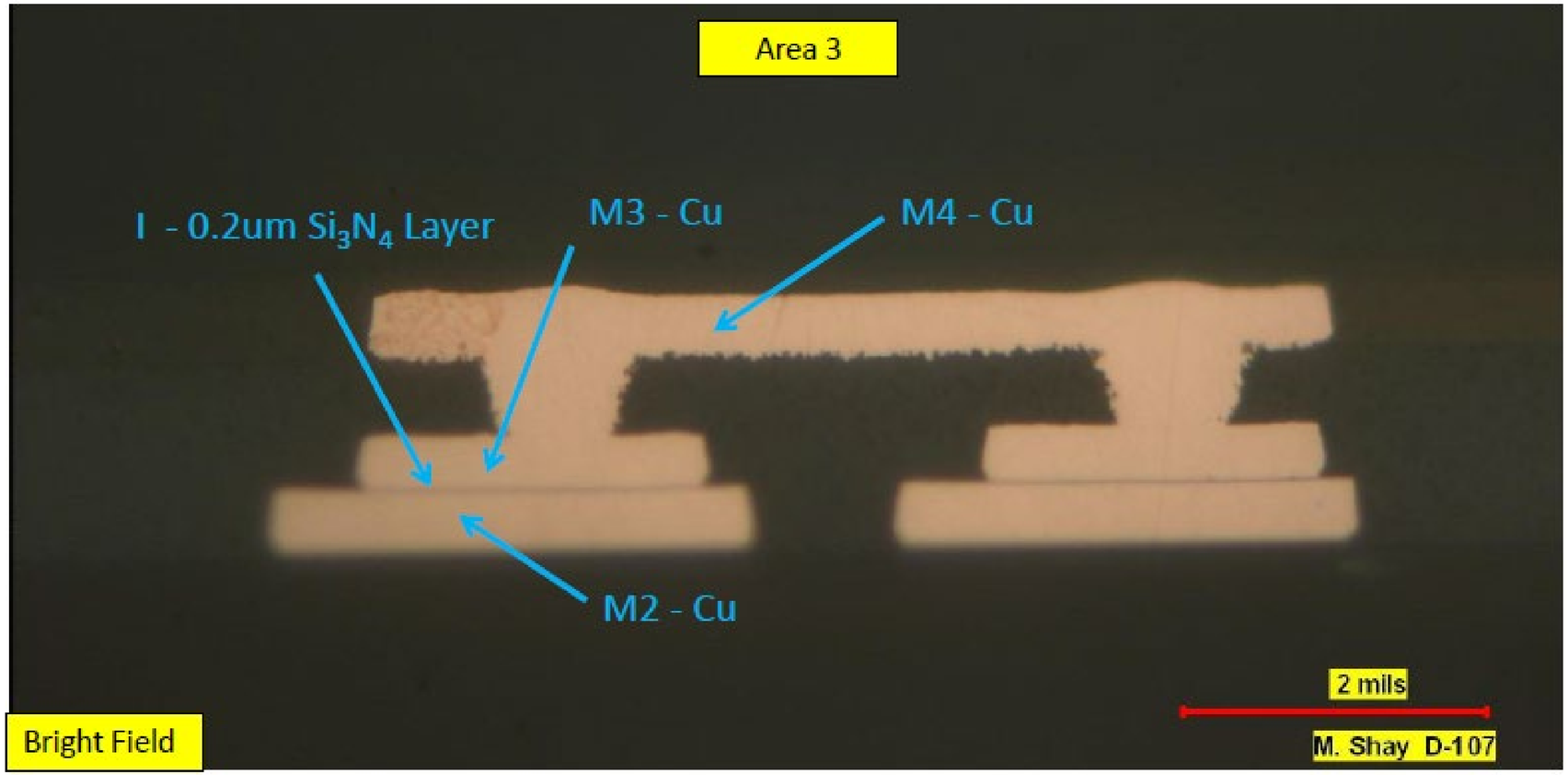
i3 Electronics

Diplexer Module



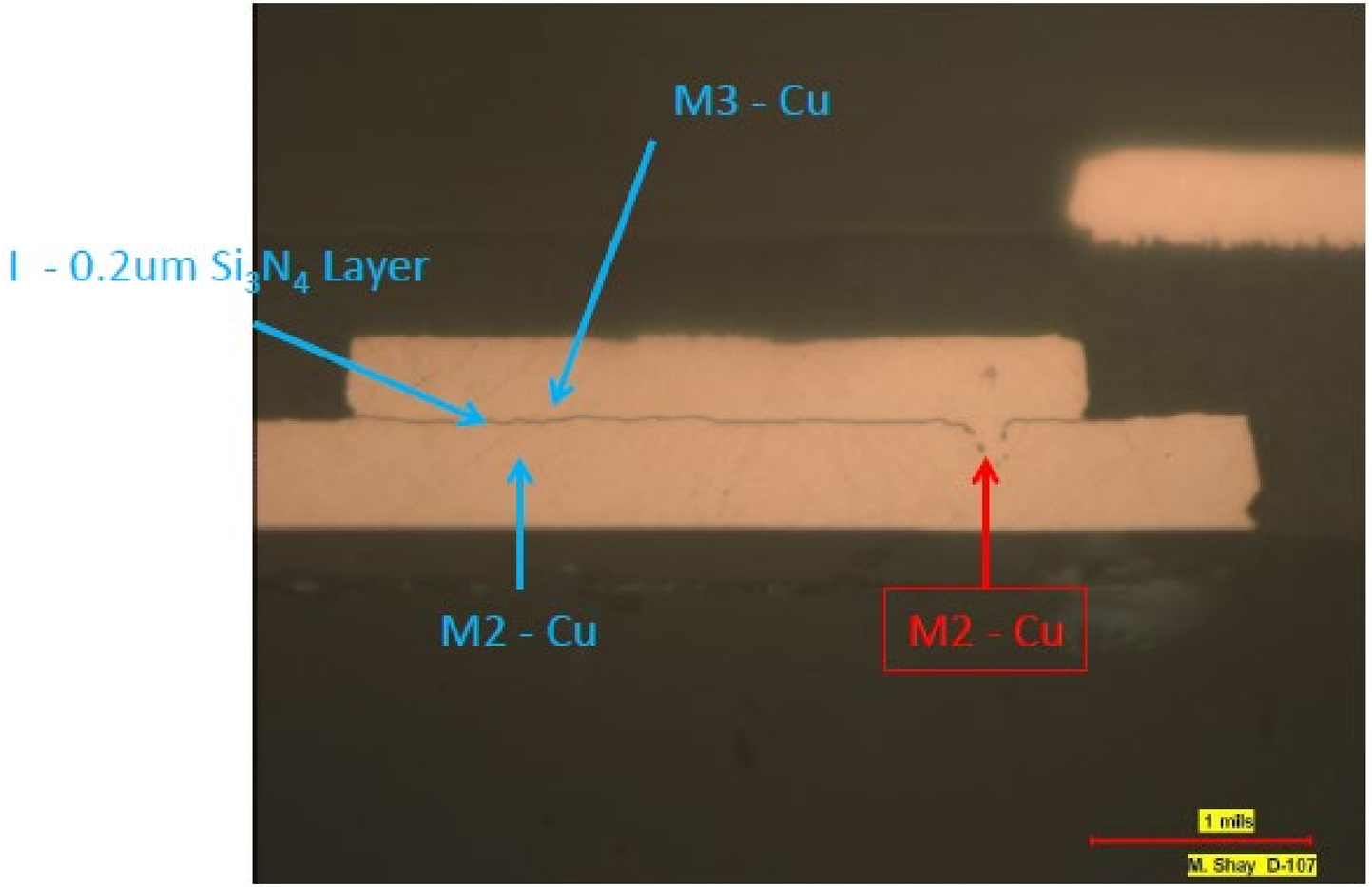
i3 Electronics

Diplexer Module



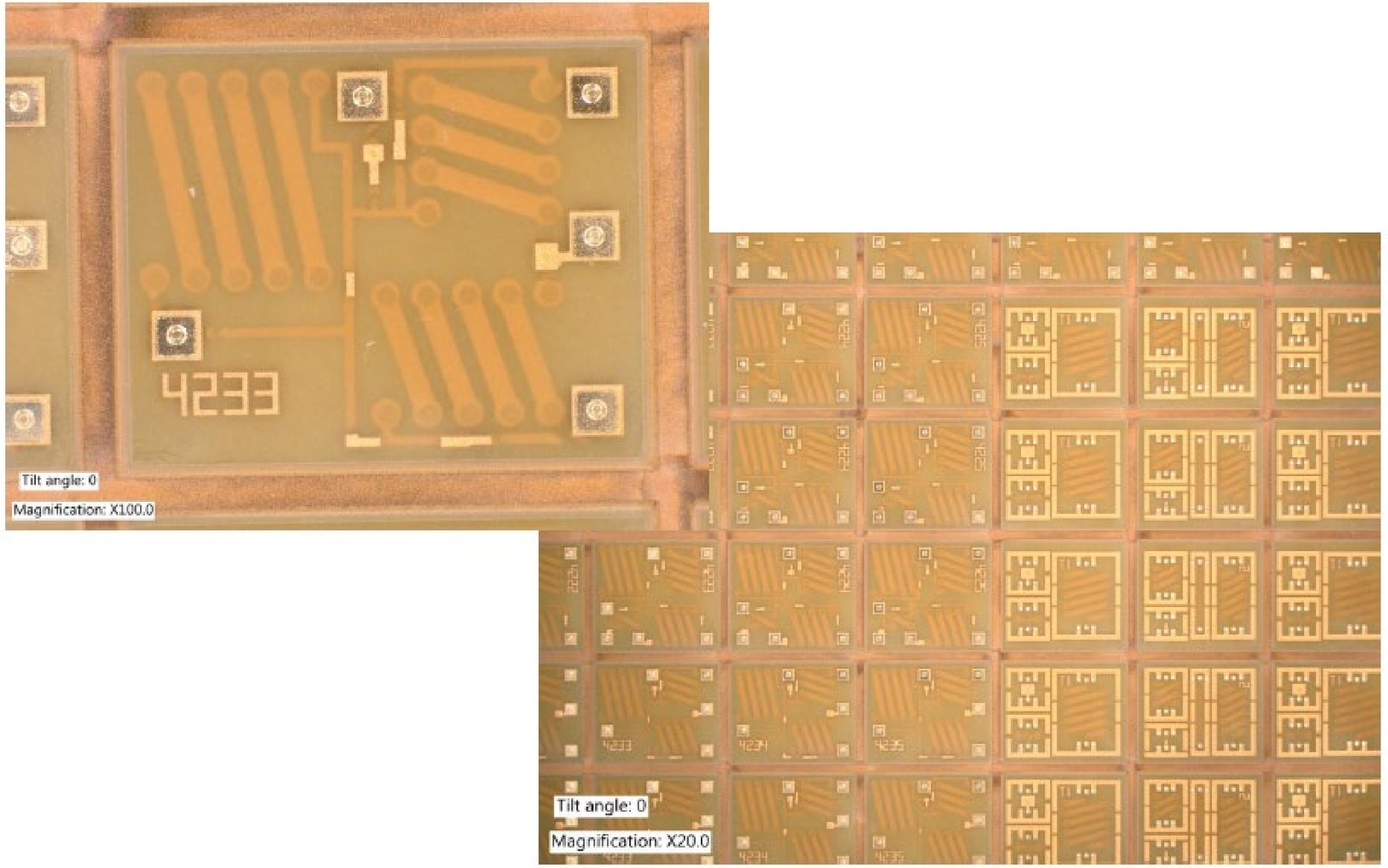
i3 Electronics

Cu-Plated Conformal Vias



i3 Electronics

Diplexer Panel Processing



i3 Electronics

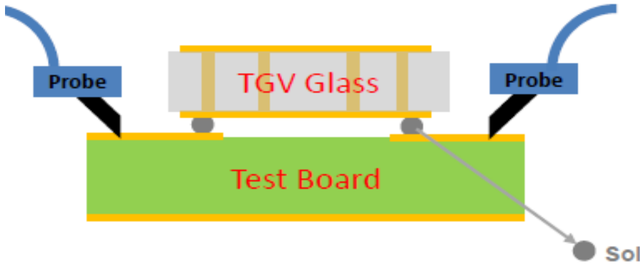
Outline

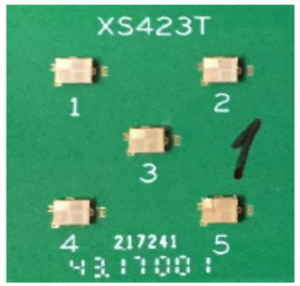
- Introduction
- Benefits of Glass for High Density Interconnects (HDI)
- Semi-Additive Plating (SAP)
- Through Glass Vias (TGVs)
- Glass Interposer
- Diplexer Module Build
- Electrical Characterization
- Thin Glass TGVs using a Cu bottom up fill process
- Summary

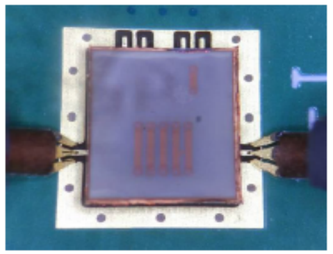
i3 Electronics

Measurement Method

- Solder balls are hand planted on device pads
- Bumped devices are mounted on test boards
- Device is probe tested on test board with VNA







i3 Electronics

#	Area /um^2	Capacitance（pF） design	Capacitance（pF） Measurement							
			1	2	3	4	5	6	7	8
Cap#1	230×280	20.8	19.1	19.6	19.9	19.9	19.7	20.2	20.3	20.2
Cap#2	50×50	0.81	0.75	0.76	0.76	0.77	0.78	0.79	0.80	0.79

Comparison of measured capacitance with designed value, only ~5% difference.

i3 Electronics

#	Inductance@100MHz（nH）	Q^{PEAK} @F /GHz	SRF (GHz)	method
Ind#1	7.1	71 @2.0	5.6	simulation
	7.2	70 @1.96	5.6	measurement
Ind#2	4.0	76 @2.6	8.3	simulation
	4.1	78@2.7	8.1	measurement

Comparison of measured and simulated inductance. Data shows very good correlation.

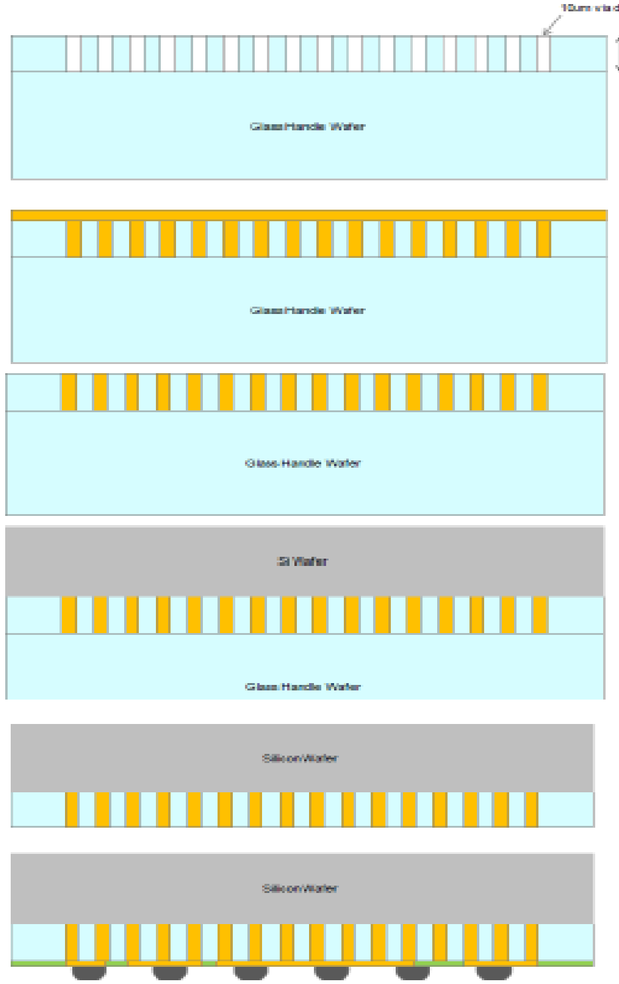
i3 Electronics

Outline

- Introduction
- Benefits of Glass for High Density Interconnects (HDI)
- Semi-Additive Plating (SAP)
- Through Glass Vias (TGVs)
- Glass Interposer
- Diplexer Module Build
- Electrical Characterization
- Thin Glass TGVs using a Cu bottom up fill process
- Summary

i3 Electronics

Method to create TGVs using a TSV fill process



a) Thin glass interposer with vias attached to a thick glass handle wafer.

b) Vias are filled using a conventional bottom up fill Cu TSV process.

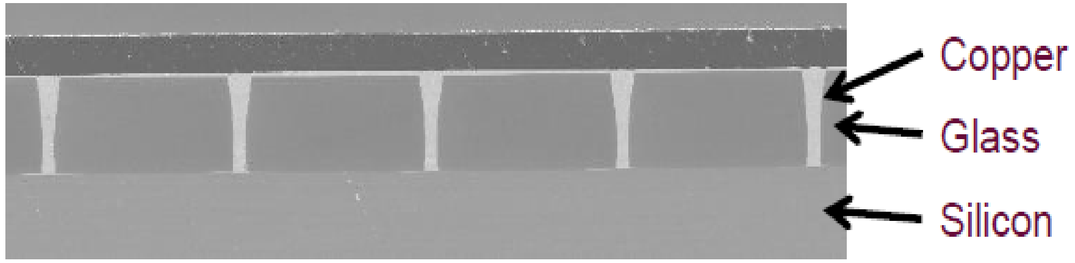
c) Topside of plated TGVs are thermally annealed and CMP.

d) Glass wafer with Cu plated TGVs are then attached to wafer.

e) Remove handle wafer

f) Backside metallization, passivation and solder bumping.

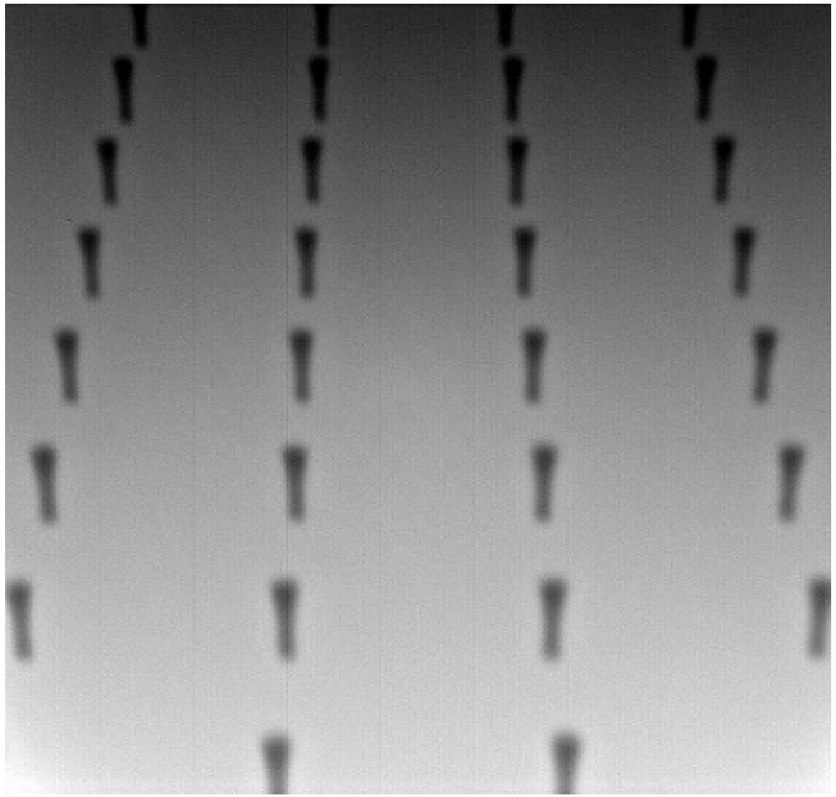
i3 Electronics



- Achieved void free via fill – important for reliability

i3 Electronics

X-ray Image of a TGVs in a 100um Thick Glass Wafer



Outline

- Introduction
- Benefits of Glass for High Density Interconnects (HDI)
- Semi-Additive Plating (SAP)
- Through Glass Vias (TGVs)
- Glass Interposer
- Diplexer Module Build
- Electrical Characterization
- Thin Glass TGVs using a Cu bottom up fill process
- Summary

Summary

- Glass manufacturers have manufacturing capability to produce holes in glass.
- Semi-Additive Plating (SAP) or pattern plating, can produce fine lines and spaces and TGVs on a glass substrate.
- Recent work has shown success in deposition a Si_3N_4 layer for an insulator used in a capacitor and as a passivation layer on a glass interposer.
- An ABF film has been successfully laminated to glass and can maintain adhesion and be effectively laser drilled. Also, the ABF material is capable of filling an AR 3 TGV.
- Processes have been developed to manufacture both glass wafers and panels using modified circuit board processes that have been adapted to handle fragile glass substrates.
- This work has shown how the use of a glass interposer can produce RF filters that have superior performance over those made using a silicon interposer.
- Cu-plating process for TSVs are compatible with similar vias dimensions in glass to produce robust and reliable TGVs.

Thank you

i3 Microsystems, Inc.
9900 16th Street North
St. Petersburg, FL 33716
Email: Charles.Woychik@i3microsystems.com