Advanced Double Side SiP with Thermal Enhance Solutions for 5G Mobile Application

Company Contact Name: Wen-Jung (Mike) Tsai
Contact Email: miketsai@SPIL.com.tw
Phone number: +886-978-890686
Siliconware Precision Industries Co., Ltd (SPIL)

Outline

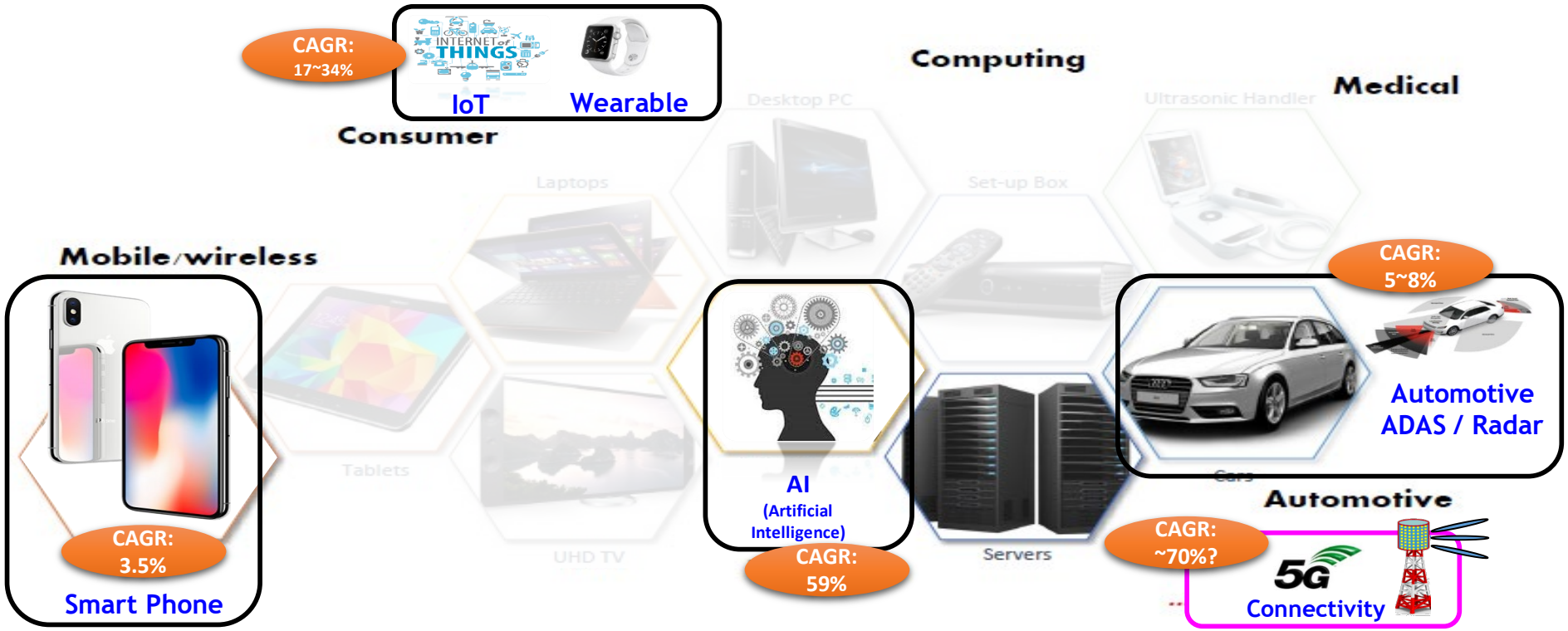
- **Introduction**
  - ✓ **Electronic Devices Trend from Market**
  - ✓ **Application Sweet Spot & Package Types**
- **Advanced Package Technology for 3D SiP**
  - ✓ **Test Vehicle: Advanced SiP Design Integration**
  - ✓ **Assembly Challenge & Solution**
  - ✓ **Reliability Result**
- **Summary**

Outline

- **Introduction**
  - ✓ **Electronic Devices Trend from Market**
  - ✓ **Application Sweet Spot & Package Types**
- **Advanced Package Technology for 3D SiP**
  - ✓ **Test Vehicle: Advanced SiP Design Integration**
  - ✓ **Assembly Challenge & Solution**
  - ✓ **Reliability Result**
- **Summary**

Semiconductor Markets Trend

Reference: Yole

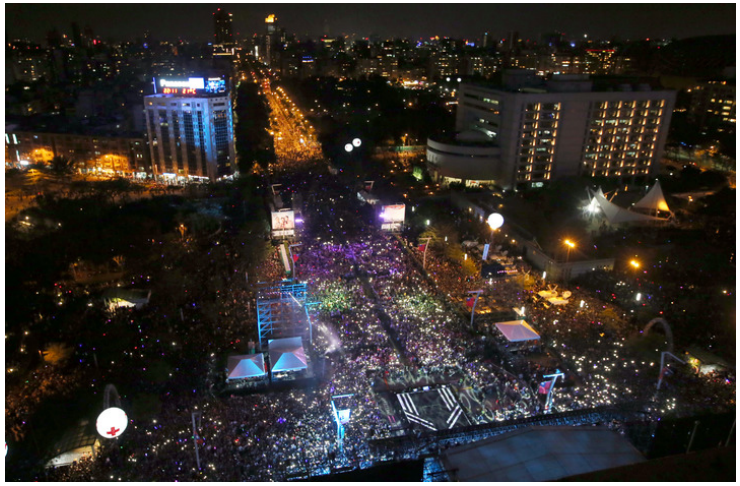


✓ Those applications are required for packaging technology with…
1. High Speed Transmission
2. Multi-Function Integration

Why Need 5G Connectivity Technology??

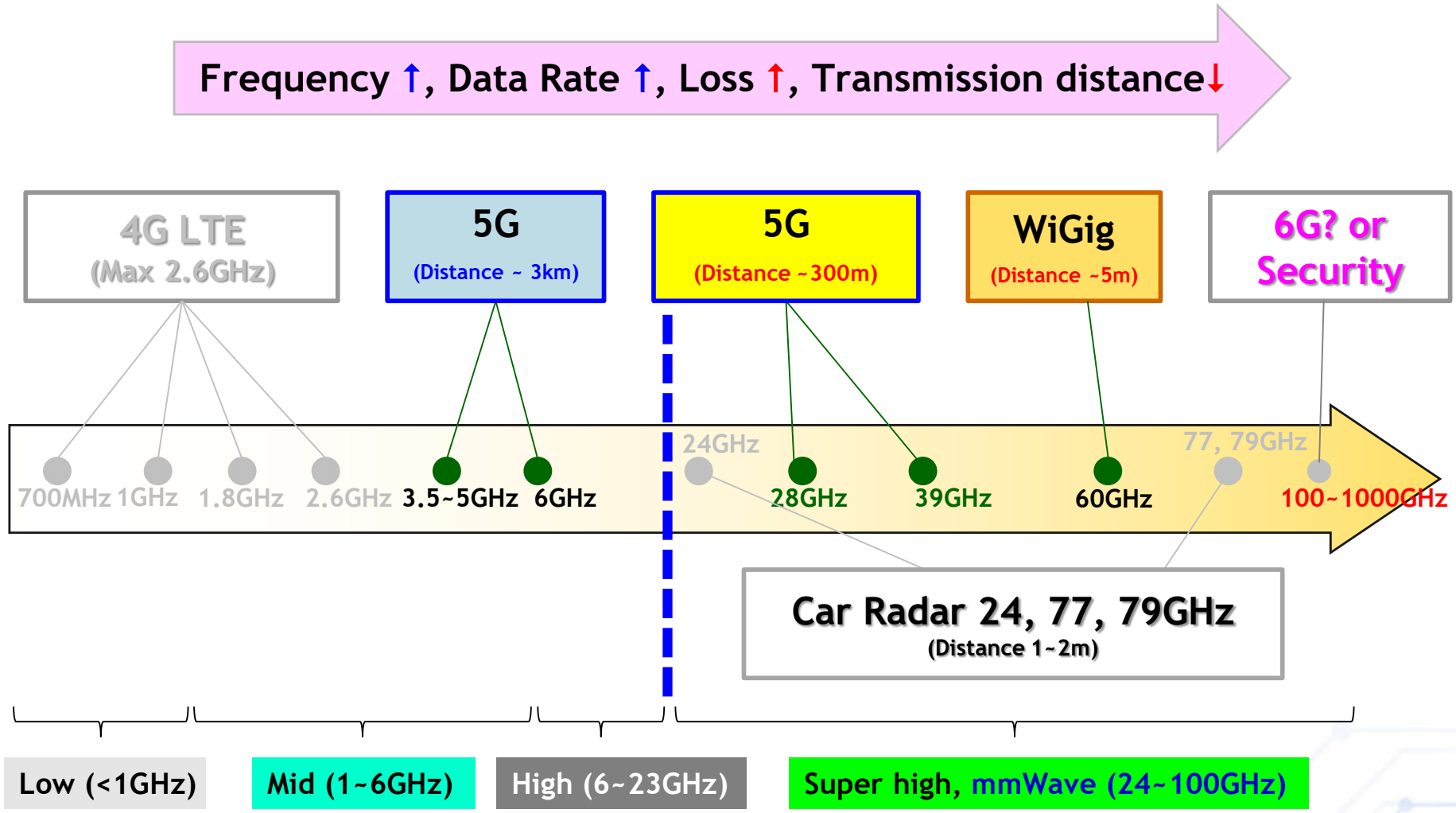
Reference: google Taiwan news

When New Year (at Taipei 101)



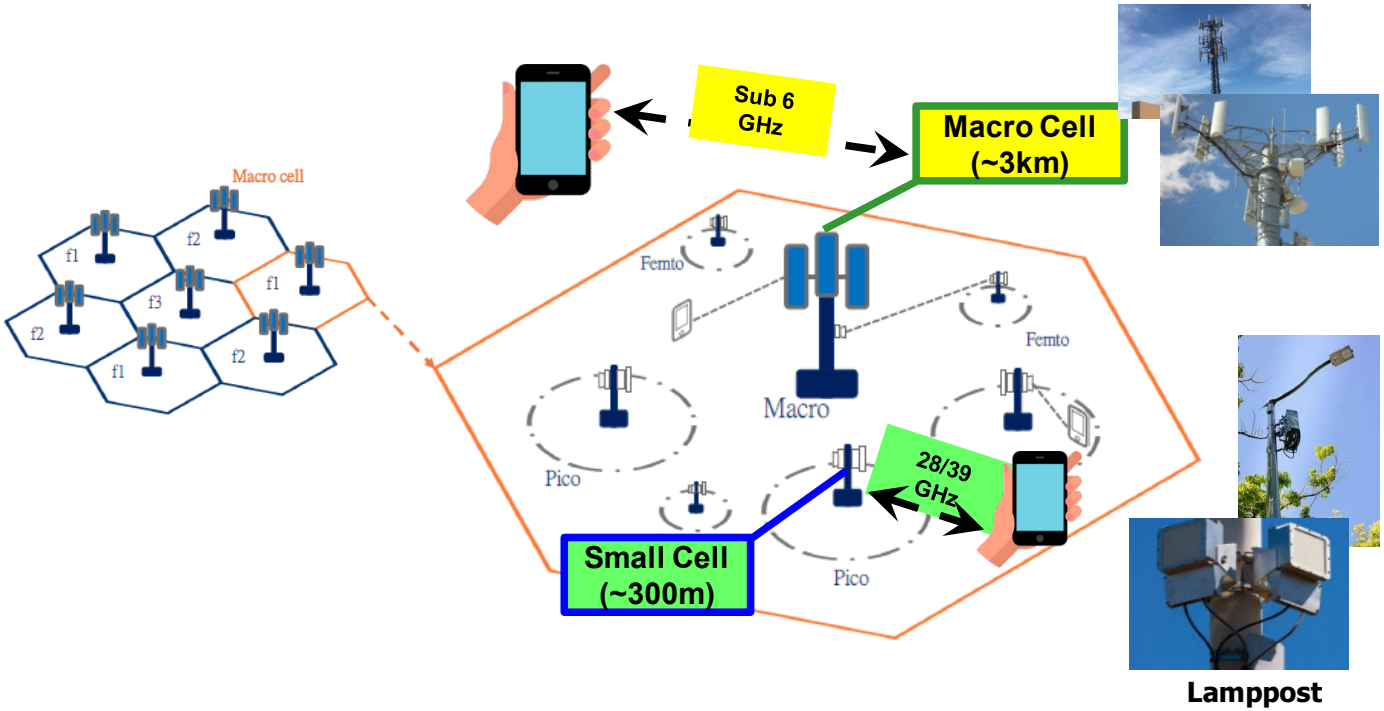
More People+ = Share Same Bandwidth = More Lag+

RF Connectivity Frequency Band



5G's Ecosystem Overview

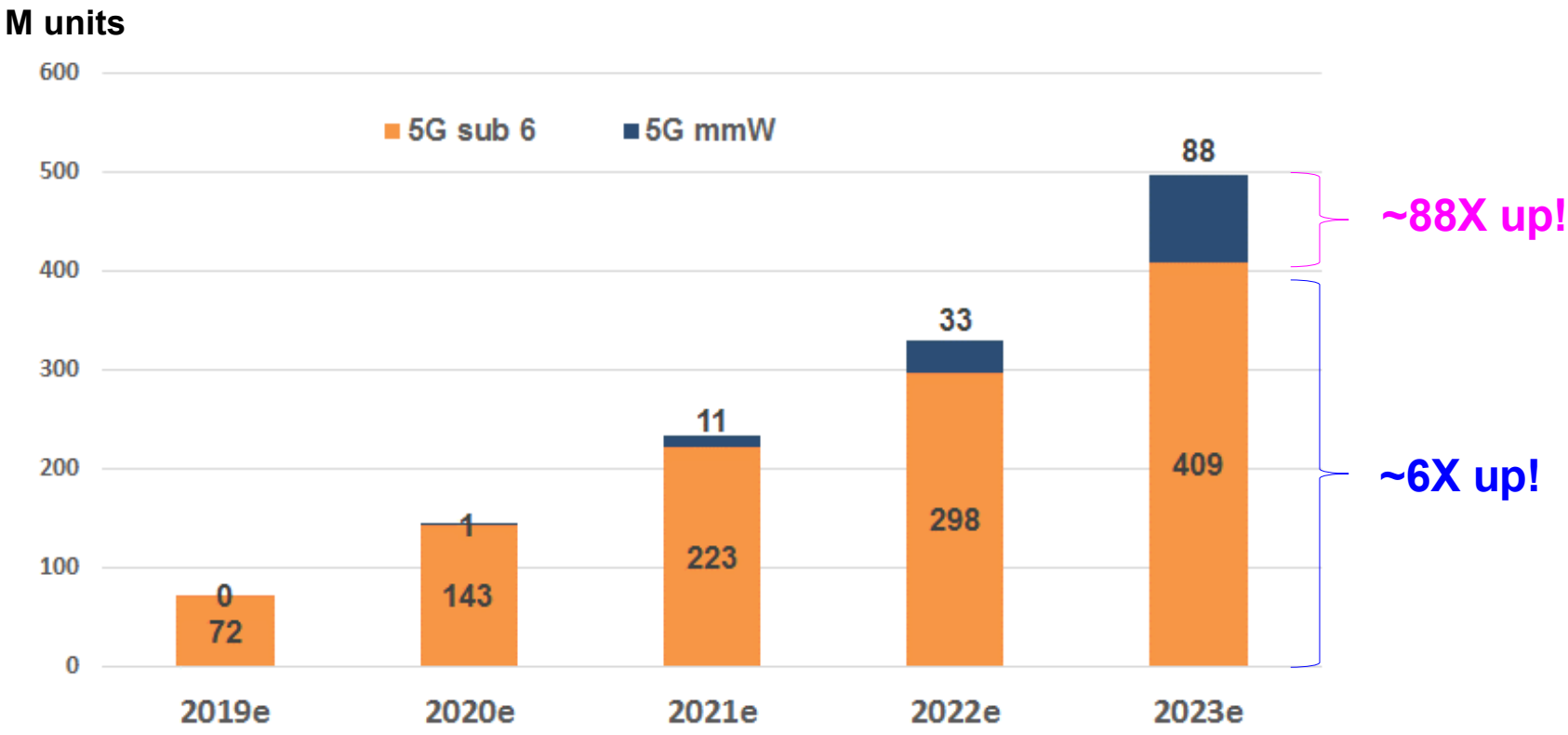
Reference source: Yole



✓5G-Sub 6 GHz will work in parallel with 5G mmWave (28 & 39GHz) developments.

5G Phone Shipment FCST

Source: Yole 2019



✓Before year 2020, major focus on Pre-5G (sub-6GHz)!!

✓After year 2020, will start commercial for 5G mmWave!!

What's Package Solution??

(Internet of Things)
IoT / Wearable / 5G Application

I. Market

1. Smart City
2. Smart Car
3. Smart Home
4. Smart Health
5. Smart Factory

II. Product

1. MCU; Micro Controller
2. Memory
3. Wireless, Connectivity
4. Power Management
5. Sensors

III. Tech

1. Small Form Factor
2. System Design Integration
3. Low-profile Technology
4. Ultra Low Power
5. High-speed Technology

What's Package solution?

5G Package Solutions


FCBGA (Modem)

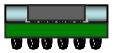

SiP (FEM module)

- ✓ **Advance Silicon Node (<16nm)**
- ✓ **High Integration Solution**

Small Cell

Macro Cell


Large Lid FCBGA
(Switch/Router)


ED-FCCSP
(GaN)

- ✓ *Large PKG Size/ Die Size*
- ✓ *High Thermal TIM (>15W/mK)*
- ✓ *High power → GaN*

FWA/CPE

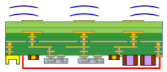

Antenna in PKG
(mmWave)

- ✓ **High Antenna Array (>4x4)**
- ✓ **High Thermal Material (>5W/mK)**

Client Devices


FC-Hybrid (Modem)

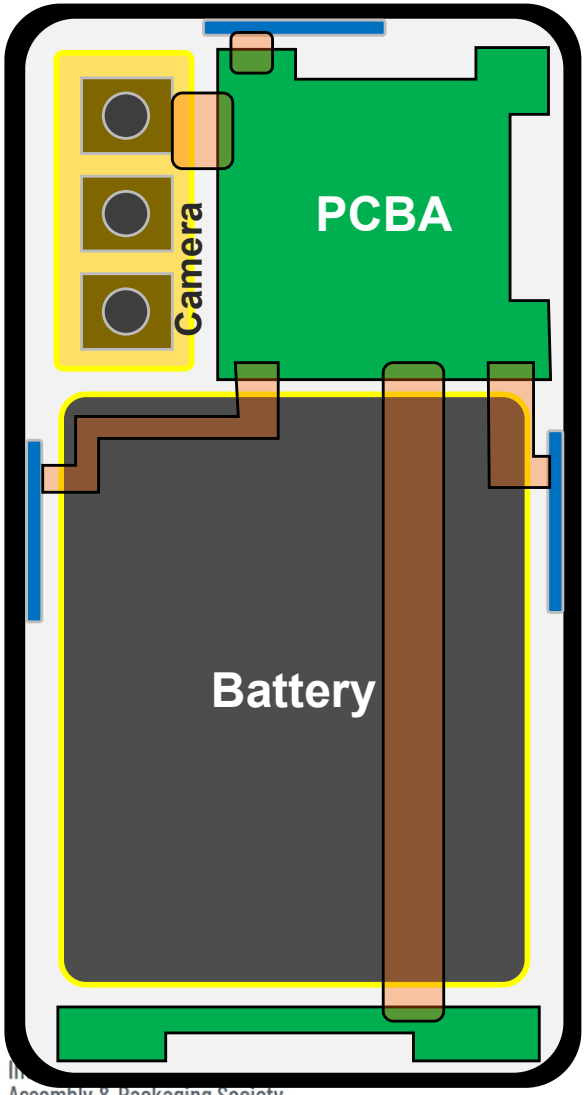

SiP (FEM module)


Antenna in PKG
(mmWave)

- ✓ **Low Loss Material/High thermal**
- ✓ **Small Form factor (→ Double Side SiP)**

000505

5G Phone KEY Requirement

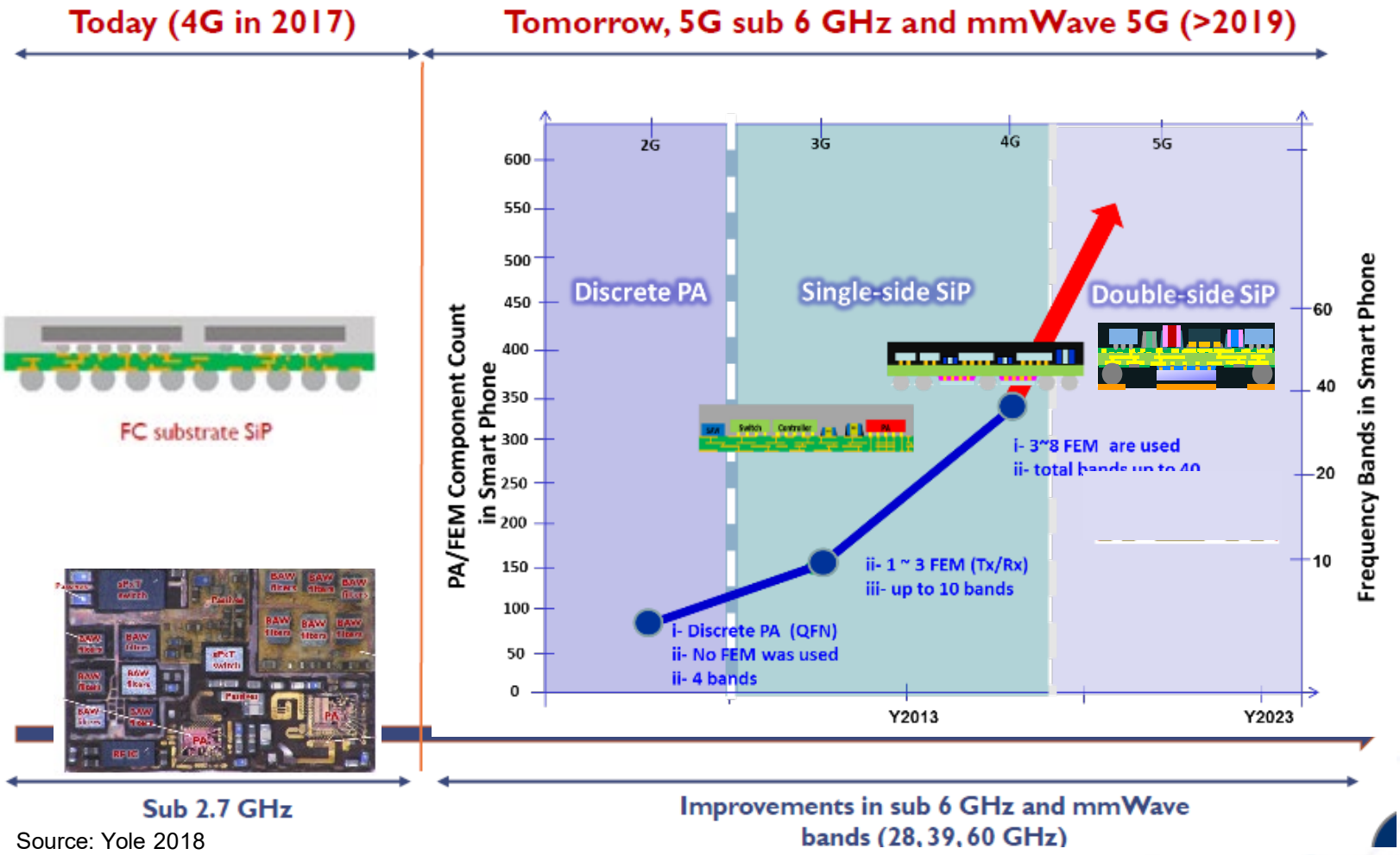


Phone	#	Major Item	Trend
Inside	1	Camera qt'y 	(3 → 4 → 5?)
	2	Battery size 	(Bigger, 1pcs → 2pcs)
	3	RF FEM Band (~36 band) 	(>40 for Sub-6GHz)
	4	-	Quick Charger Wireless Charger
	5	-	mmWave AiP (2~3pcs)
	6	2D PCBA (Larger) 	3D PCBA (Smaller) 
Outside	7	Thickness	7 ~ 8mm

Source: Teardown report (Prismark, iFixit…)

➔ More challenge on PCBA area (Limit space)
➔ Need high density & high integration SiP solution….

RF-FEM Package Evaluation Trend

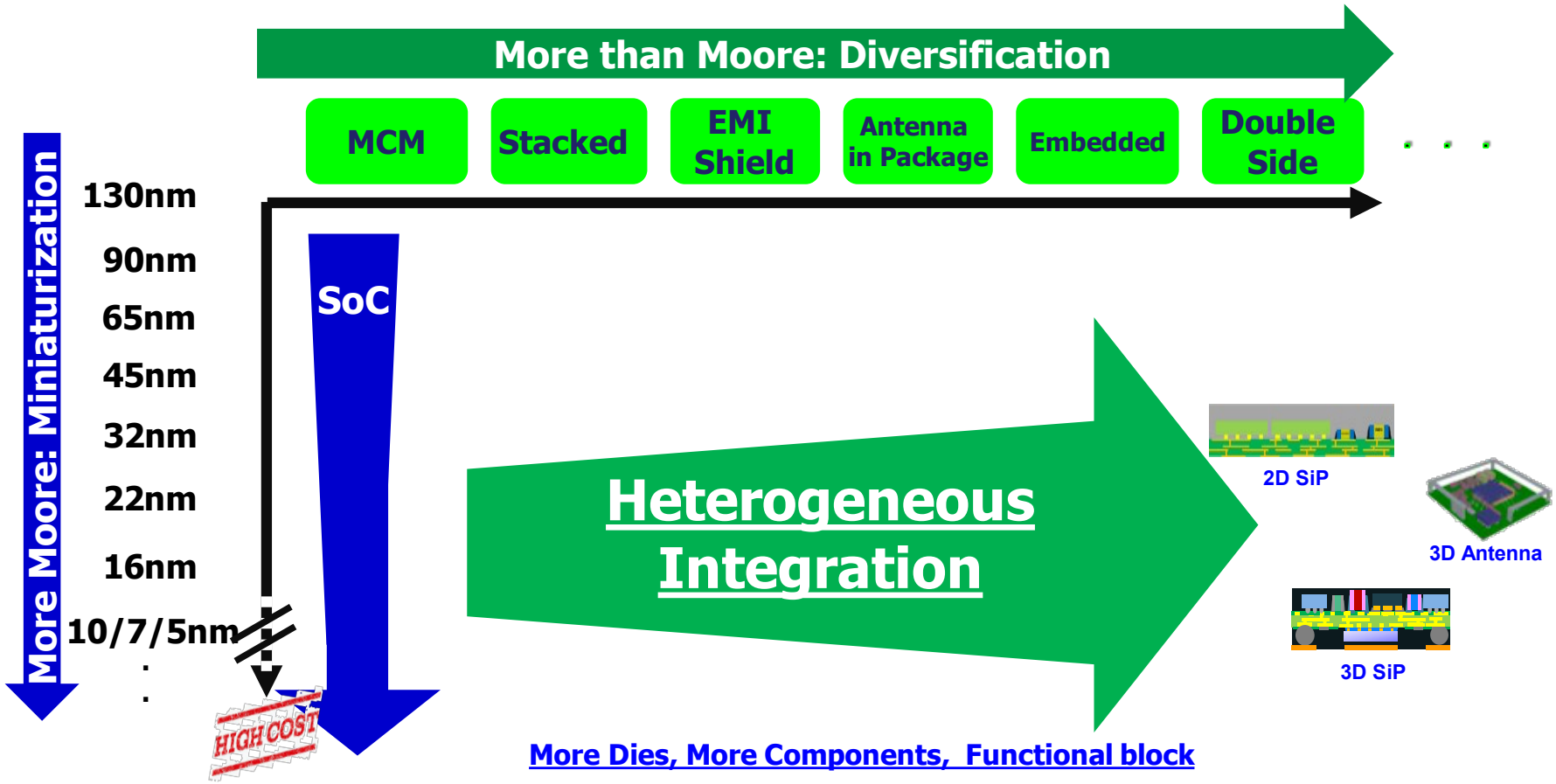


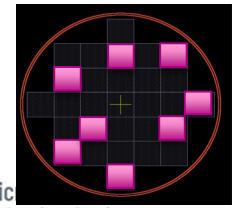
Source: Yole 2018

- ✓ More and more FEM component to support difference 3G ~ 5G frequency band!
- ✓ Key challenge is how to design a high integration solution for SiP module!

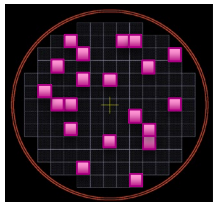
So, Why Need 3D SiP?

The Major Sweet Spot for Integration

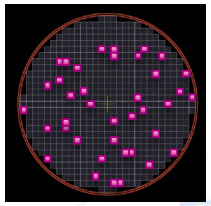




40*40mm die size
13 pcs defect
➔ Low Yield

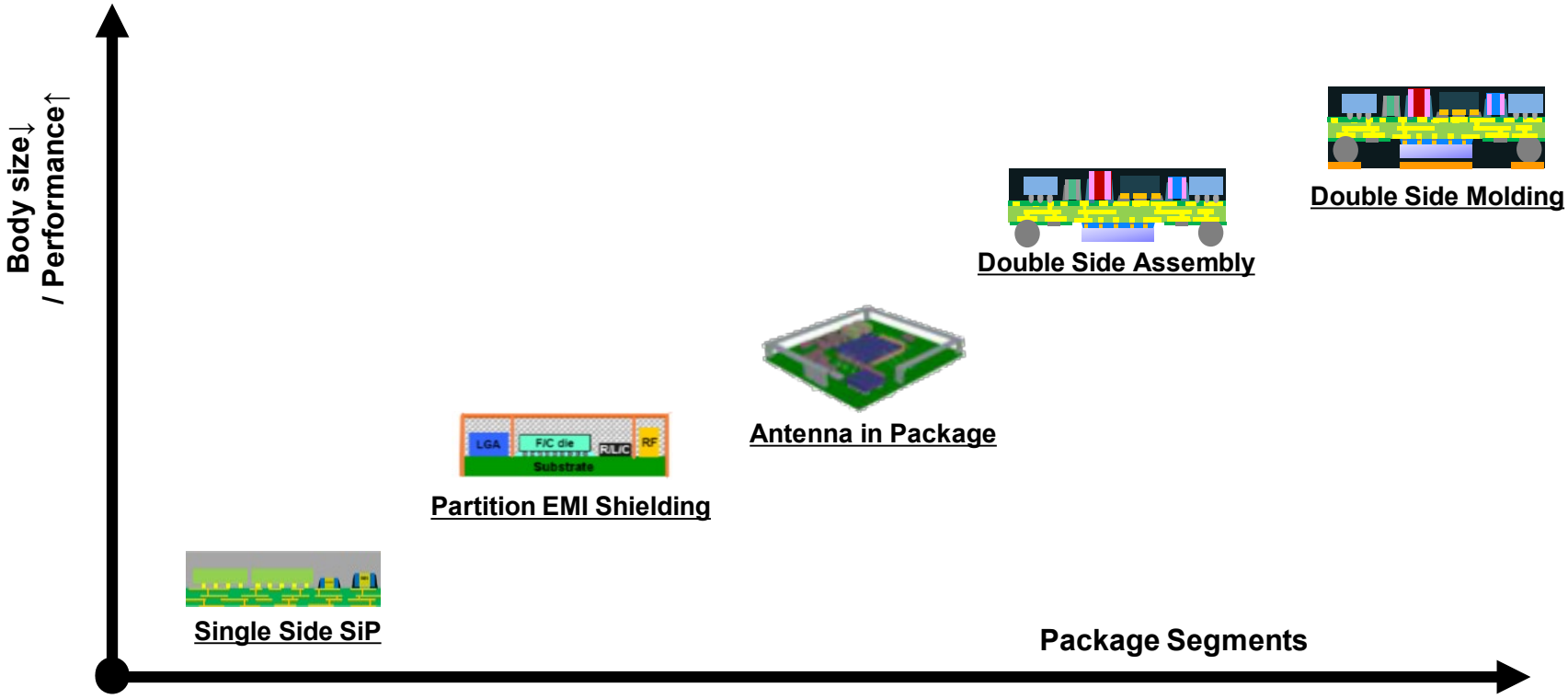


20*20mm die size
40 pcs defect
➔ Mid Yield



10*10mm die size
65 pcs defect
➔ High Yield

Advanced SiP Evolution Trend



➔More and more system integration requirements to drive packaging trend from

Horizontal → Vertical Integration Styles…

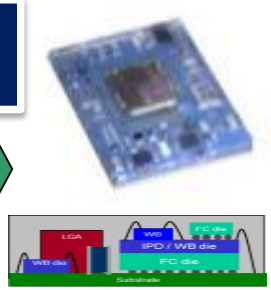
3D SiP Technology Anywhere for IoT

IoT Application Case I :

MCU + WiFi COB Solution

Size : 22 x 19mm

75% size reduction



3D SiP Integration
MCU + WiFi SiP

Size : 10 x 10mm

WiFi Plug

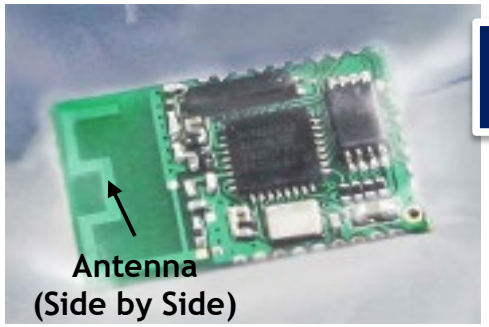
WiFi Air Conditioner

WiFi Lamp

WiFi Speaker

WiFi Sensor Hub

IoT Application Case II :

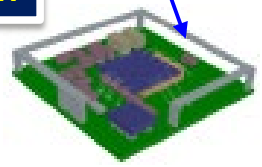


MCU + BLE COB Solution

Size : 18 x 12mm

80% size reduction

Antenna (3D Structure)



3D SiP Integration
MCU + BLE SiP

Size : 6 x 6mm

BLE Locker

BLE Toy

Care system

Hearing Aid

Swimming Band

Hand Band

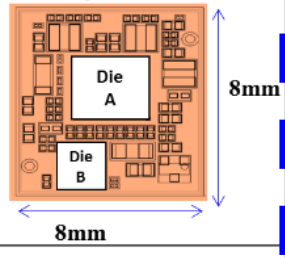
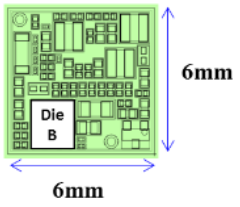
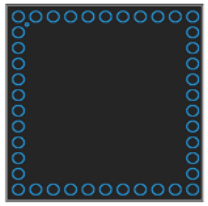
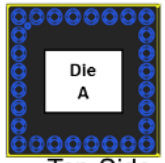
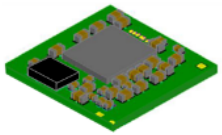
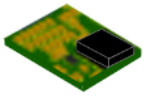
Outline

- Introduction
  - ✓ Electronic Devices Trend from Market
  - ✓ Application Sweet Spot & Package Types
- **Advanced Package Technology for 3D SiP**
  - ✓ **Test Vehicle: Advanced SiP Design Integration**
  - ✓ Assembly Challenge & Solution
  - ✓ Reliability Result
- Summary

Test Vehicle Design Information

➢ Test Vehicle Comparison Table:

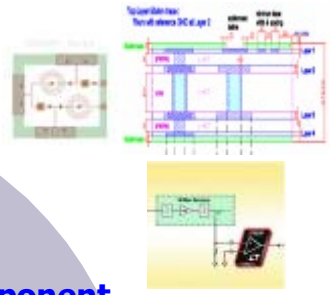
Item	Structure 1	Structure 2	Structure 3
Purpose	Single Side	Double Side	Double Side + Thermal Enhance
Package Structure			
PKG Size	100%	40~60% Smaller	40~60% Smaller
Thermal Solution	NA	Thermal Pad	Add Thermal Interface Material

Item	Single Side SiP	Double Side SiP
Dimension (mm)	8 x 8	6 x 6
Layout Simulation (Top/Back side)	Top side 	Top side 
Bottom Side	 Back side	 Top Side Back side
3D Structure Photo		
Size Ratio	100%	~50%

✓ 3D SiP by using Double Side Molding Integration technology.
✓ This structure provided ~50% size reduction benefits to save the assembly and substrate cost!!

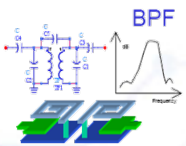
3D SiP Module Development Flow

1. Feasibility Study



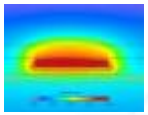
2. Component Selection

3. Schematic / Layout Design

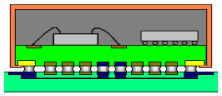


RF, Thermal… Simulation

4. Performance Simulations



5. Package / Process Development

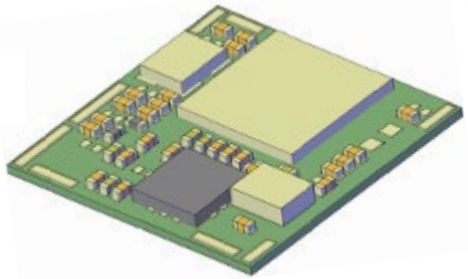


6. Test System Setup

7. Qualification

MSL

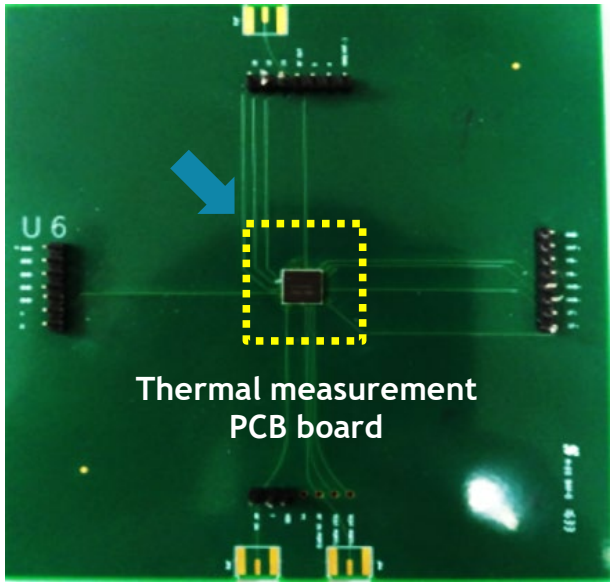
TCT
HAST

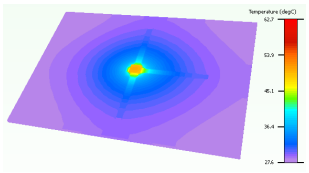


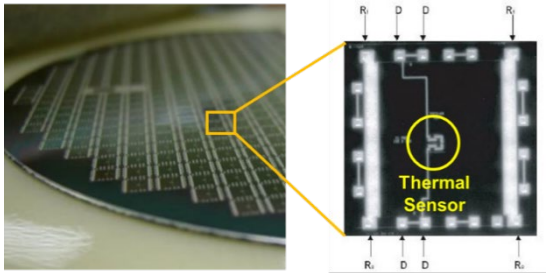
3D SiP

Thermal Performance Verification Result

➢ Thermal simulation & Measurement:







(b)

Thermal die structure

➢ Thermal dissipation comparison result:

Package Type	Single Side SIP	Double Side SIP		
M/C type	Normal EMC (K=1.0w/mk)	Normal EMC (K=1.0w/mk)	High thermal EMC (K=2.5w/mk)	Normal EMC (K=1.0w/mk)
Ag epoxy	--	--	--	k = 25w/mk
θ JA (˚C/W)	33.8	45.2	37.7	33.5
θ JB (˚C/W)	24.8	30.0	21.9	18.7

-17% ~ -26% | -10% ~ +13% | +1% ~ +33%

PKG size difference (6x6 vs. 8x8mm)

Used High thermal EMC

Used TIM material (Ag epoxy)

✓Advanced double side SiP could be enhanced 13% ~ 33% ratio by using high thermal EMC & TIM material to get good thermal dissipation.

Outline

- Introduction
  - ✓ Electronic Devices Trend from Market
  - ✓ Application Sweet Spot & Package Types
- **Advanced Package Technology for 3D SiP**
  - ✓ Test Vehicle: Advanced SiP Design Integration
  - ✓ **Assembly Challenge & Solution**
  - ✓ Reliability Result
- Summary

Process Flow Introduction

Process Flow Sequences

(1) Substrate In-coming

(2) Top Side SMT process

(3) Bottom Side SMT process

(4) Singulation to Tray

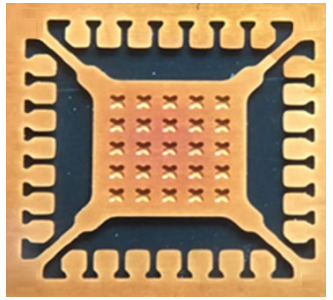
(5) Cu Substrate + TIM Dispensing

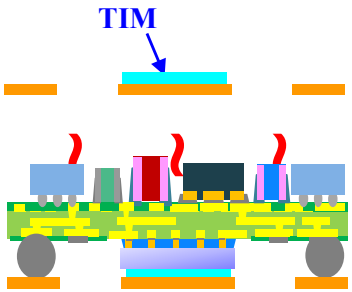
(6) SMT stacking

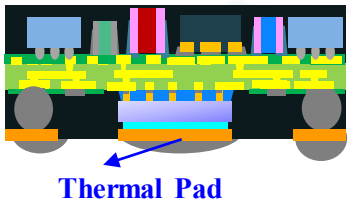
(7) Molding

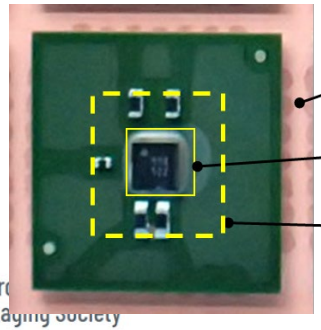
(8) Marking/ Soldering

(9) Singulation/ Test



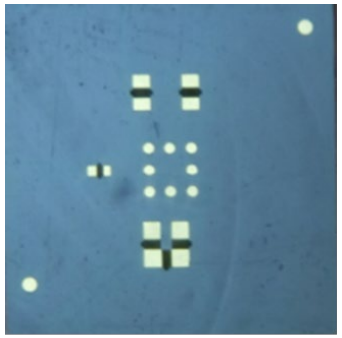




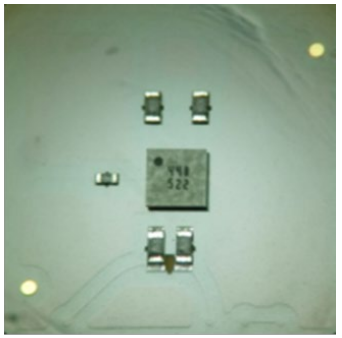


Assembly Result of 3D SiP with Antenna

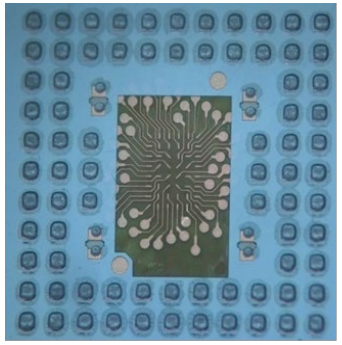
➢ SMT Assembly Result:



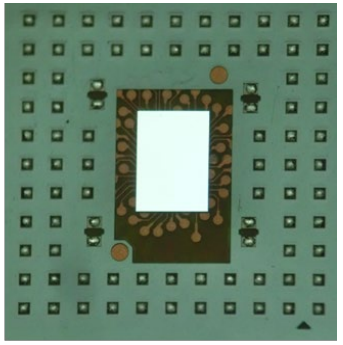
(a) Top side solder printing



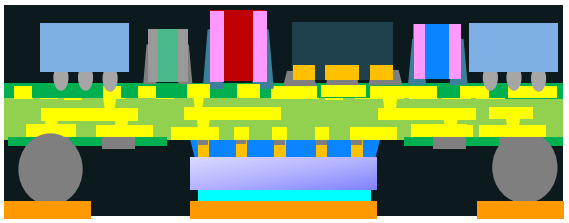
(b) Top side SMT process



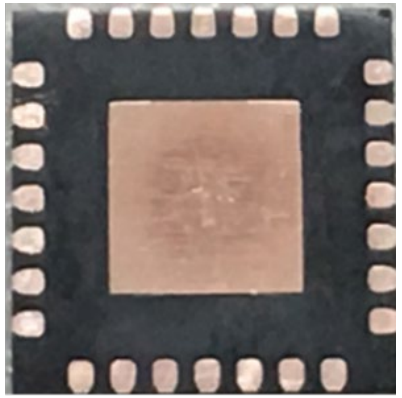
(c) Bottom side ball placement



(d) Bottom side die attached



(a) Top side



(b) Bottom side

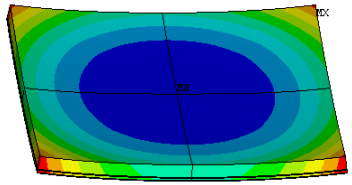
(c) Side view of 3D double side SiP

✓Demonstration result of advanced double side SiP for top side /bottom side SMT placement process result!!

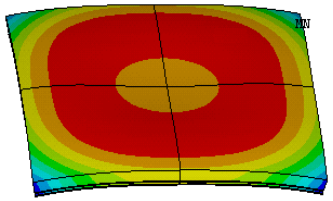
3D SiP of Warpage Performance

3D SiP

What's Major Challenge?



Smiling @ 25C



Crying @260C

Challenge

→ *Package Warpage Behavior by using Double Side SiP Structure*

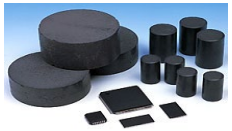
Guideline in Package Simulation Analysis

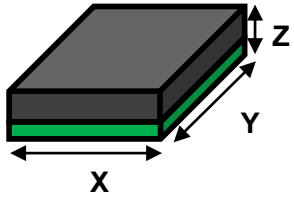
- Package Design - through CAE simulation

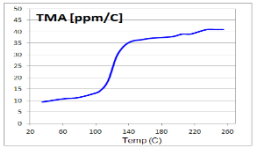
Package Structure

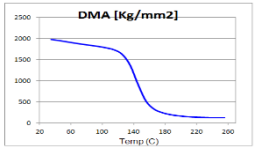
Simulation Model
(Quarter)

- *Structure definition – Dimension?*
- *Material selection*
- *CTE & Modulus Balance*



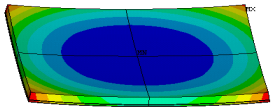




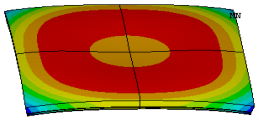


- Simulation output:

  Warpage trend & improvement direction



Smiling @ 25C



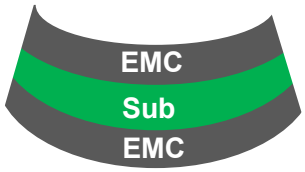
Crying @260C

Ideas for 3D SiP Warpage Analysis

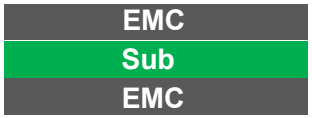
➢ Package Warpage behavior:

CTE factor

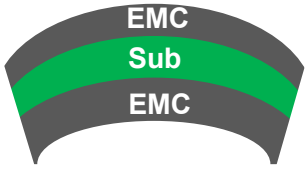
Top BTM
EMC : Sub : EMC



1 : 1 : 0.5

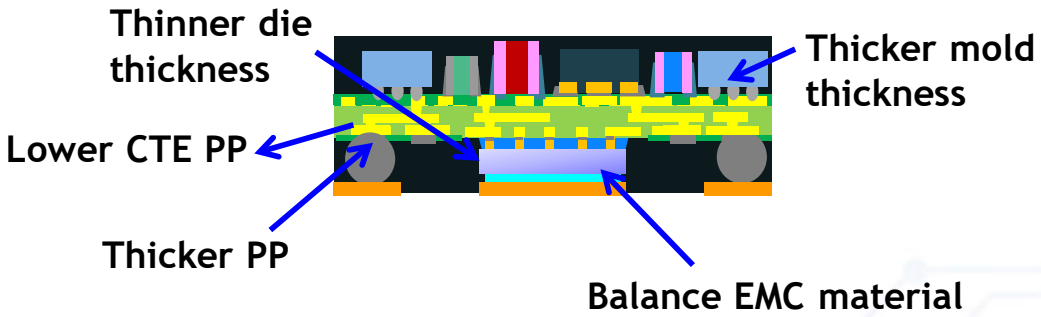


0.5 : 1 : 0.5



0.5 : 1 : 1

Item	Key factors	Level
Package Design	Mold thickness	↑
	Die thickness	↓
Substrate design	PP CTE	↓
	PP thickness	↑
Material	EMC CTE	Balance



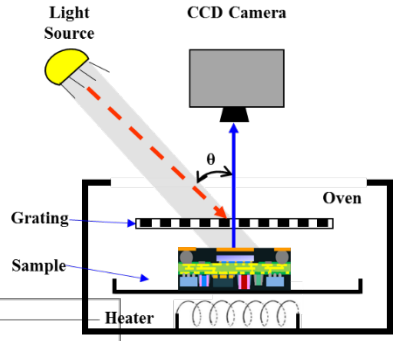
✓Advanced double side SiP could be enhanced warpage by KEY factors from Package, Substrate structure to get better warpage balance structure.

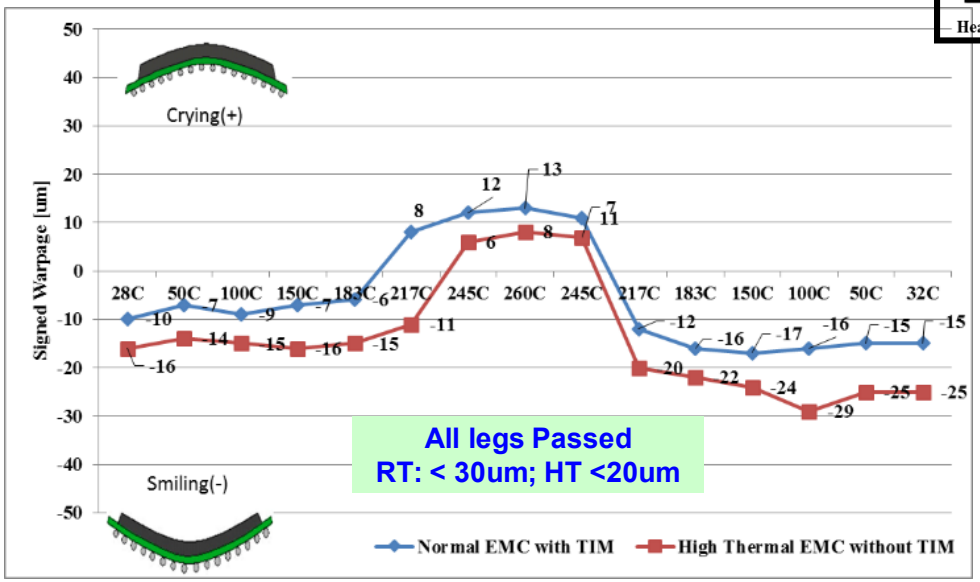
3D SiP Assembly Warpage Verification

➢ Warpage DOE study verification:

EMC type	Normal EMC	High Thermal EMC	Thermal Interface Material
Thermal Conductivity (W/mk)	<1W	2.5W	15W
CTE (ppm/°C)	~10	~15	~20

➢ Shadow Moire Measurement:





✓ The normal EMC with TIM got better warpage result than high thermal EMC without TIM due to low CTE mis-match from double side molding structure.

✓ All legs are within JEDEC warpage requirement (Max. 80um).

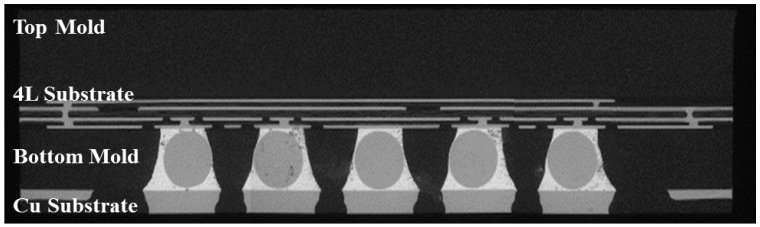
Outline

- Introduction
  - ✓ Electronic Devices Trend from Market
  - ✓ Application Sweet Spot & Package Types
- **Advanced Package Technology for 3D SiP**
  - ✓ Test Vehicle: Advanced SiP Design Integration
  - ✓ Assembly Challenge & Solution
  - ✓ **Reliability Result**
- Summary

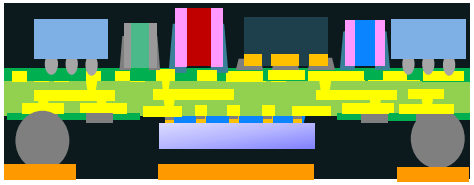
3D SiP Reliability Test Validation Result

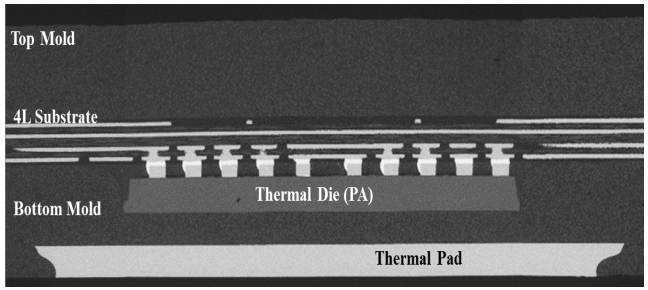
➢ Package Level Reliability Result:

#	Reliability Test Items	Read Point	Sample size	O/S Test and SAT Result
1	Time Zero	T0	0 / 231pcs	All Pass
2	MSL3	Precon	0 / 154pcs	All Pass
3	TCT (-55 ℃ ~+125 ℃)	1000 Cycles	0 / 77pcs	All Pass
4	u-HAST (130℃/85%RH)	96 Hours	0 / 77pcs	All Pass
5	HTS (150℃)	1000 Hours	0 / 77pcs	All Pass

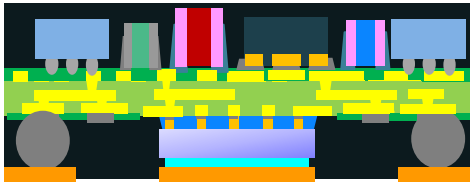


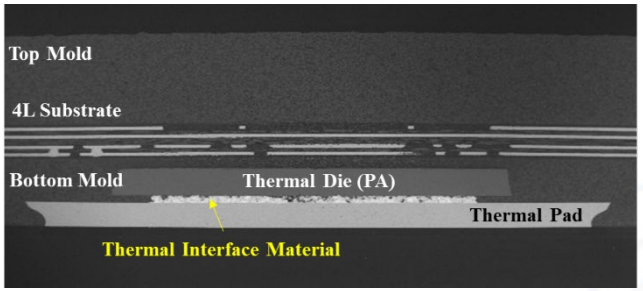
➢ Thermal Die without TIM material:





➢ Thermal Die with TIM material:





➢ Advanced SiP with thermal solution had passed standard JEDEC reliability test requirement.

Outline

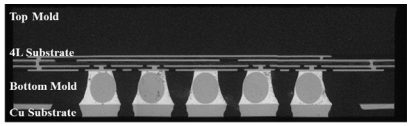
- Introduction
  - ✓ Electronic Devices Trend from Market
  - ✓ Application Sweet Spot & Package Types
- Advanced Package Technology for 3D SiP
  - ✓ Test Vehicle: Advanced SiP Design Integration
  - ✓ Assembly Challenge & Solution
  - ✓ Reliability Result
- **Summary**

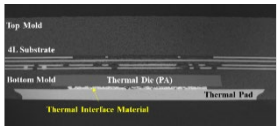
Summary

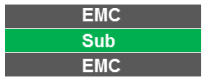
- The benefits of 3D Double Side SiP Integration Technology especially for 5G!!
  - Small form factor with High integration approach
  - High electrical and Good thermal performance

- 3D Double Side SiP structure has been successful demonstration process verification and reliability test for production.

- 3D Double Side SiP could be enhanced warpage by KEY factors from Package, Substrate structure simulation, material selection and process parameter fine-turn to get better warpage balance structure.







0.5 : 1 : 0.5

- *NEXT Focus—*
  - ➔ *Continue to drive Package development trend with more NEW Integration Solution together!!*

(ex. Antenna Integration, *Partition EMI shielding)*

000526

Q&A

Thank You For Your Attention!!!