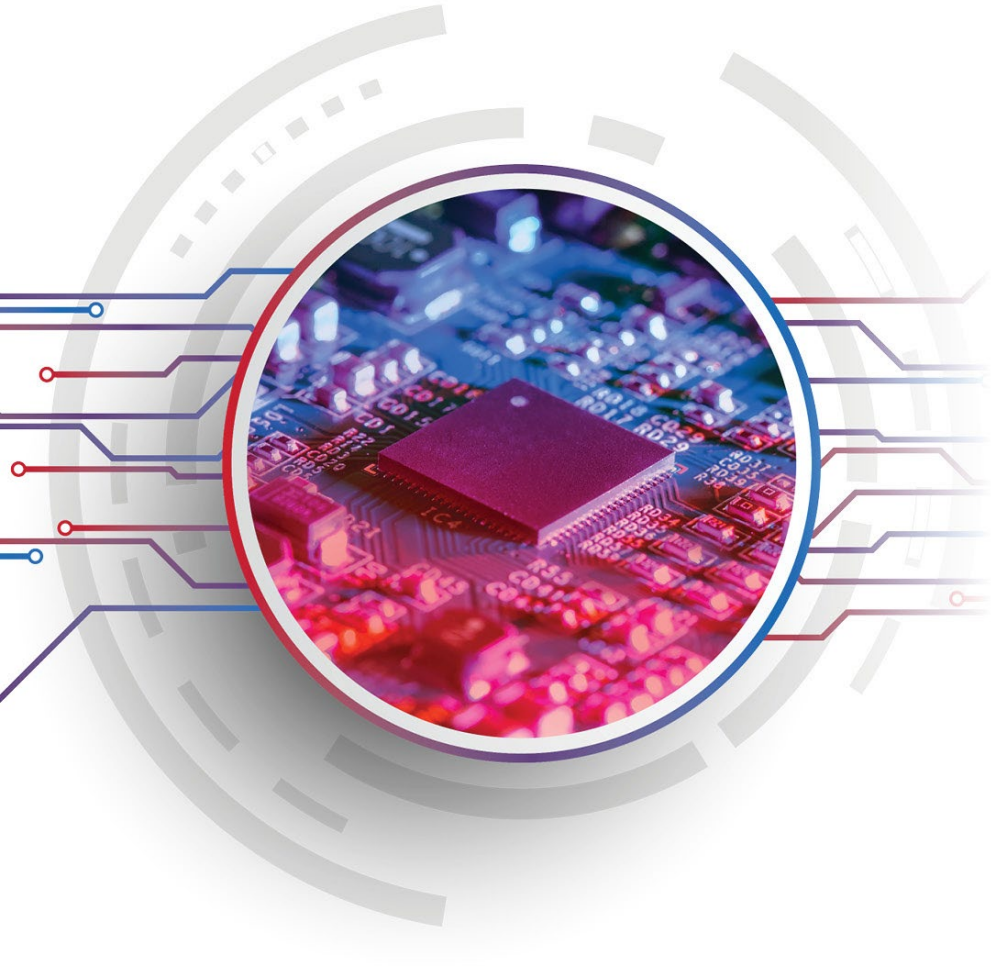

Embedded Trace and RDL Copper Plating Process for Panel Level Packaging Applications

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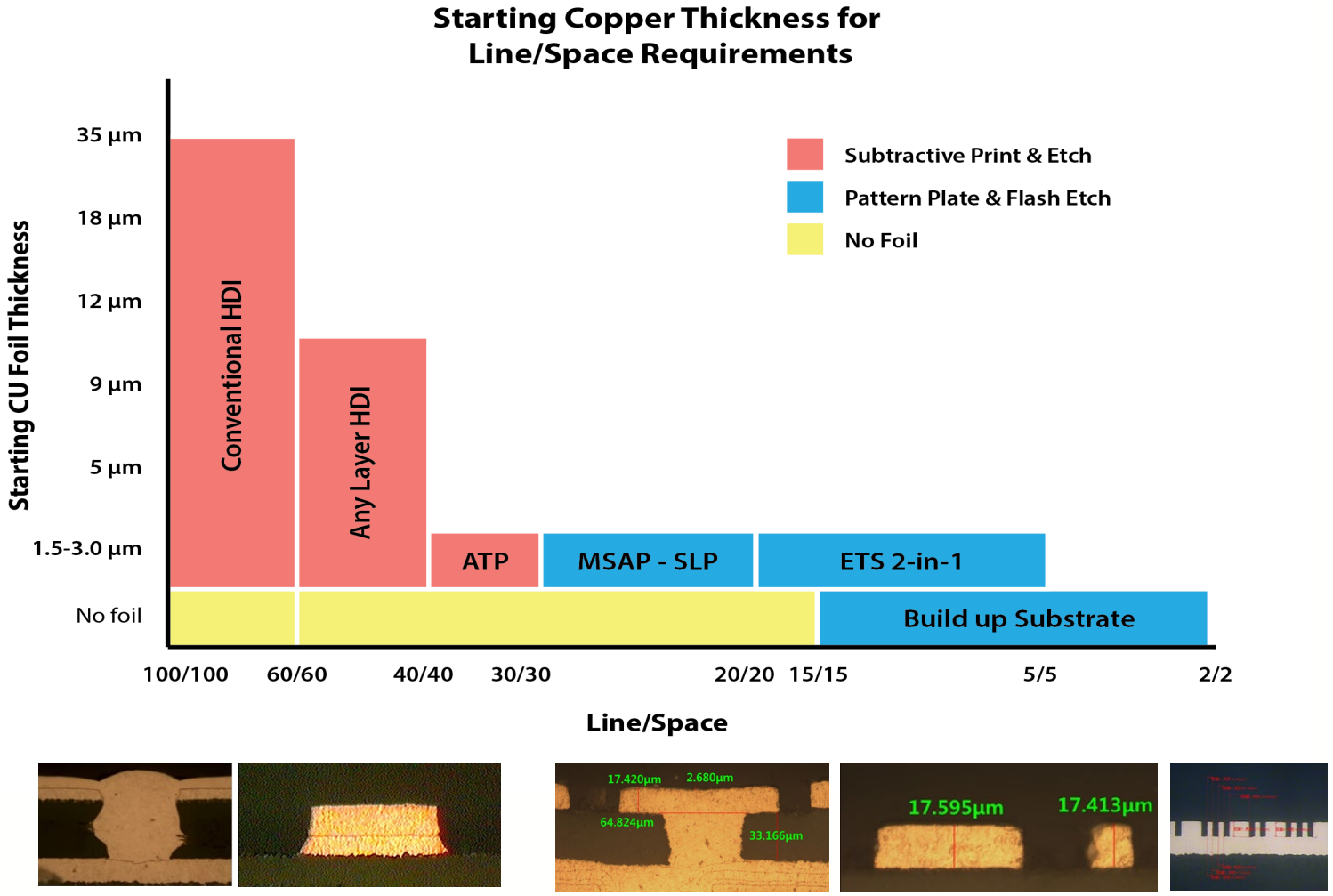
MacDermid Alpha ELECTRONICS SOLUTIONS

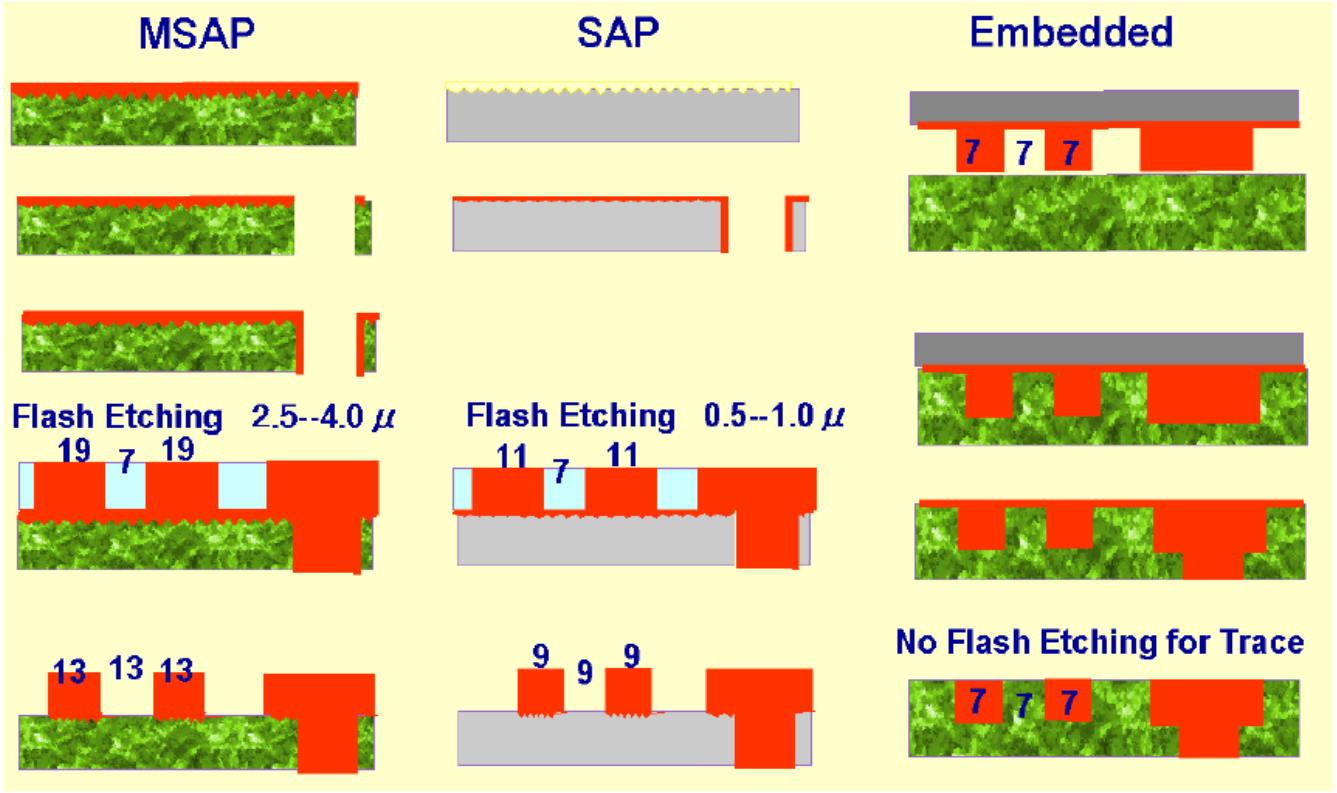
Outline

- Introduction
  - Requirements of fine line resolution with different applications
  - Technologies for fine line formation − SAP, mSAP and ETS
  - Challenges of fine line plating by panel level approach for IC substrate
- Systek ETS process for fine line plating and 2-in-1 RDL plating
  - Electrolyte and plating tools
  - Fine line formation capability
  - Key factors that influence plating uniformity
- Systek UVF process for 2-in-1 RDL plating
  - Filling larger vias
  - Via fill and fine line plating capability

HDI Trends in L/S Requirements



Comparison on Technologies

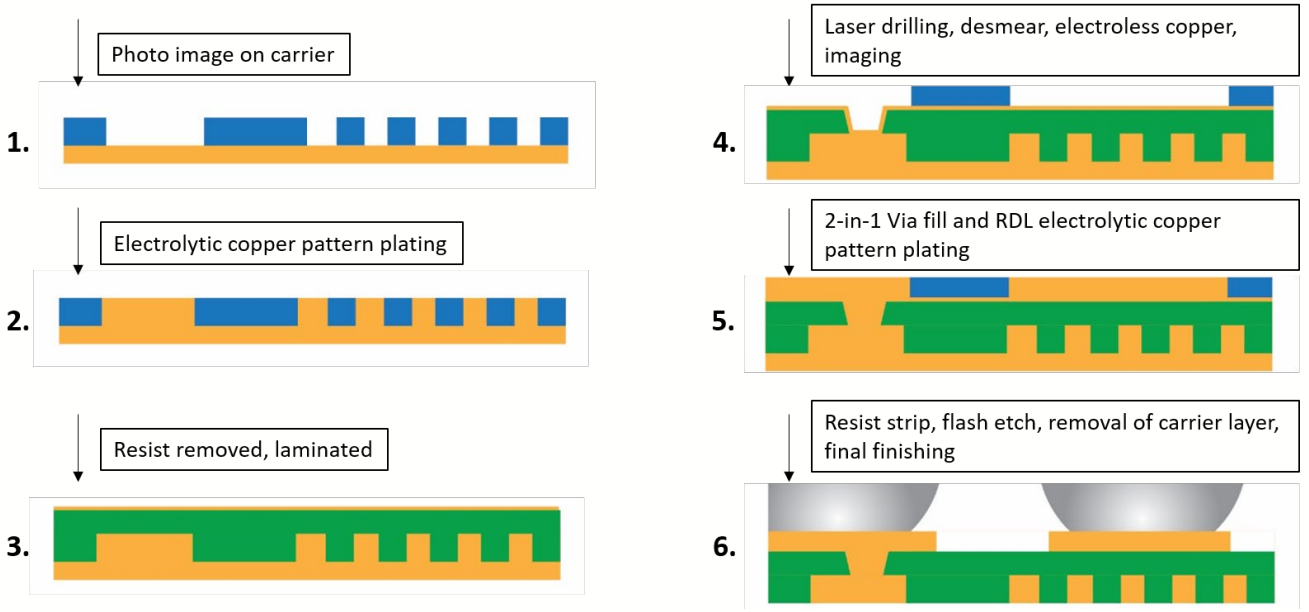


SAP: Semi-Additive Processing. Additive seed layer Pattern plating.
MSAP: Modified Semi-Additive Processing. Thin Cu foil. Pattern Plating
ETS: Embedded Trace Substrate. Cu pattern plating on carrier.

Source: Mitsubishi/MGC

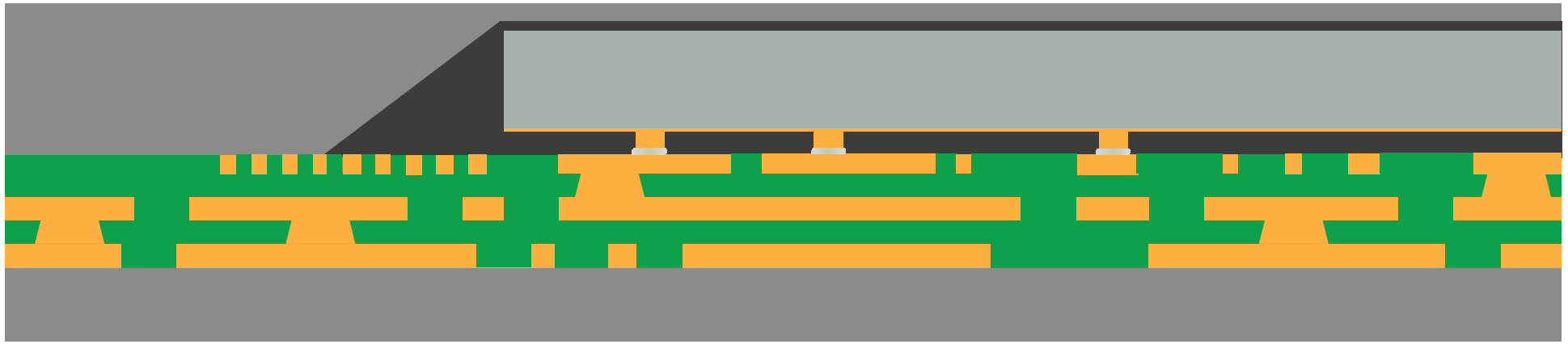
Embedded Trace & mSAP for IC Substrate

- Embedded trace substrate (ETS) technology involves using photo lithography to pattern photoresist onto a conductive carrier, electrolytic copper pattern plating to form fine lines. Fine line traces are then laminated onto dielectric embedding the circuits to form M1 layer.
- mSAP process utilizes electrolytic copper pattern plating to fill vias and to plate RDL fine lines simultaneously, in what is called 2-in-1 RDL plating (M2 layer & M3 layer).



PLP (Panel Level Package) Substrates

- M1 layer is formed by embedded trace processing, pattern plated with Systek ETS electrolyte for fine line formation
- M2 and M3 RDL layers are formed by mSAP processing, pattern plated with either Systek ETS electrolyte or Systek UVF electrolyte for 2-in-1 via fill & RDL plating

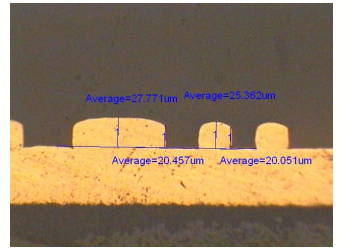


- **Embedded trace substrate (ETS)**
  - L/S 5-10 µm
  - Up to 20 µm Cu thickness
- **2-in-1 RDL by mSAP**
  - L/S 15-25 µm, via at 60 x 40 µm
  - Up to 20 µm Cu thickness

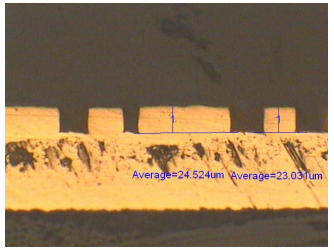
Challenges of Fine Line Plating

Panel based approach is to reduce cost and increase throughput, but the production has been limited

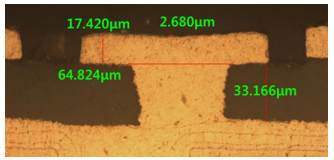
- Cost reduction & technology limitation
- Technical challenges from acid copper plating process
  - Coplanarity on fine lines, pads and vias – 2-in-1 RDL
  - Feature profile – plated bump shape
  - Uniformity within panel
  - Plated copper physical properties – Reliability
  - Operation range
    - Tool/chemistry interaction
    - Wide operation window
  - The cause of poor plating performance
    - Variation of CD distribution
- Solutions
  - Additives in an electrolyte play key role in reducing CD variation
  - Plating tool design, the type of anodes, VMS, plating CD, board design



- Plated height difference
- Domed bump

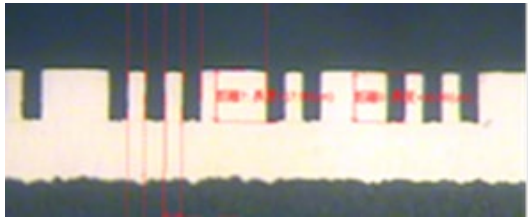


- Plated height consistence
- Flat surface



PLP Fine Line Plating Process – Systek ETS

- Systek ETS, in a Vertical Continuous Plater, can offer fine line 5 µm



Process Cycle and Operating Parameters

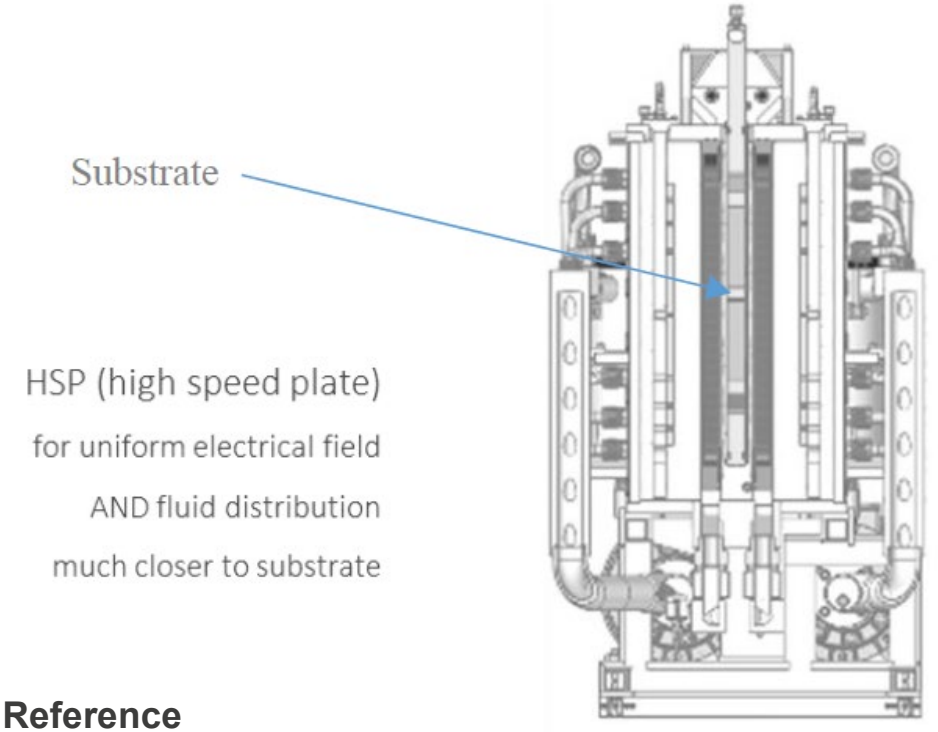
Acid Cleaner → **Water Rinse** → **Acid Dip** → **Acid Copper Electrolyte Systek ETS**

Electrolyte Make-up

ETS	Chemistry	Concentration	Function
VMS	$CuSO_4$	100 g/L	Source of copper ion
	H_2SO_4	200 g/L	Conductivity, prevents the precipitation of basic salts
	Cl^-	60 ppm	• Enhance the adsorption and inhibition effect of the wetter; act as binding sites for the polyglycols • Secondary accelerator • Affect the appearance, structure, and internal stress
Additives	Wetter	5 ml/L	Wetting and suppressing function and grain refining agent
	Brightener	2.5 ml/L	Anti-suppressor, it is also called accelerator
	Leveler	10 ml/L	Secondary suppressor, key for the uniformity & performance
Parameter	CD	1.0-4.0 ASD	
	Temp	20-27 ºC	

PLP Fine Line Plating Equipment – VHS-P

- Vertical High Speed Panel (VHS-P) Plater – Fine line down to 2 µm
  - Uniform injection of electrolyte onto substrate surface with high flow rate
  - Uniform electrical field close to the substrate surface
  - RDL fine line resolution down to 2 µm with panel uniformity < 10%
  - Single panel each time, unsuitable for high volume production

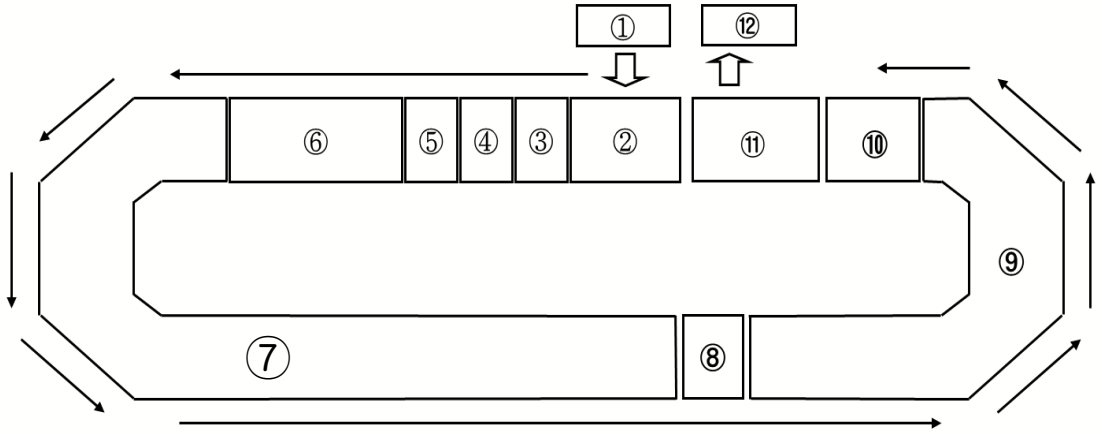


Reference

"Fine line panel level plating technology," *Herbert Otzlinger, Claudia Landstorfer, Tetsuya Onishi, Christian Dunkel and* ***Raoul Schroeder****, IMPACT, 2018*

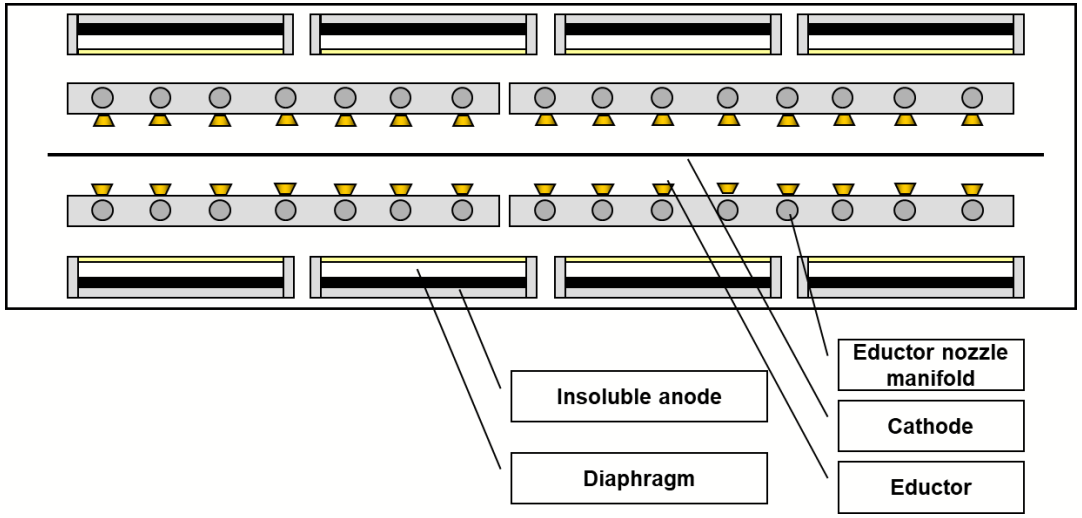
PLP Fine Line Plating Equipment – VCP

- Vertical Continuous Plater (VCP) for high volume production – Fine line down to 5 µm
  - Panels progress along the tank, pass by each anode and nozzle manifold, which provides consistent plating results by “average” out.
  - Systek ETS electrolyte is able to offer fine line resolution down to 5 µm on a pilot VCP line, 7-10 µm in high volume production.



① Load ② Acid Clean ③ Rinse ④ Rinse ⑤ Rinse
⑥ Acid dip ⑦ ETS Acid Copper Plating ⑧ DI Rinse
⑨ Antitarnish ⑩ DI Rinse ⑪ Dryer ⑫ Unload

Top view of VCP plating line

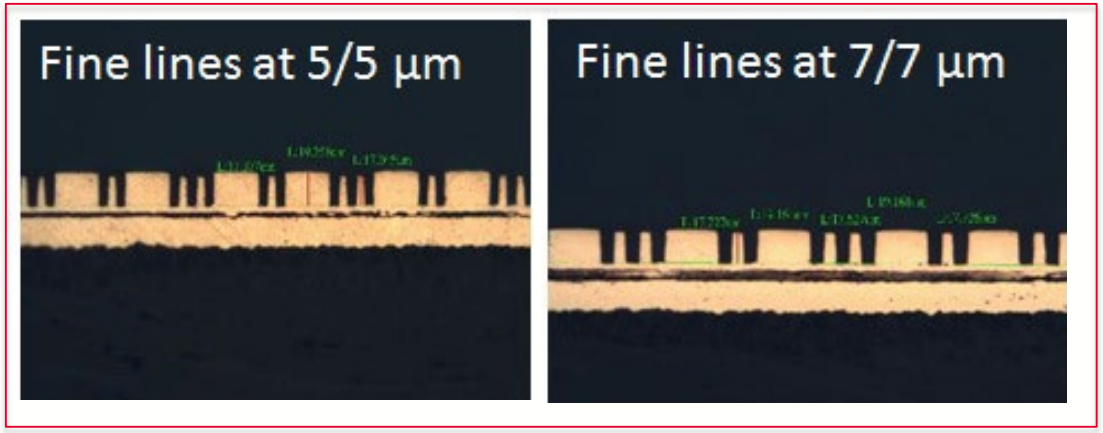


Anode Influence, Insoluble vs Soluble Anode

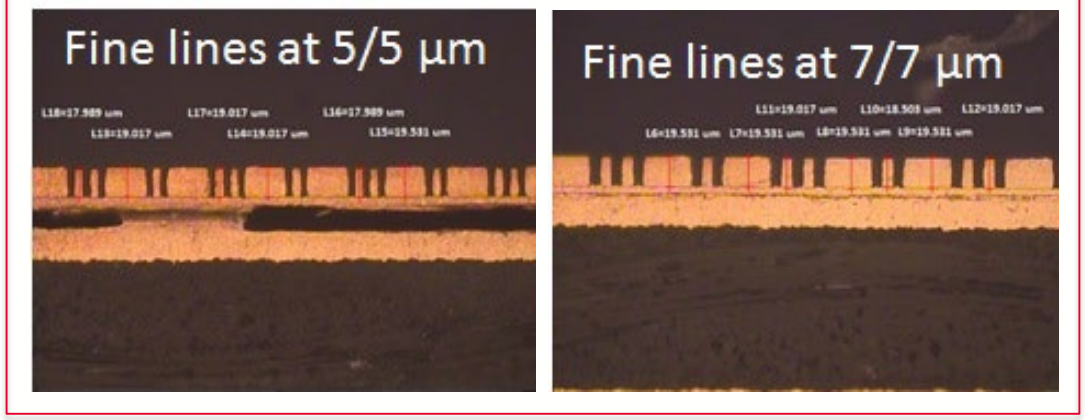
- VCP with insoluble anodes offers higher uniformity, CD at 1.5 ASD/60 min
- Flat even copper surface, less variation on plated height between fine lines and pads

Systek ETS soluble anode	Line (20um)				Pad (20um)				R
T/S (um)	1	2	3	avg.	1	2	3	avg.	(line-pad)
7/7	17.82	18.03	17.73	17.86	19.45	19.16	19.16	19.26	1.40
5/5	17.14	17.86	17.37	17.46	20.14	19.55	19.26	19.65	2.19
Systek ETS insoluble anode	Line (19um)				Pad (19um)				R
T/S (um)	1	2	3	avg.	1	2	3	avg.	(line-pad)
7/7	19.02	18.5	19.02	18.85	19.53	19.53	19.53	19.53	0.68
5/5	17.99	19.02	17.99	18.33	19.02	19.02	19.53	19.19	0.86

With soluble anodes

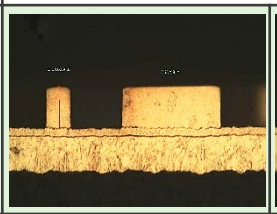
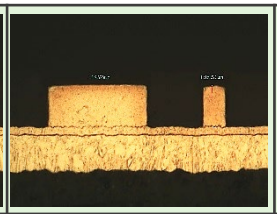
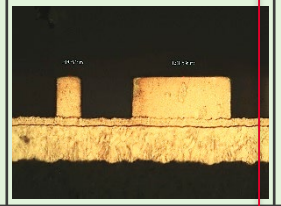
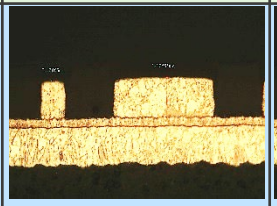
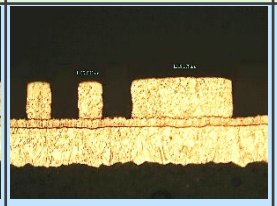
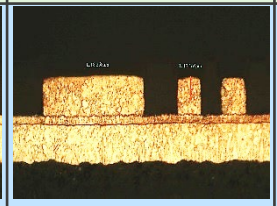
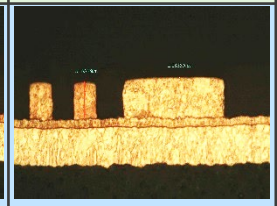
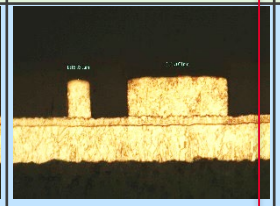


With insoluble anodes



CD Influence

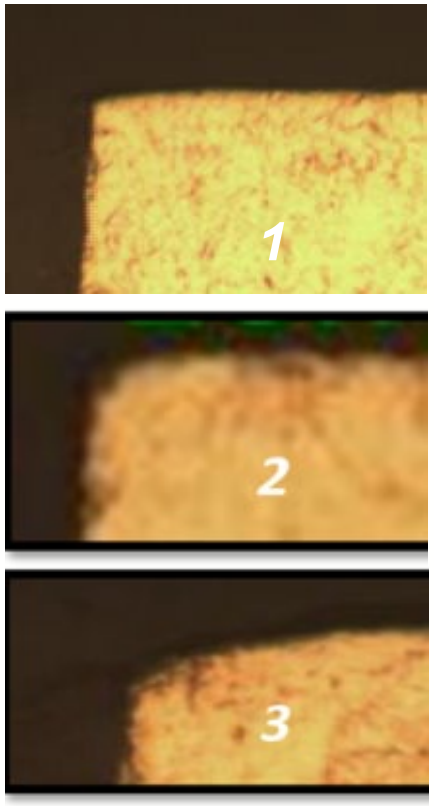
- Fine lines at 10 µm, the plated height variation below 0.5 µm, CD at 1.5 ASD/60 min
- Fine lines at 10 µm, the plated height variation around 1.0 µm, CD at 4 ASD/22 min

Test		Cross-section					R
1.5 ASD							Average
	Line	18.36	18.00	18.27	17.78	18.49	0.37
	Pad	18.76	18.54	18.63	18.27	18.54	
4.0 ASD							
	Line	17.07	17.07	17.07	16.80	16.93	1.09
	Pad	17.56	18.18	18.27	18.36	18.00	

VMS Influence

- Higher sulfuric acid, less variation between fine lines and pads
- Higher sulfuric acid, sharper trench

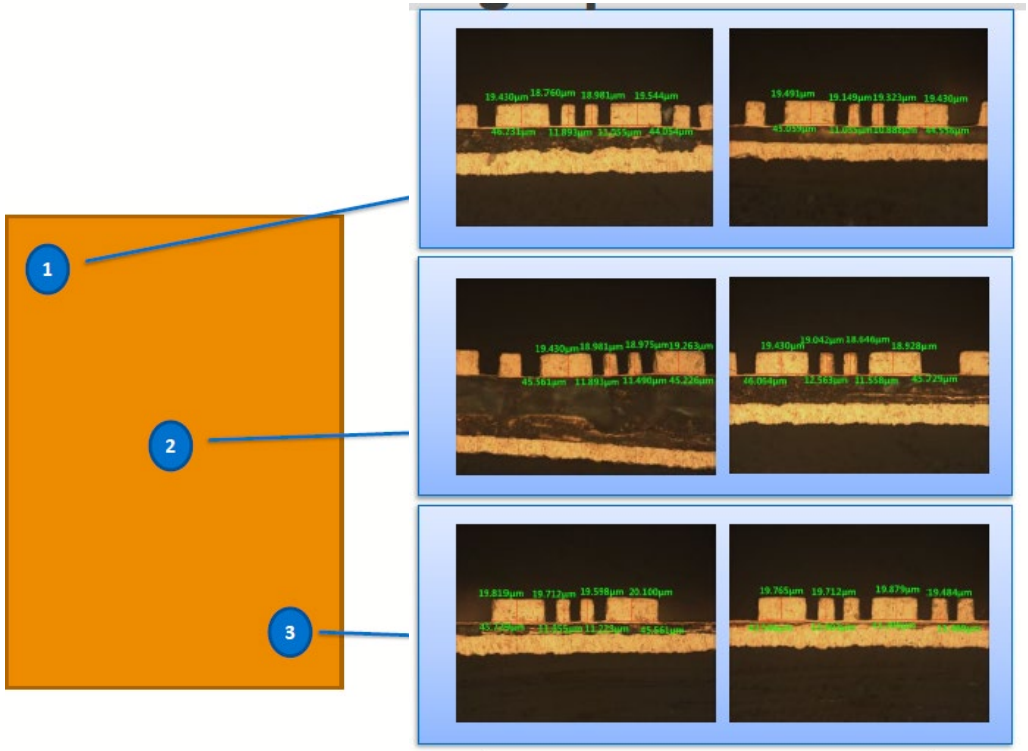
Plating bath	Chemical	DOE 1	DOE 2	DOE 3
VMS	$CuSO_4$	100 g/L	150 g/L	200 g/L
	H_2SO_4	200 g/L	150 g/L	100 g/L
	Cl^-	60 ppm	60 ppm	60 ppm
Additive	Wetter	5 ml/L	5 ml/L	5 ml/L
	Brightener	2 ml/L	2 ml/L	2 ml/L
	Leveler	10 ml/L	10 ml/L	10 ml/L
Deviation R within the unit (Average)		***0.33 μm***	***0.47 μm***	***0.49 μm***



VMS Influence

- Panel size, 410 x 510 mm, cross sections on 3 areas after plating
- VMS with high copper & low acid
- Great uniformity within unit as well as within panel

VMS	$CuSO_4$	H_2SO_4	Cl^-
3	200 g/L	100 g/L	60 ppm

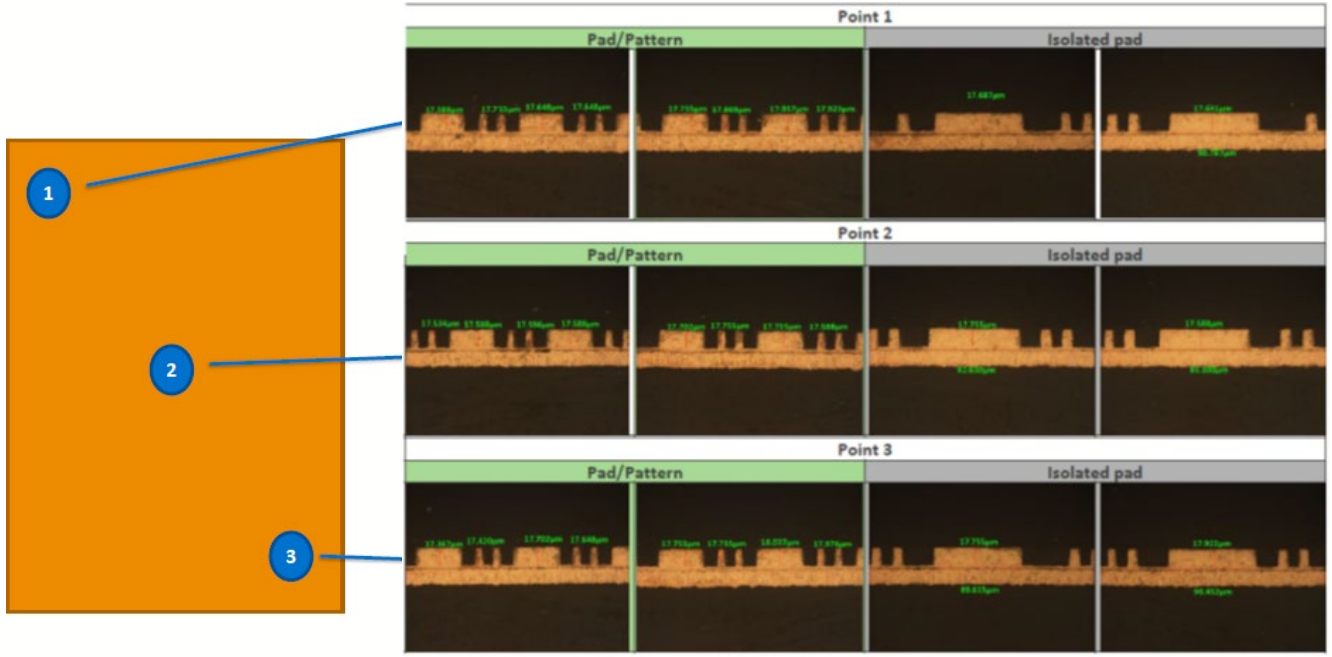


	Fine Line thickness (µm)					Pad thickness (µm)					Thickness variation
	1	2	3	4	Average	1	2	3	4	Average	
Top	18.76	18.98	19.15	19.32	19.05	19.43	19.54	19.49	19.43	19.47	0.42
Center	18.98	18.99	19.04	18.65	18.92	19.43	19.26	19.43	18.93	19.26	0.34
Bottom	19.71	19.60	19.71	19.48	19.63	19.82	20.10	19.77	19.88	19.89	0.26

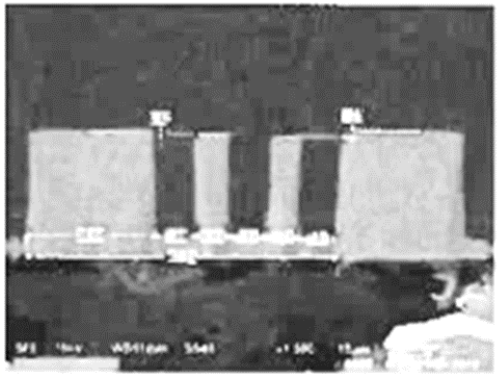
VMS Influence

- Panel size, 410 x 510 mm, cross sections on 3 areas, fine lines at 5 µm
- VMS with higher sulfuric acid
- Excellent uniformity within unit as well as within panel, very sharp trench

VMS	$CuSO_4$	H_2SO_4	Cl^-
4	50 g/L	250 g/L	60 ppm

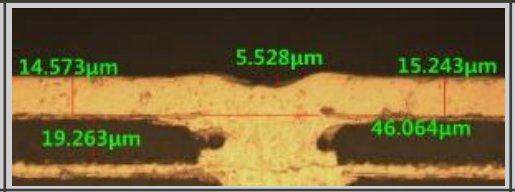
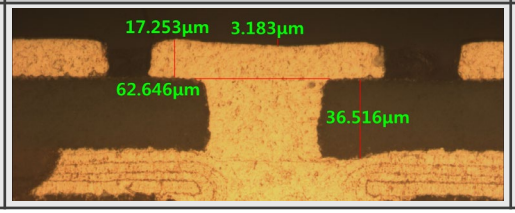


	Fine Line thickness (µm)	Pad thickness (µm)	Thickness variation
	Average	Average	
Top	17.80	17.74	0.06
Center	17.62	17.69	0.07
Bottom	17.70	17.72	0.02



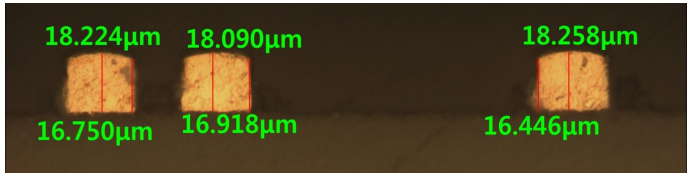
Systek ETS Electrolyte for 2-in-1 RDL

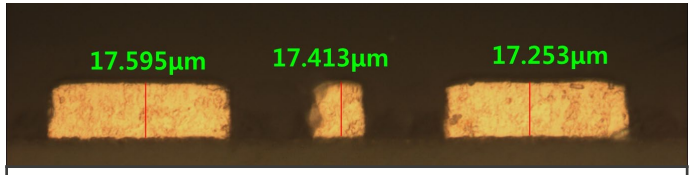
2-in-1 RDL pattern plating, small via in RDL design. Vertical Continuous Plater

VMS	$CuSO_4$	H_2SO_4	Cl^-	Via Fill V	Via size/Dimple
3	200 g/L	100 g/L	60 ppm		50 x 20 µm /5.5 µm
5	220 g/L	50 g/L	60 ppm		60 x 40 µm /3.1 µm

Dimple (µm)			
3.18	2.51	3.52	3.35
Max	3.52	Ave.	3.14

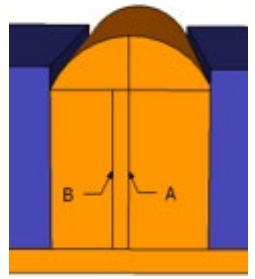
Fine Pattern (µm), fine line 15 µm		
18.22	18.09	18.26
Pad & Pattern (µm)		
17.60	17.41	17.25
Deviation between Fine and Pad R @ 1.01 µm		





Pattern Shape (%)			
8.09 %	6.48 %	9.92 %	
Max	9.92%	Ave	8.16%

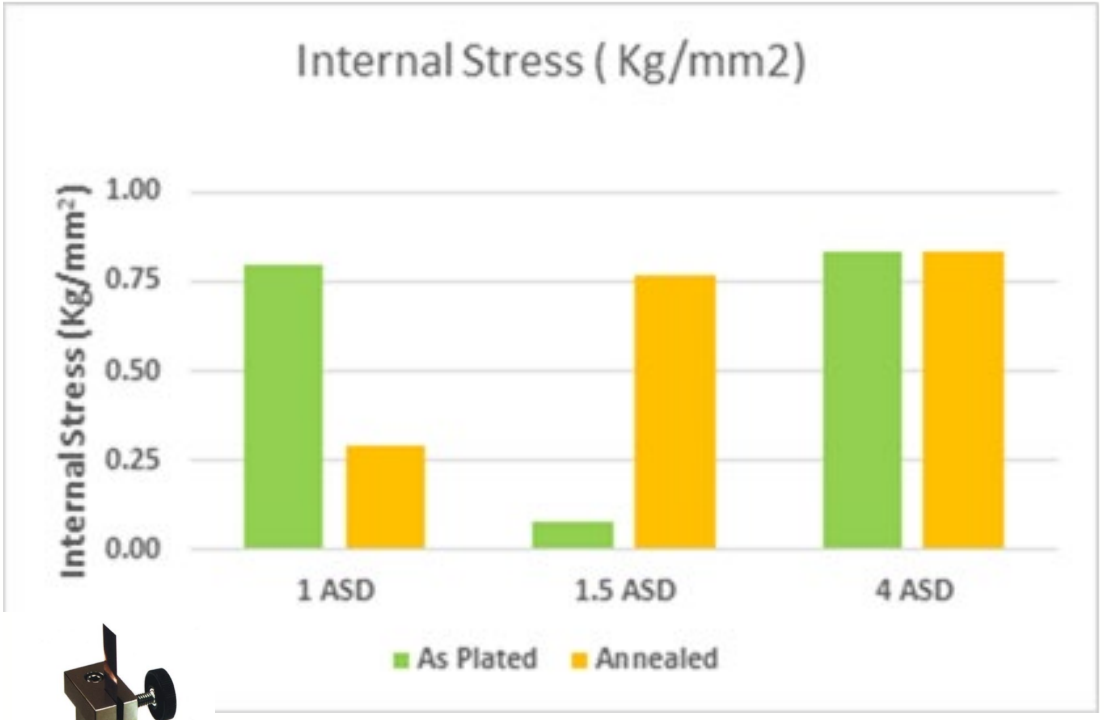
Plated Cu



Profile % = (A-B)/A*100

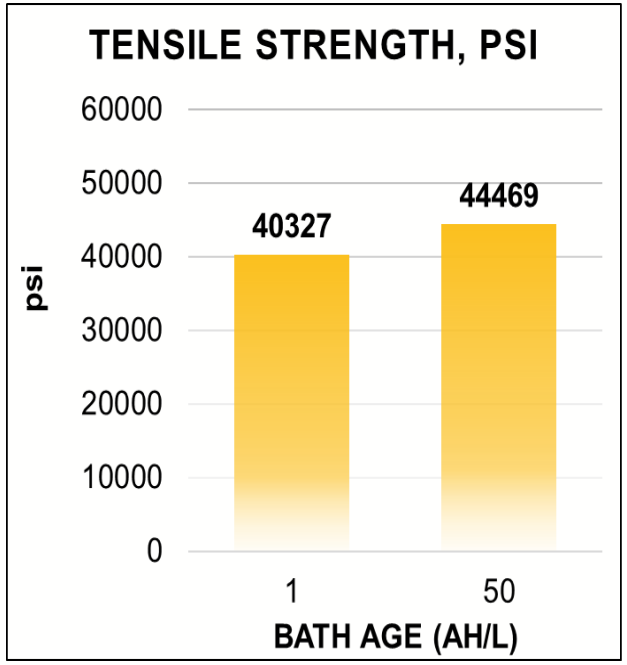
Physical Properties, Low Internal Stress

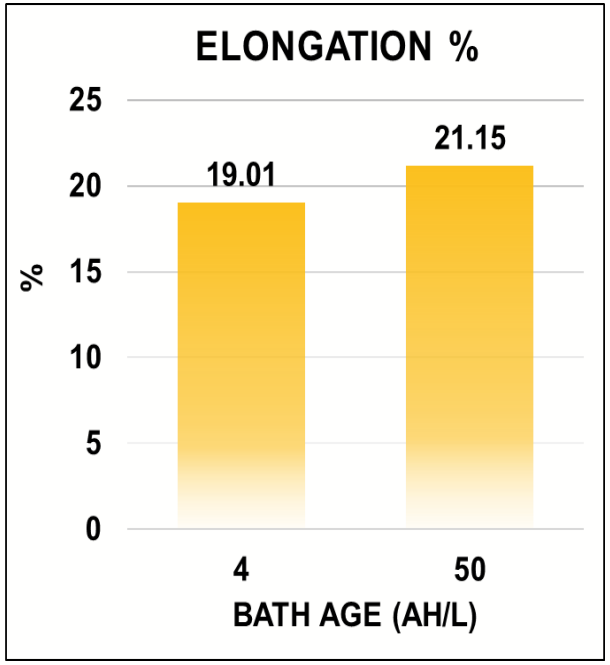
1. Soak a test strip in a soak cleaner solution at 110-120 °F for up to 30 seconds then water rinse.
2. Dry completely and weigh the test strip.
3. Clip a weighed test strip to the stainless steel cross support so the test strip is centered between the cell walls.
4. The test strip leg tips should be approximately 1/16 of an inch or 3 mm from the plating cell bottom.
5. Plate the strip at desired current density for desired time to achieve the Cu thickness necessary
6. Rinse the strip with water and dry very carefully with low pressure air.
7. Mount the strip on the measuring stand (Deposit Stress Analyzer).
8. Read and record the total increments spread on both sides of the zero as the value for U.
9. Weigh the plated test strip and record the final weight.
10. Anneal at 130 ºC for one hour



Physical Properties, T&E

- Low internal stress both as plated and annealed at 130 °C for 1h
- Passed the IPC class III criteria, tensile strength greater than 36,000 psi and elongation greater than 18%
- Stable with aged bath

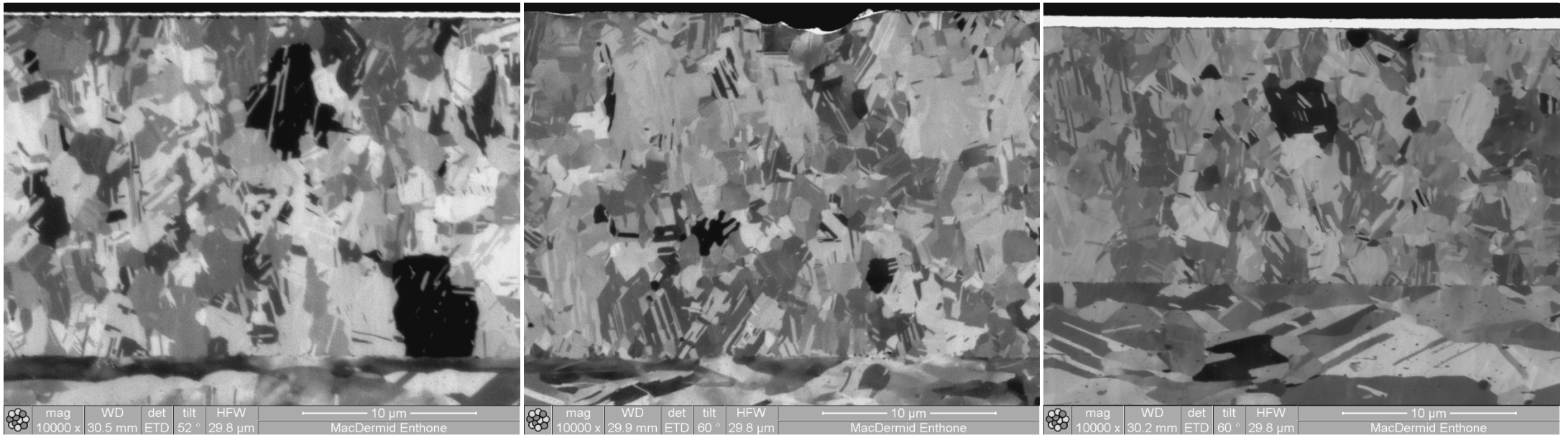




Copper Grain Structure

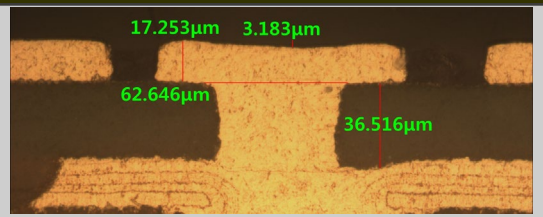
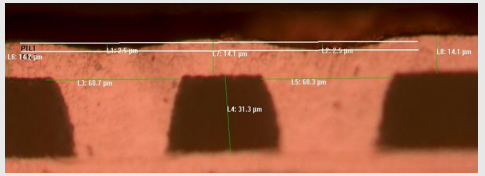
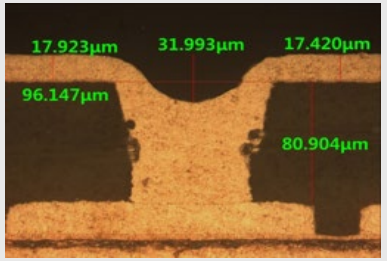
- Consistent grain structure under different plating current density
- Small size, equiaxial grain structure

1.0 ASD	1.5 ASD	4.0 ASD



Via Fill Capability

- Slight dimple under CD @ 1.5 ASD, 60 minutes, it could not be reduced by higher amount of copper sulfate in VMS
- Deep dimple with larger vias.

VMS	$CuSO_4$	H_2SO_4	Cl^-	Via Fill V	Via size/Dimple
5	220 g/L	50 g/L	60 ppm		60 x 40 µm /3.1 µm
6	250 g/L	50 g/L	60 ppm		60 x 40 µm /2.5 µm
6	250 g/L	50 g/L	60 ppm		100 x 80 µm /Deep dimple

Systek UVF

- 2-in-1 RDL pattern plating, larger vias in RDL design. Vertical Continuous Plater

Process Cycle and Operating Parameters

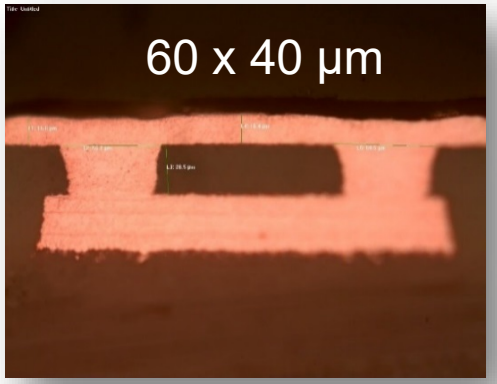
Acid Cleaner → **Water Rinse** → **Acid Dip** → **Acid Copper Electrolyte Systek UVF**

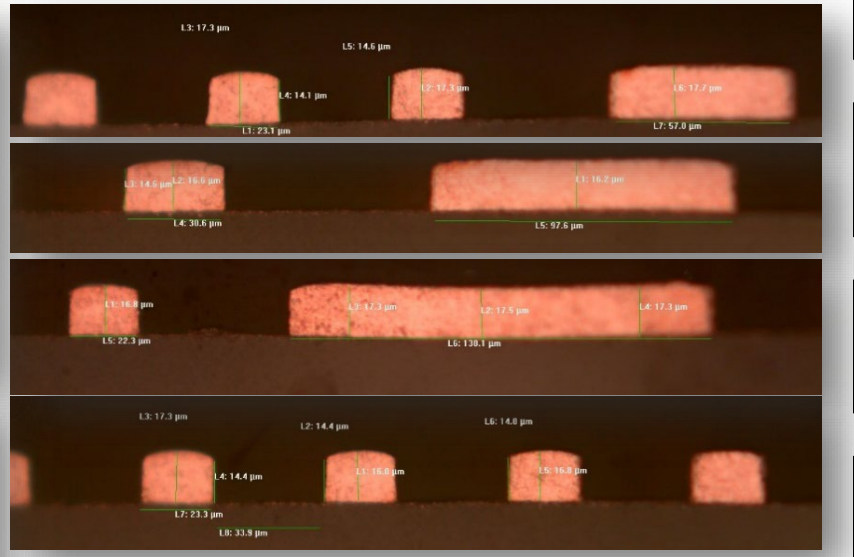
Bath Make-up

UVF	Chemistry	Concentration	Function
VMS	**$CuSO_4$**	**200 g/L**	Source of copper ion
	H_2SO_4	**50 g/L**	Conductivity, prevents the precipitation of basic salts
	Cl^-	**50 ppm**	• Enhance the adsorption and inhibition effect of the wetter; act as binding sites for the polyglycols • Secondary accelerator • Affect the appearance, structure, and internal stress
Additives	**Wetter**	**10 ml/L**	Wetting and suppressing function and grain refining agent
	Brightener	**1.0 ml/L**	Anti-suppressor, it is also called accelerator
	Leveler	**20 ml/L**	Secondary suppressor, key for the uniformity & performance
Parameter	**CD**	**1.0-3.0 ASD**	
	Temp	**20-27 ºC**	

Systek UVF, 2 in 1 RDL for IC Substrate

- Flat filled vias, trace profile below 15% with fine lines, 25 µm. 1.5 ASD/60 min
- Height variation below 0.5 µm with lines, 25 µm, pads, 60-100 µm





Ave. Height pad (µm)	Ave Height Lines(µm)	Ave. R
17.7	17.3	0.4

Ave. Height pad (µm)	Ave Height Lines(µm)	Ave. R
16.6	16.2	0.4

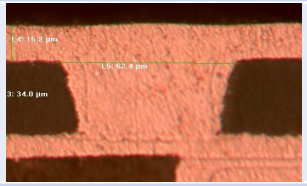
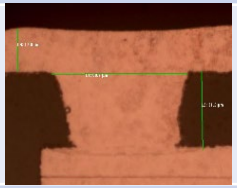
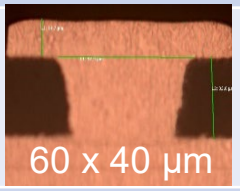
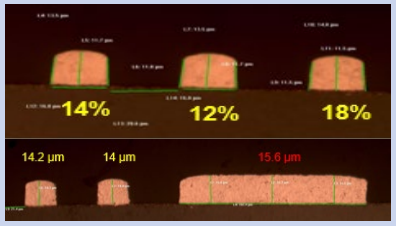
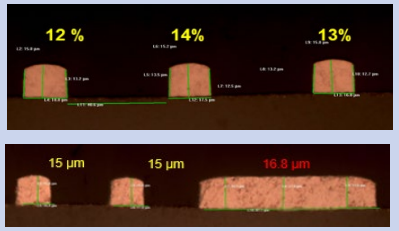
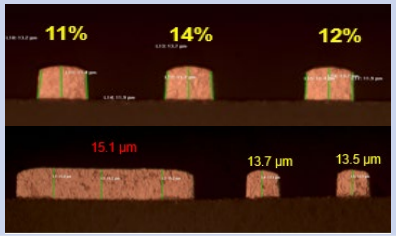
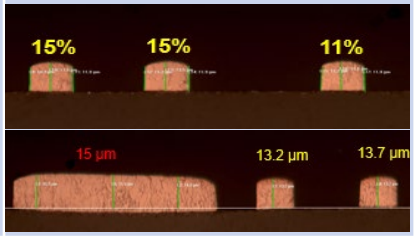
Ave. Height pad (µm)	Ave Height Lines(µm)	Ave. R
17.3	16.8	0.5

L/S	Ave. Height (µm)	Profile
25/35	16.7	15%

L/S	Ave. Height (µm)	Profile
25/50	17	12%

Electrolyte Stability

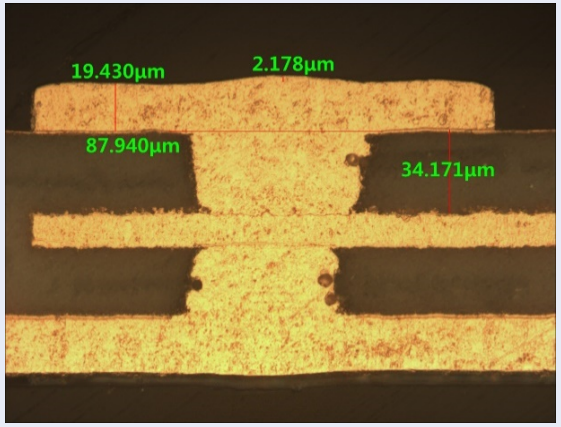
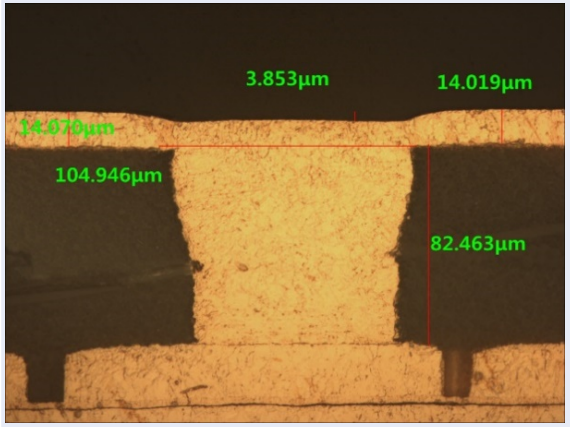
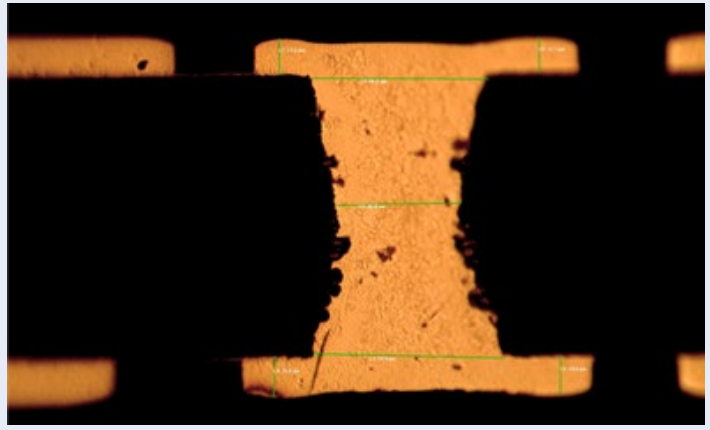
- Flat filled vias, trace profile below 20%with fine lines, 15 µm
- Height variation below 1.6 µm with lines, 15 µm, pads, 100 µm, WID% < 5%
- Consistent performance with aged bath

	Bath Aging Study			
Ah/L	0 Ah/L	50 Ah/L	100 Ah/L	150 Ah/L
Filling (60x40µm)				
Trace 15 µm Pad 100 µm				
Height variation	1.5 µm	1.6 µm	1.5 µm	1.5 µm
WID%	4.4%	4.7%	4.4%	4.4%

$$WID\ \% = (H_{max}-H_{min})/2H_{avg} \times 100\%$$

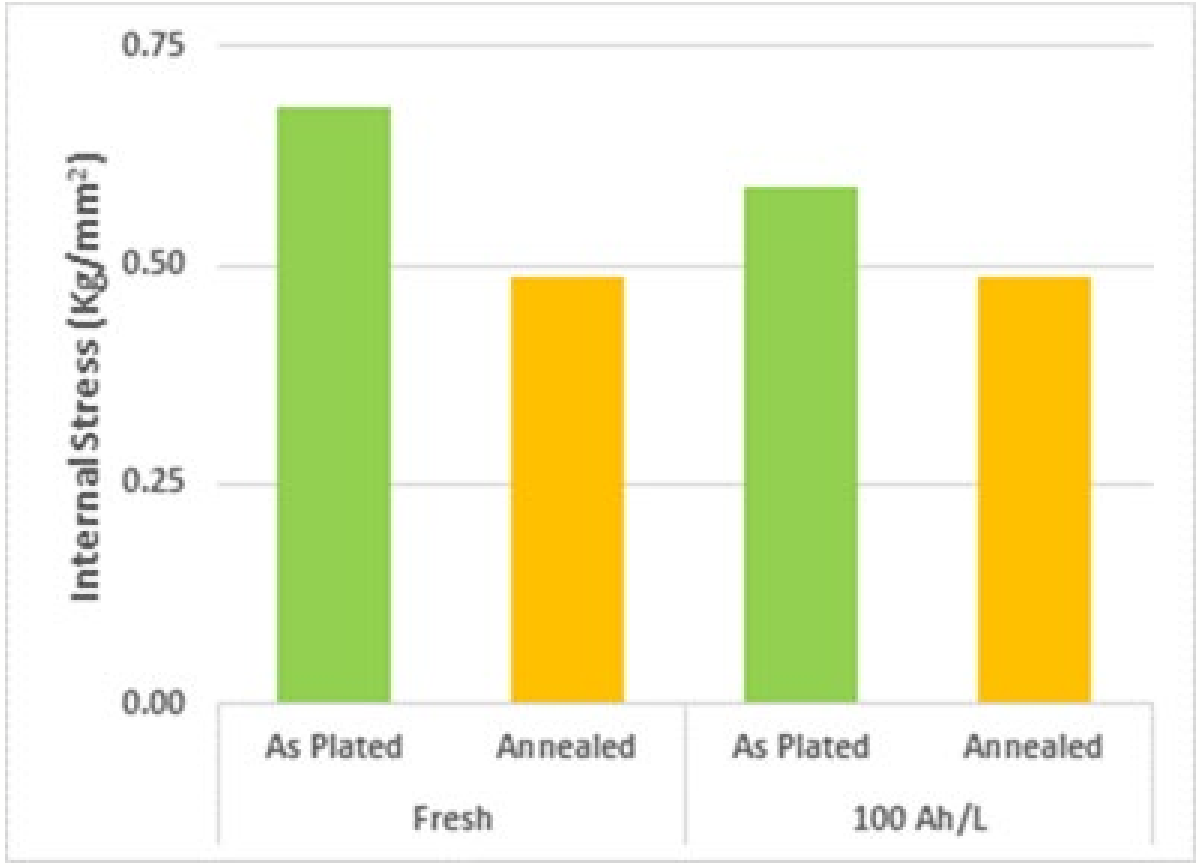
Via Fill Capability

- Slight bump with shallow vias
- Slight dimple, < 5 µm with larger vias, 100 x 80 µm
- Great through via fill capability

	Larger Vias and Through Hole Filling		
Via size	90 x 35 µm	100 x 80 µm	110 x75 µm
			
Dimple	+2.2 µm	3.9 µm	2.0 µm

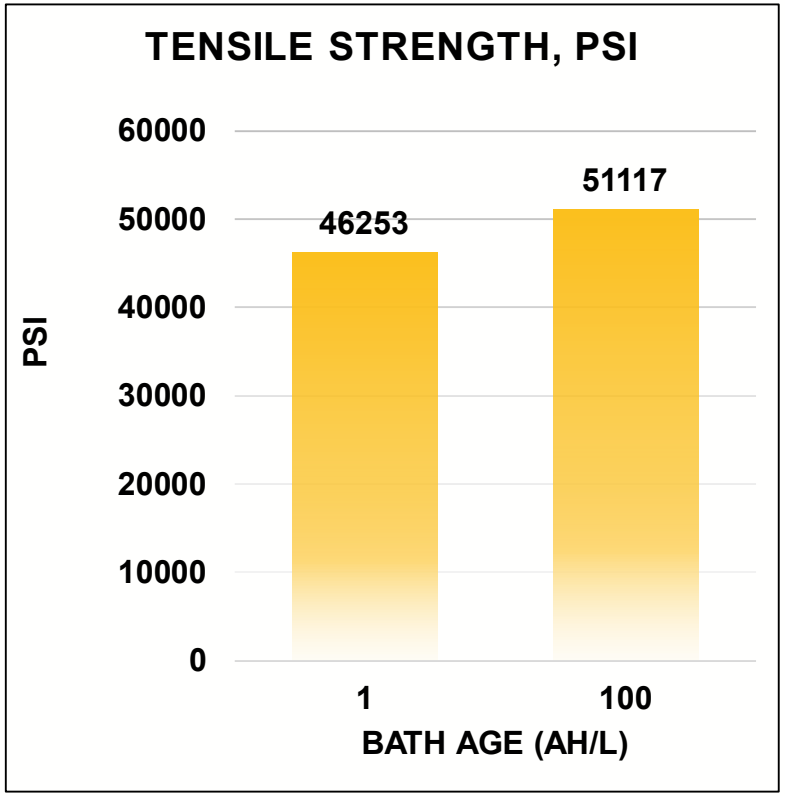
Physical Properties, Low Internal Stress

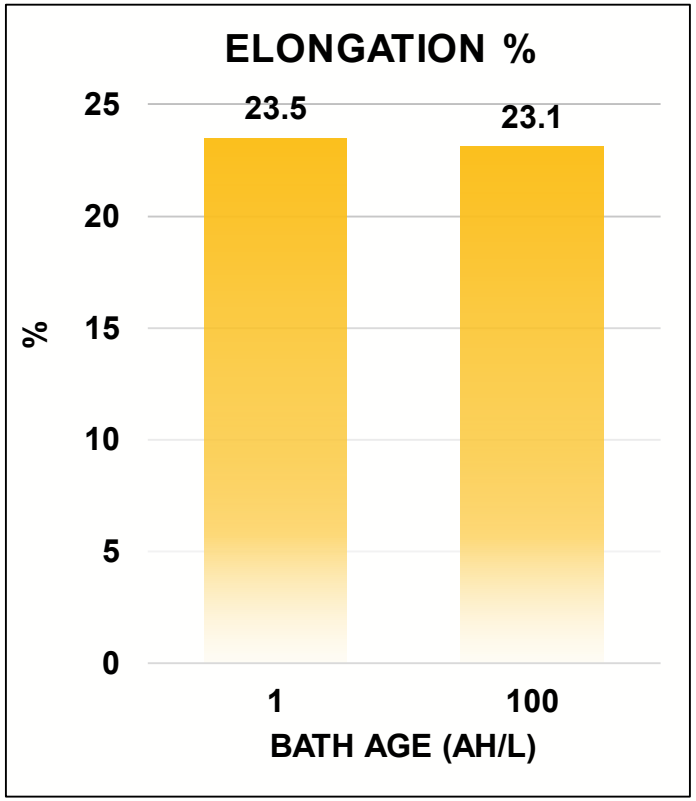
- Low internal stress both as plated and annealed 130 °C for 1h
- Stable with aged bath



Physical Properties, T&E

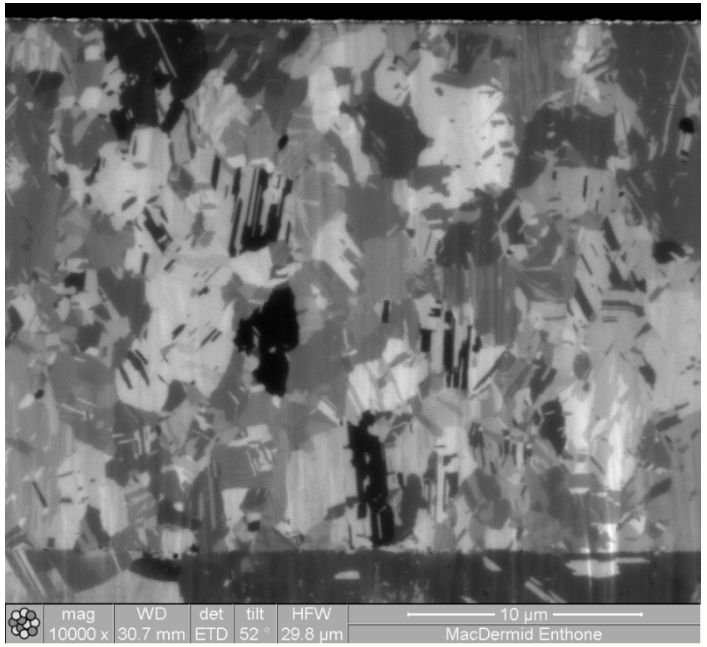
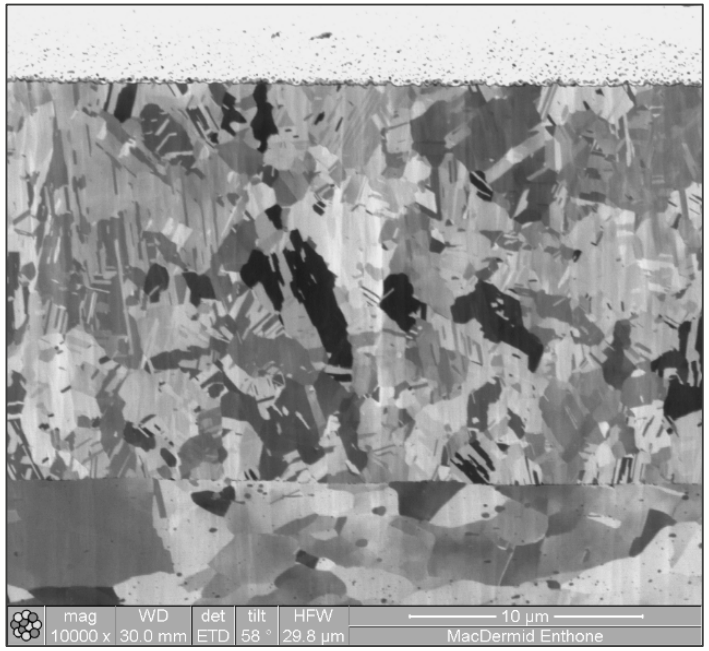
- Passed the IPC class III criteria, tensile strength greater than 36,000 psi and elongation greater than 18%
- Stable with aged bath





Copper Grain Structure

- Consistent grain structure with different aged bath
- Small size, equiaxial grain structure

New bath	100 Ah/L
	

Conclusion

- Two acid copper plating processes were introduced on embedded fine line and 2-in-1 RDL plating with panel level approach
- Systek ETS acid copper plating process offers excellent uniformity, within-unit and within-panel
- Fine line down to 7 µm can be achieved on the panel level in high volume production with VCP plater
- Systek ETS acid copper plating process can also be used for 2-in-1 RDL plating when the electrolyte contains low concentration of sulfuric acid
- Systek UVF 2-in-1 RDL plating process offers great trace profile, excellent via fill capability
- Plated height variation, WID%, is below 5% with fine line down to 15 µm
- The copper deposits had low internal stress. Tensile strength and elongation passed IPC class III criteria

Booth #33/34