PCB Embedding Technology for 5G mmWave Applications

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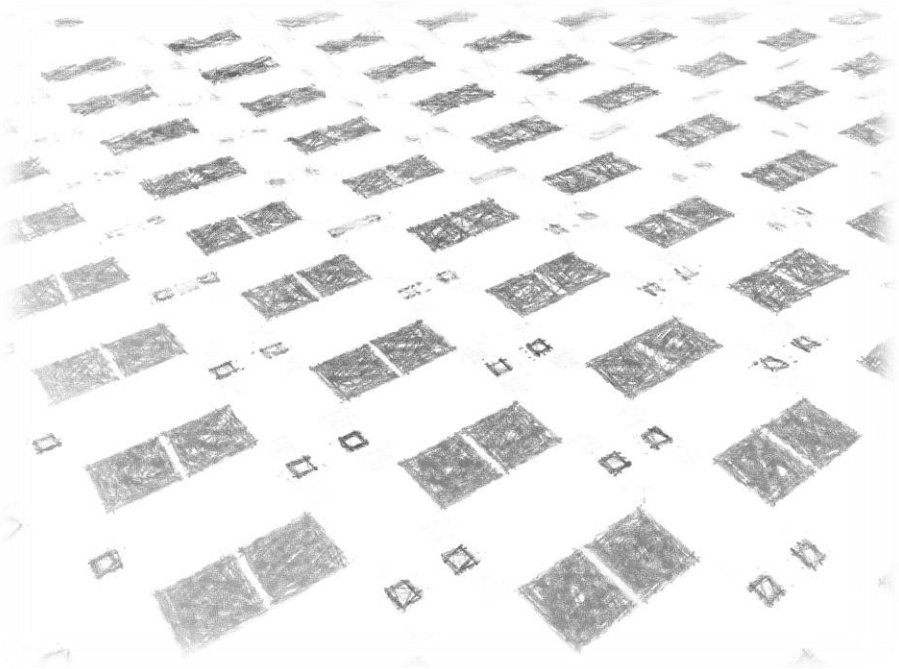
Outline



- Introduction
  - Motivation
  - Challenges
- Embedding Process
  - Concepts
  - Process
- Module / Antenna Development
  - Dielectric Material characterization
  - Design Validation
- Conclusion

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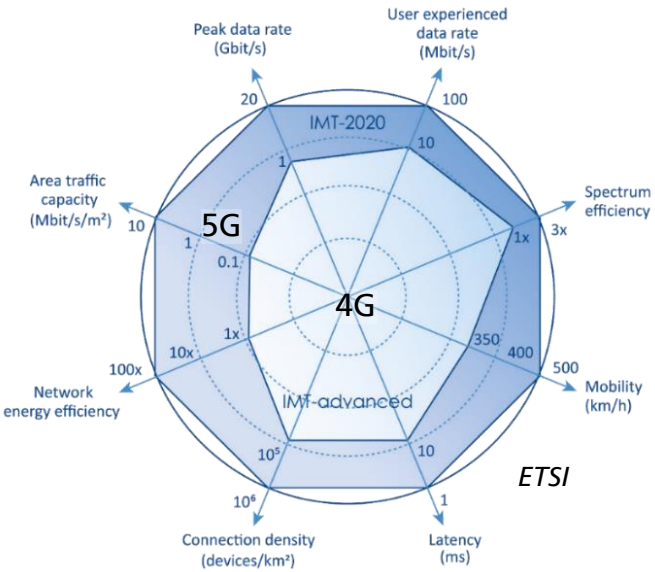
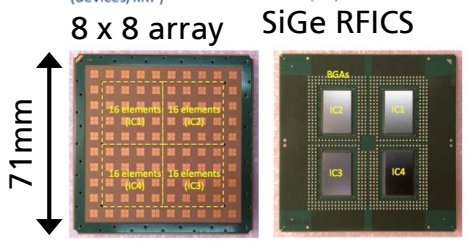
Motivation - Embedding for RF Applications

5G Millimeter Wave Front-Ends Goals + State of the Art

- 5G wireless networks will offer improved performance
- Technical challenges
  - Large number of connections, high data rate
  - Usage of millimeter wave frequencies
  - Antenna arrays with narrow steerable beam
  - RF path loss from transmitter to receiver
  - Modular approach for systems improves yield





X. Gu: A Multilayer Organic Package with 64 Dual-Polarized Antennas for 28GHz 5G Communication, IBM Research

ERICSSON infineon EPIGAN OMMIC innovating with III-V'S FOI CHALMERS Technische Universität Berlin Fraunhofer IZM

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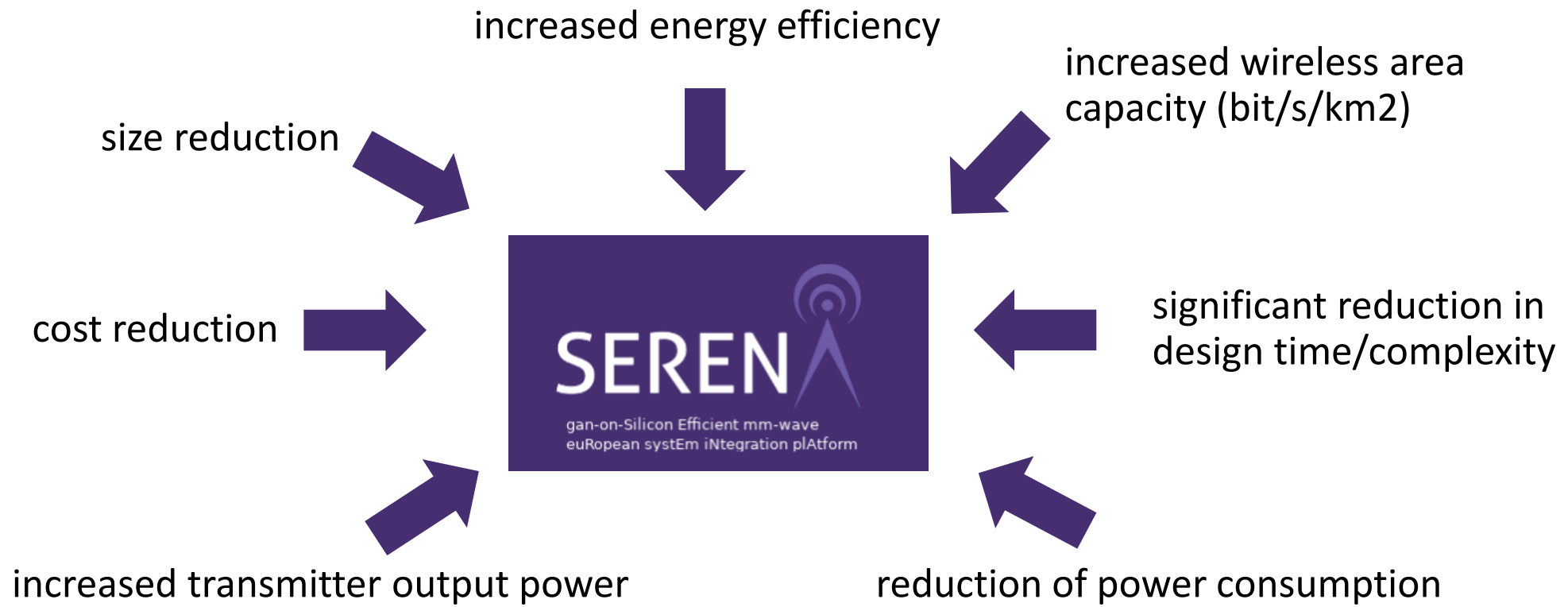
Motivation - Embedding for RF Applications



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Challenges – Embedding Technology SERENA

- Long experience in embedding at Fraunhofer Projects (since 1999)
- More than 7 European funded projects
- More than 40 projects with industry partners and technology transfers

HOWEVER

- In SERENA challenging types of chips and preconditioning
- Non-standard embedding materials requested
- Therefore no standard technology applicable
- Substantial technology developments necessary in SERENA

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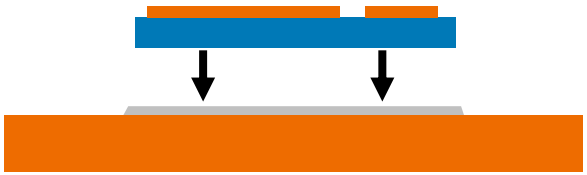
Embedding - Process



chip attach
(chips with top side Cu bumps)

embedding into prepreg layers by **vacuum lamination**

via drilling of chip top side contacts
(+ micro vias / through vias)

Cu plating and structuring

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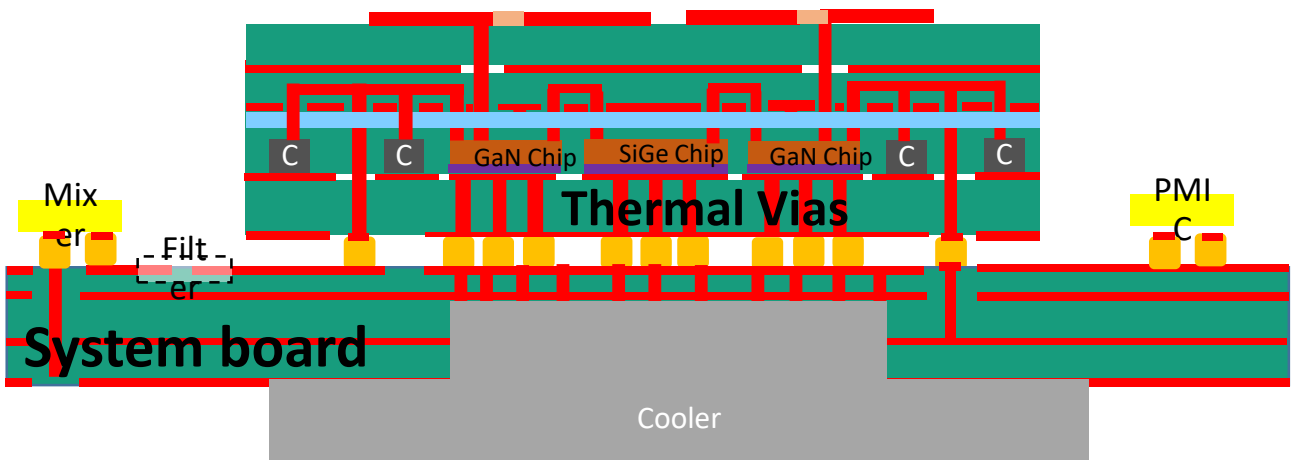
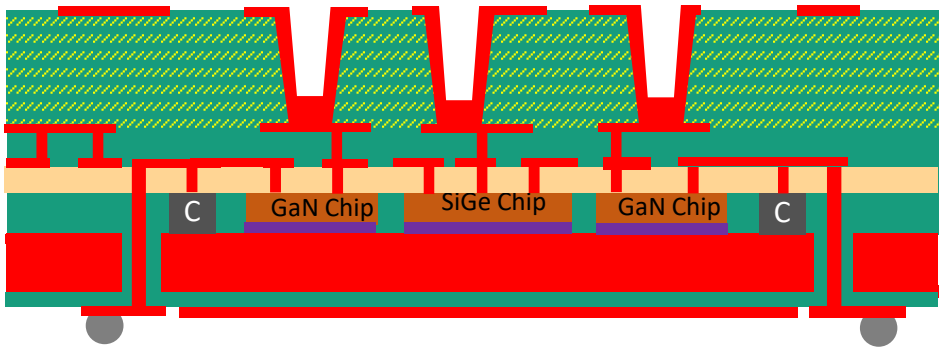
Embedding for RF Applications - Tasks

specification	Standard embedding	SERENA
Contact pad metallization	Copper	Gold
Metallization thickness	Minimum 10µm	3µm
dimension of contact pad	150µm	100µm
Power dissipation	0,8Watt/mm² power electronics	1,5 Watt/mm²
Embedding Material	High TG PCB Material	High frequency material



Embedding for RF Applications - Concepts

Concept 1: thick Copper layer



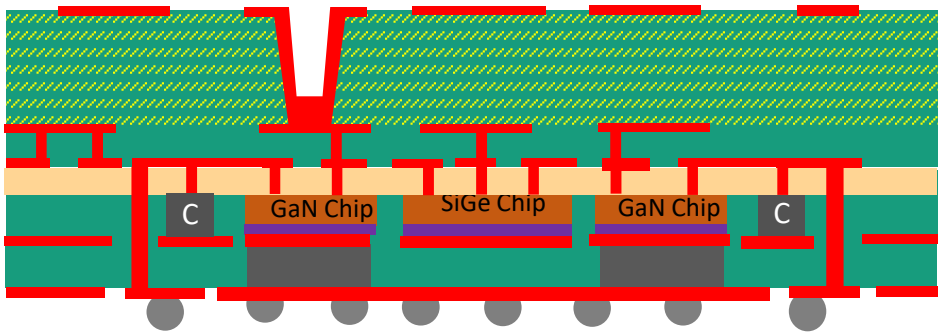
Advantages

- High thermal conductance

Risks

- Thin Chip metallization
- Complicated process to produce thermal Core and coaxial vias

Concept 2: thermal Bridges with sintering



Advantages

- Very high thermal conductance

Risks

- Thin Chip metallization
- Complicated process to produce thermal Core

Antenna layer | HF Material | ABF 10µm | Ag sintering paste

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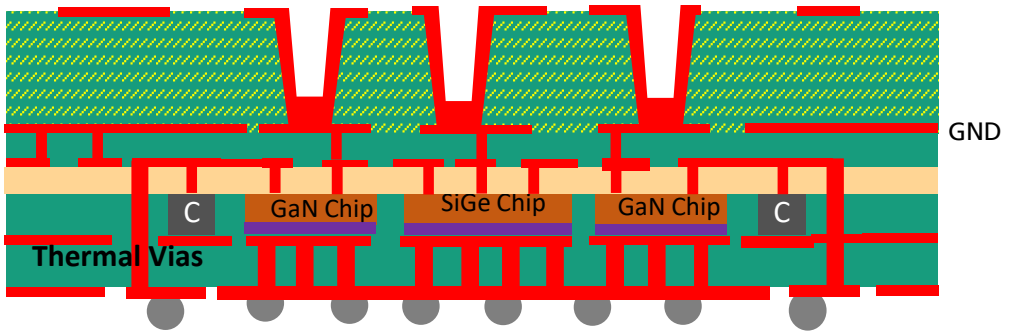
Embedding for RF Applications - Concepts

Concept 3: thermal Via



Advantages

- Thermal Core easy to produce

Risks

- Thin Chip metallization

Antenna layer HF Material ABF 10µm

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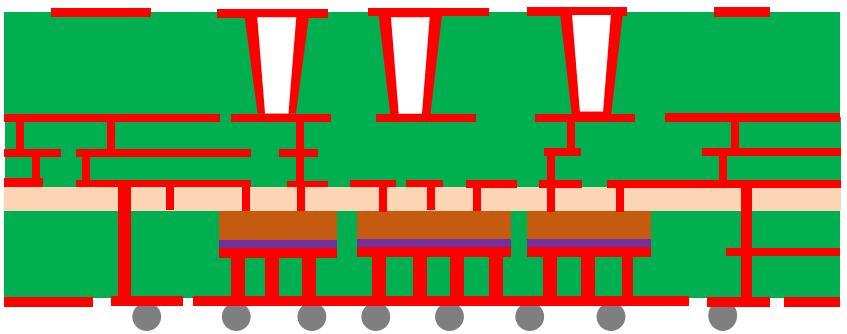
Embedding for RF Applications - Tasks

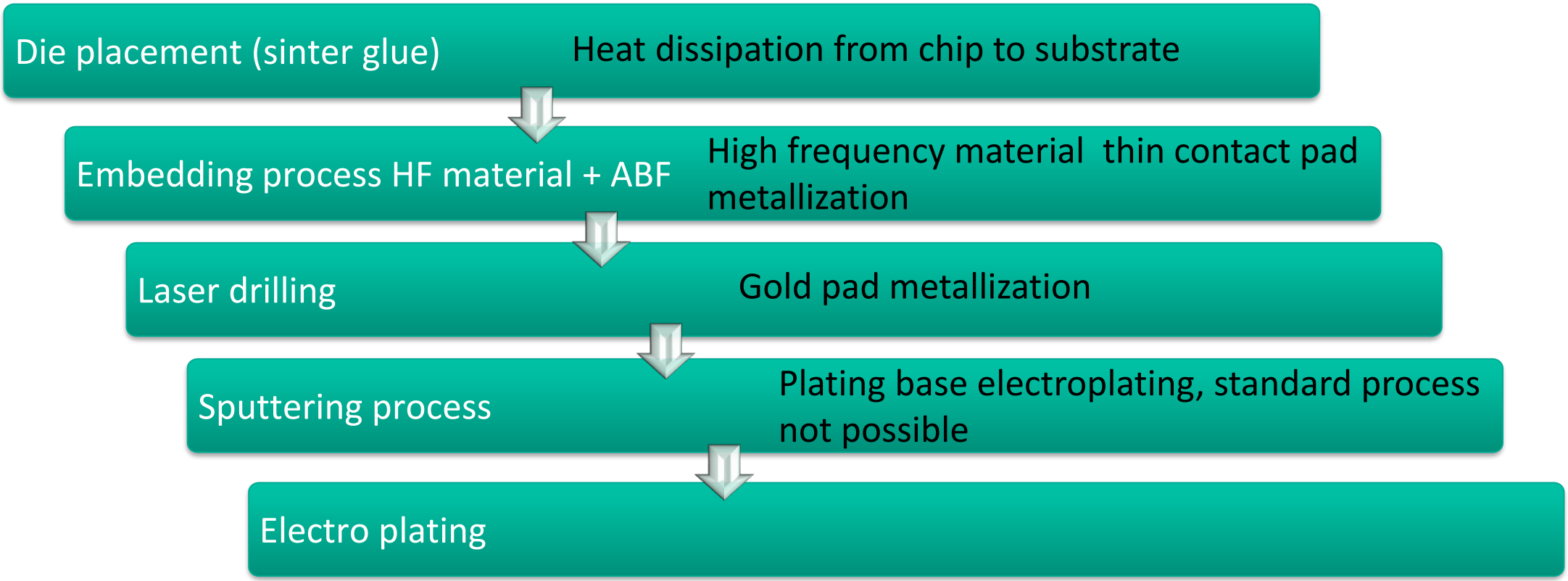
SERENA Approach: PCB Embedding for Millimeter Wave Front-End Modules

- Goal: Minimize TX-RX path loss at mmWave
- Antenna-in-package integration: PCB-embedding of RFICs directly below antennas
- RF low loss laminates
- High integration density
  - Antenna beam former IC (beam steering)
  - RF power amplifer ICs
  - Decoupling capacitors



German Patent Application 1020172001275

Development Embedding Process - SERENA



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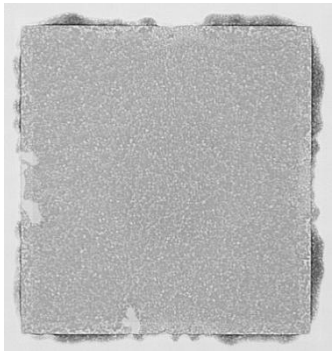
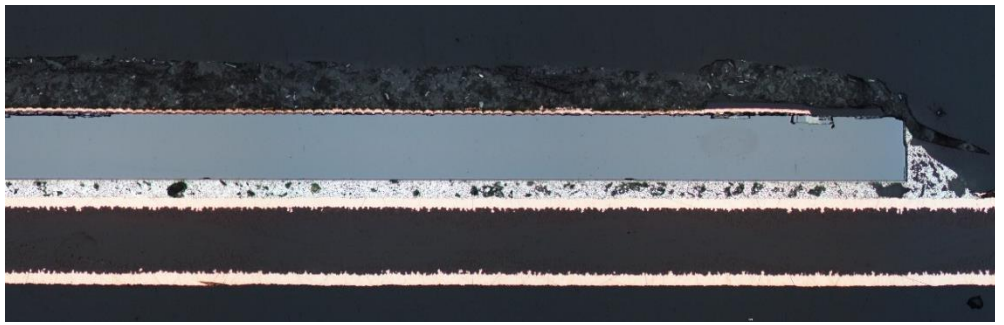
Development Embedding Process - SERENA

Setup sinter glue

Die placement (sinter glue)

- New advanced sinter glue (Namics)
- Processability tested and approved at IZM
- shear test and x-ray inspection passed





Parameter		Unit	Note / Condition
PASTE PROPERTIES (before curing)			
Viscosity	60	Pa·s	Viscometer type EHD 3°Cone R9.7 (25°C) @5rpm
Thixotropic index	7.0	--	0.5 rpm / 5 rpm
Non-volatiles content	94	%	
Silver content	89	%	Calculated
Density	4.7	g/cc	Calculated
CURED PROPERTIES (60 min. ramp to 200°C, and 60 min. hold at 200°C)			
Volume resistivity	8	µΩcm	LCR Meter
Die Shear strength RT	45	N/mm²	Si chip (2x2mm, backside Au)/ Ag plated CuLF
Die Shear strength @260°C	25	N/mm²	Si chip (2x2mm, backside Au)/ Ag plated CuLF
Coefficient of Thermal Expansion (CTE)	23	ppm/°C	TMA
Water Absorption	< 0.1	%	After 96 hours at 85°C 85% RH exposure
Storage Modulus RT	17	GPa	DMA
Storage Modulus 200°C	8.0	GPa	DMA
Impurities concentration Na	< 5	ppm	NATS
Impurities concentration K	< 5	ppm	NATS
Impurities concentration Cl^-	< 35	ppm	NATS
Thermal conductivity 1 layer	140	W/mK	Laser Flash, 0.7 mm thickness
Thermal conductivity 3 layer	120	W/mK	Laser Flash, 35 µm BLT
Thermal Resistance	0.3	K/W	JEDEC JESD51-1 static test method (T3Ster, 3x3mm Si chip (backside: Au)/Ag plated Al_2O_3
SYRINGE PROPERTIES			
Pot Life	2	days	25% increase in viscosity @ 5rpm @ 25°C

Development Embedding Process - SERENA

Embedding

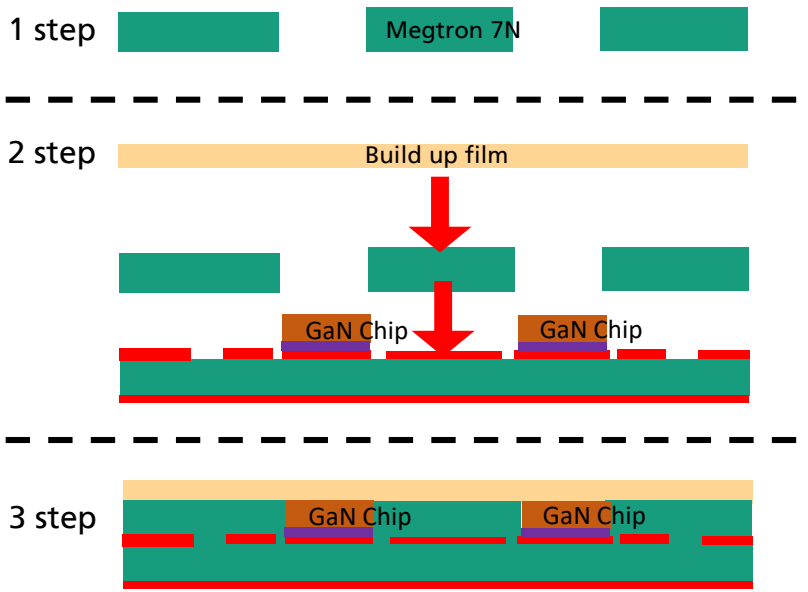
Embedding process HF material + ABF

- Development of a new embedding lamination process to combine PCB-material together with a build up film:

1st step: laser cut chip cavity (HF material Prepreg)

2nd step: pre-lamination of the layer stack in a vacuum applicator

3rd step: conventional PCB-lamination process



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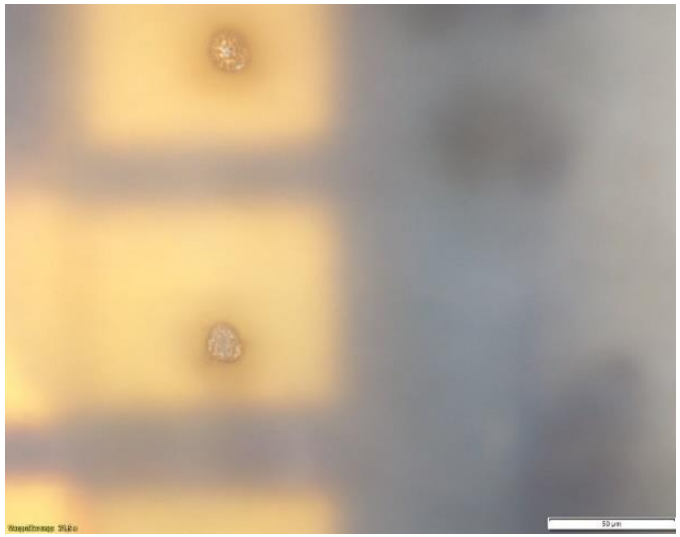
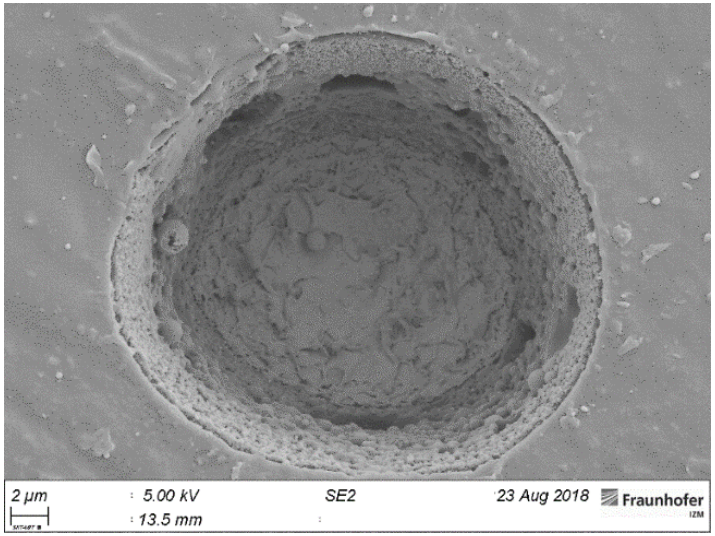
Development Embedding Process - SERENA

Via formation

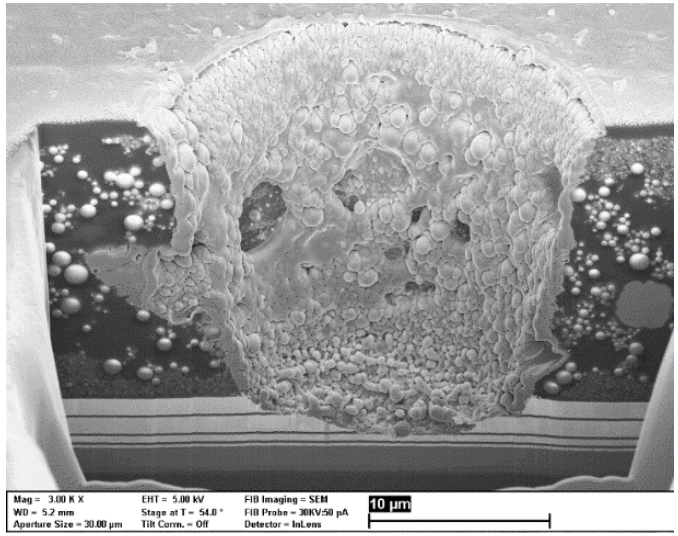
Laser drilling



Laser via microscope



Laser via SEM



Laser via FIB cut

- Challenging laser setup, due to thin Au-metal layer.
- Explorative study to find appropriate laser parameters.
- SEM and FIB cut to analyze intermediate results

  → It is possible to stop on 3µm Au pad

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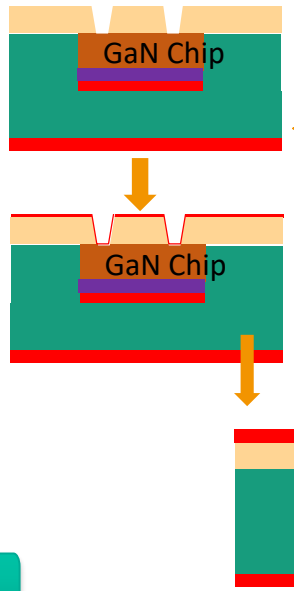
Development Embedding Process - SERENA

- Die placement (sinter glue)
- Embedding process HF material + ABF
- Laser drilling
- Sputtering process
- Electro plating



sputtering process (plating base): 100nm TiW / 300nm Cu

important: degassing of substrate prior to sputter process in order to ensure better Cu adhesion

electro plating:
electro plating bath leveling characteristic (“via filling”)

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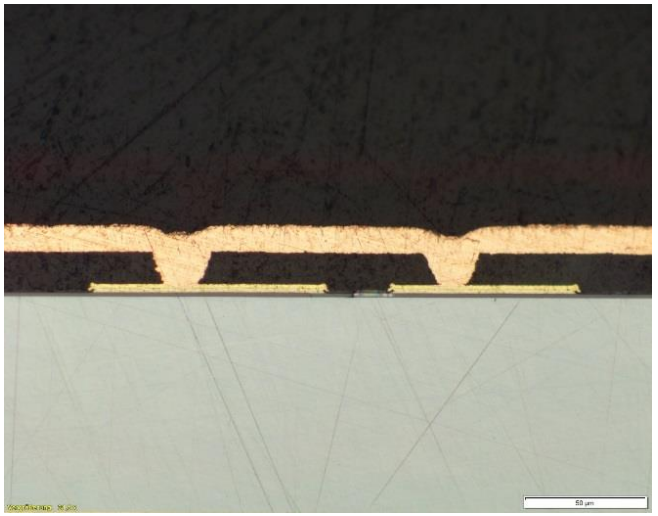
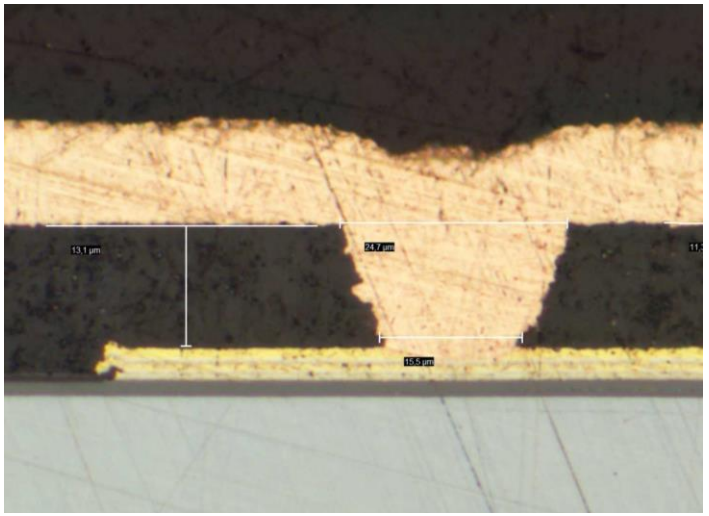
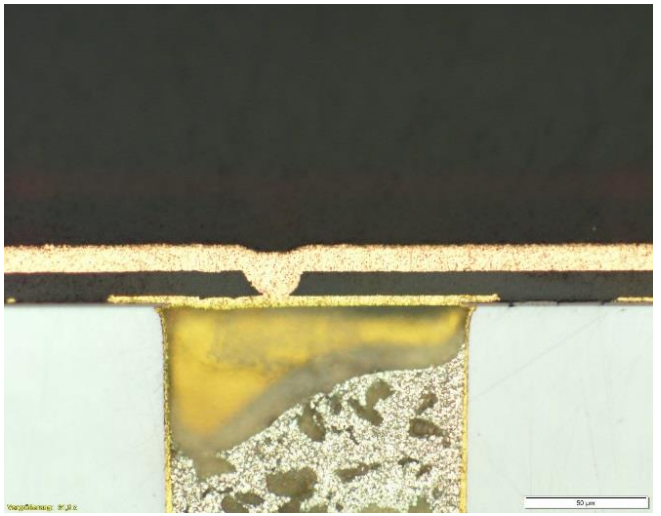
Development Embedding Process - SERENA

Embedding Process: Sputtering + electroplating







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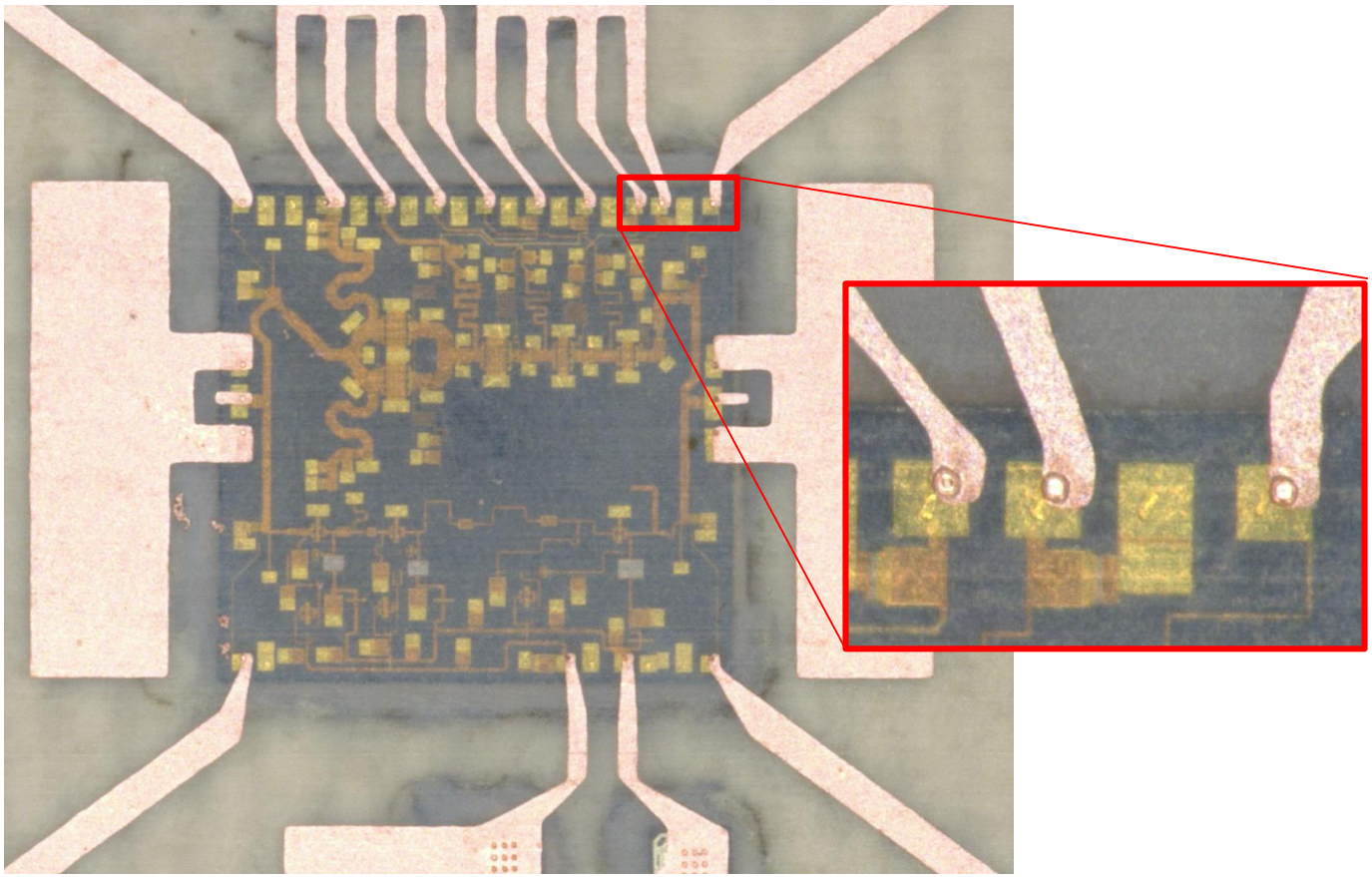
Development Embedding Process - SERENA

Embedding Process: RDL



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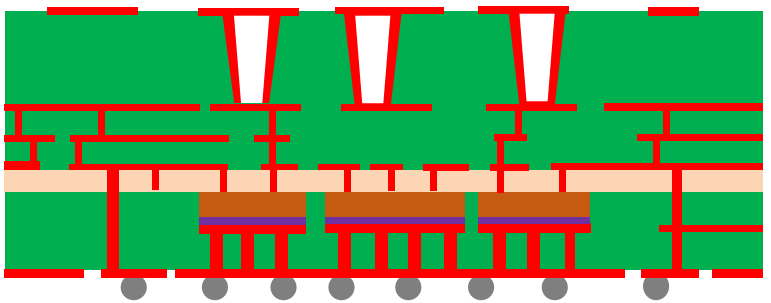
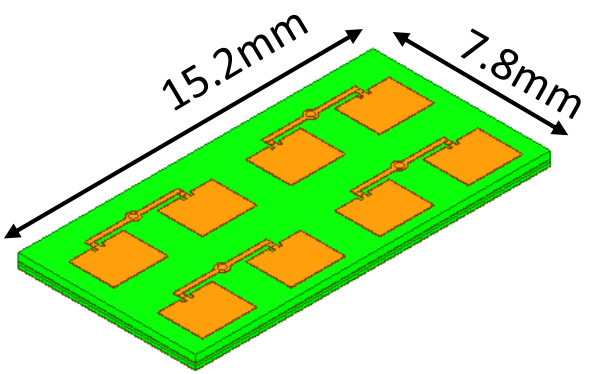
PCB Embedding for Millimeter Wave Front-End Modules

- Goal
  - Minimize TX-RX path loss at mmWave
  - Antenna-in-package integration: PCB-embedding of RFICs below antennas
- Usage of low loss RF laminates
- Stack-up
  - Antenna layers: thick RF laminates (low DK, low DF) for antenna performance
  - Routing layers : Controlled impedance for mmWave low loss interconnects



German Patent Application 1020172001275



Module cross section and integrated antenna array

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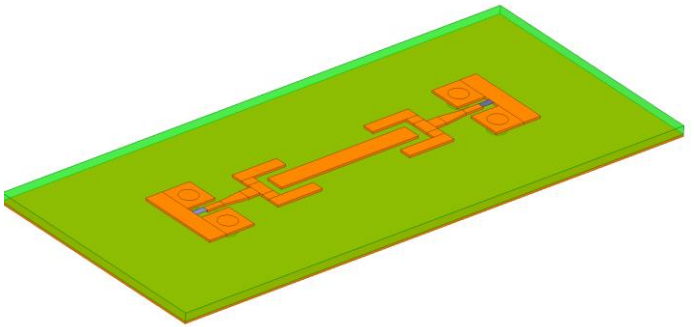
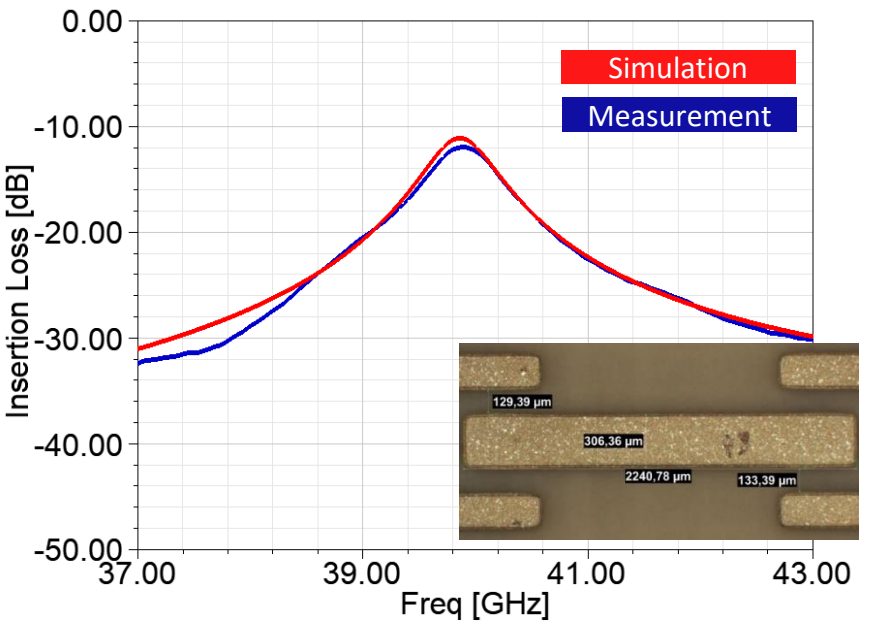
Dielectric Material Characterization

- Integration of antennas requires knowledge of frequency dependency of dielectric material properties DK, DF at application frequency
- Planar resonators as test and monitoring structures for process values of DK, DF
- Requires rigorous modeling of resonator insertion loss including loss mechanisms and geometry with numerical field simulations





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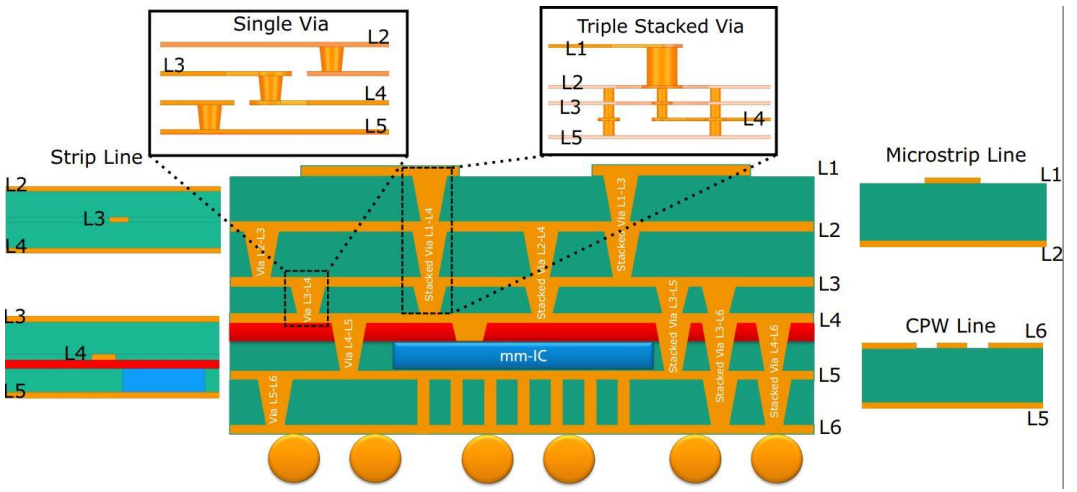
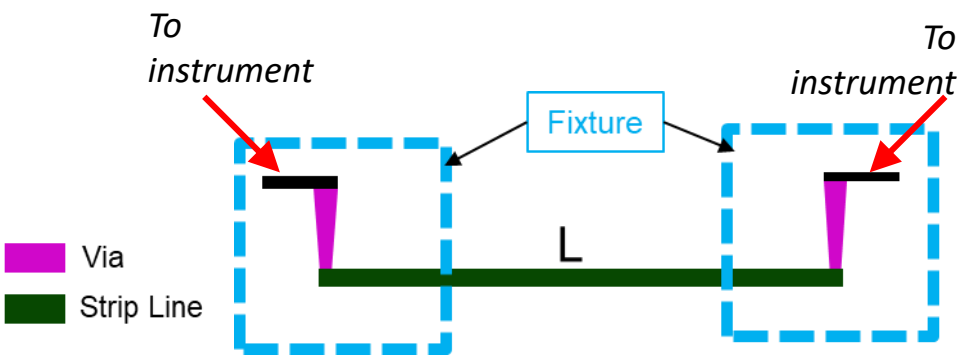
Validation Methodology

- Complex interconnect signal paths are divided into elements for electrical modelling
- Model validation by test structures containing fixtures for contact to measurement equipment





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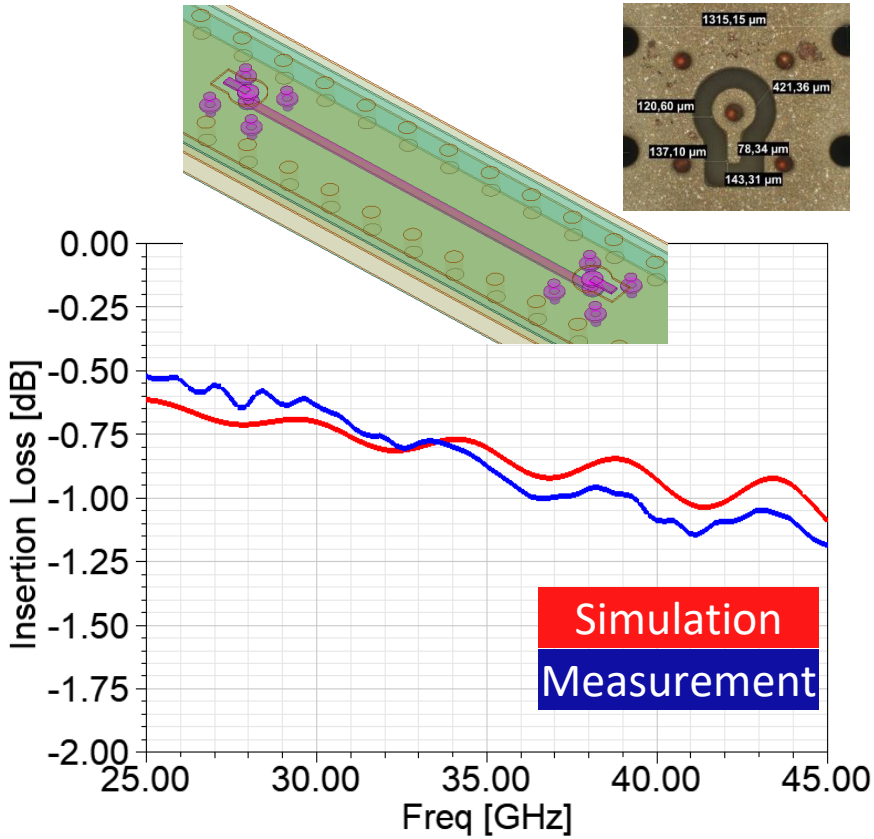
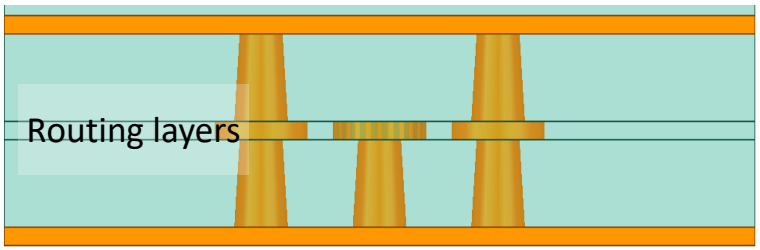
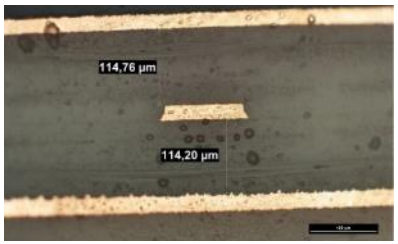
Interconnects

- Optimization of interconnect geometry for RF performance
- Good match between electrical model and measurement
- Good RF performance at application frequency
  (<1dB insertion loss,
  > 23dB return loss)



RF signal path test structure including Pad, via, strip line, via, contact pad





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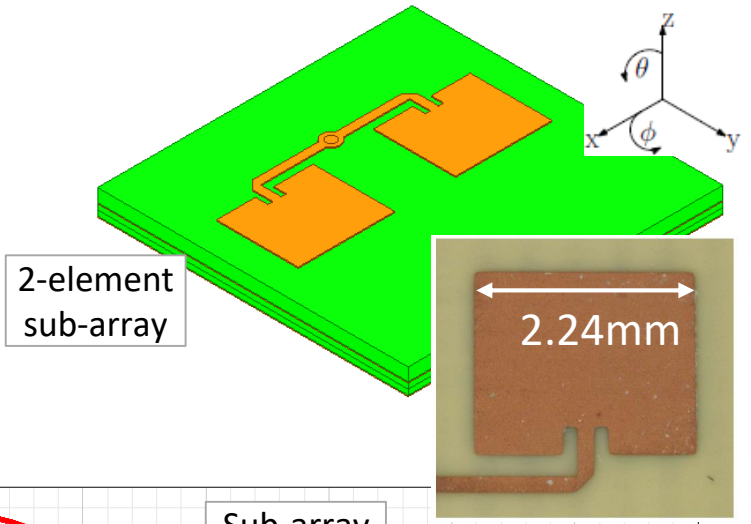
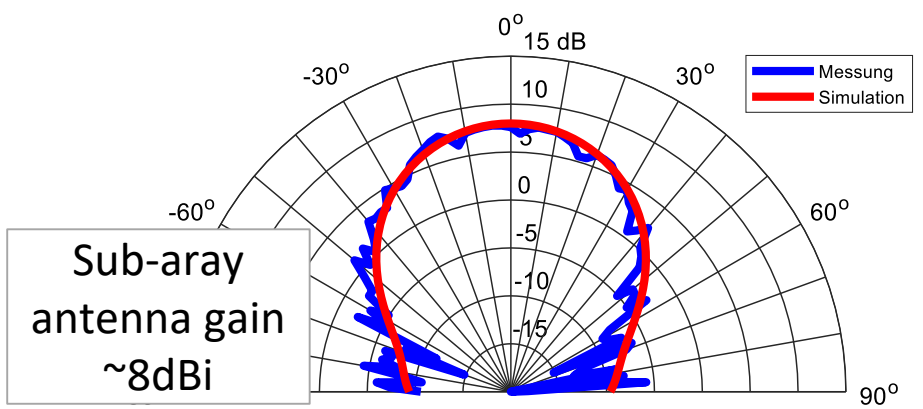
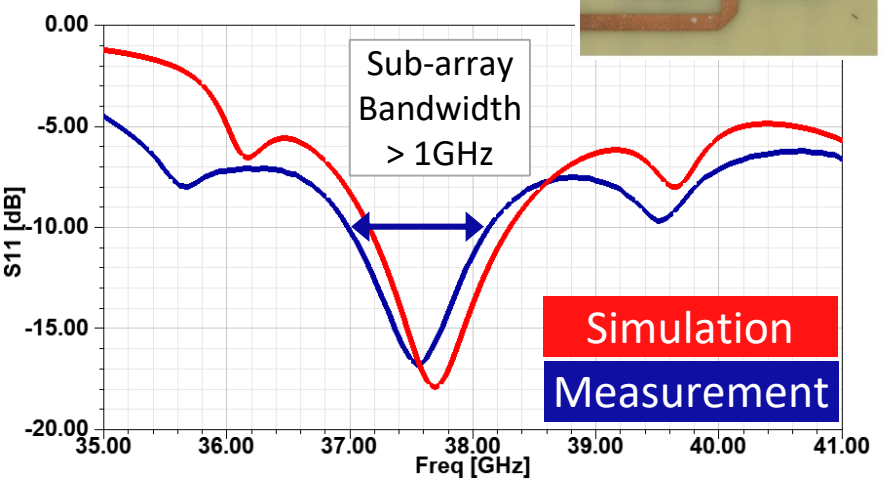
Performance of 1 x 2 Antenna-in-Package Array

- Antenna pitch for optimum performance $\sim\lambda/2$ dictates module geometry
- Good match of electrical model to mesurement
- Sufficient bandwidth > 1 GHz
- Narrow beam with ~8dBi gain





Sub-aray antenna gain ~8dBi



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Conclusion

- PCB embedding technology was developed for 5G communication applications
- The RF characteristics of package integrated antennas and RF interconnects were investigated using test structures
- The characterization of the test structures show good RF performance in terms of antenna radiation characteristics and interconnect performance.
- The developed embedding technology is suited for realization of integrated 5G communication modules including RFICs and antenna arrays.

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Thank you very much for your attention!

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