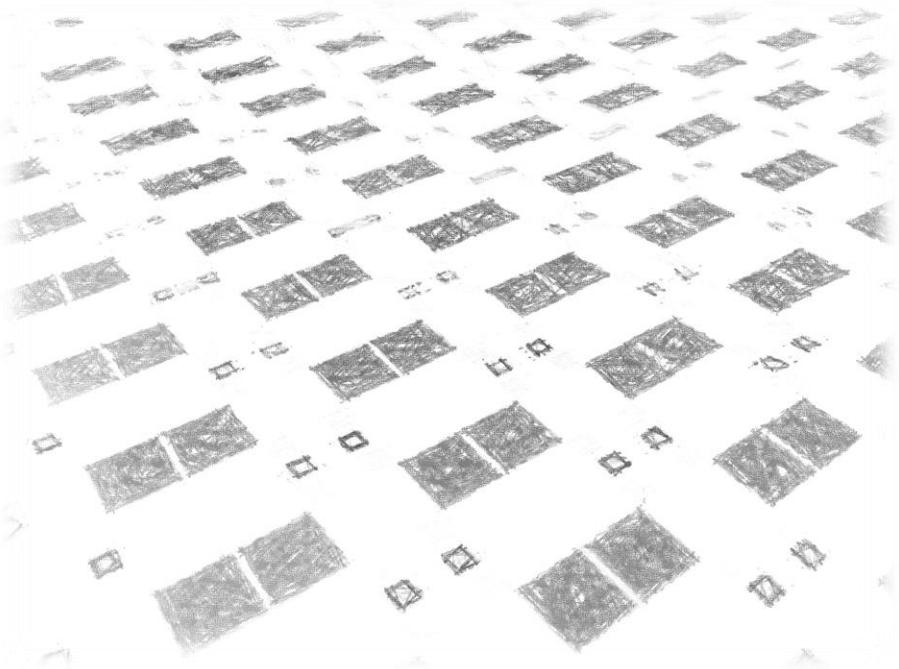
Adaptive High Density RDL Technologies for Panel Level Packaging

- Lars Böttcher
- Fraunhofer IZM Berlin
- lars.boettcher@izm.fraunhofer.de

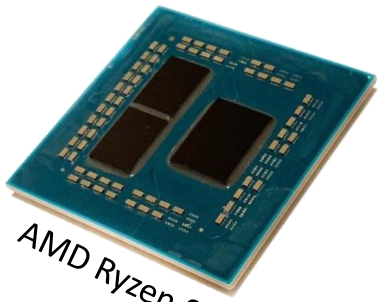
Outline

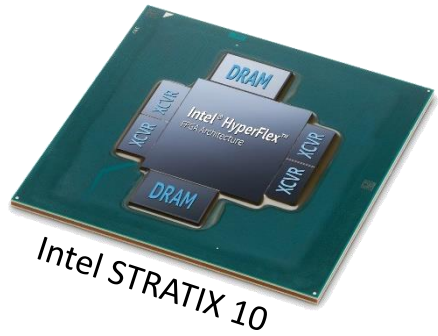


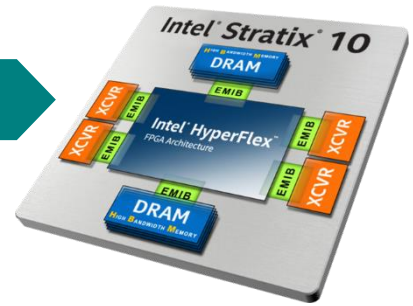
- Introduction
  - Packging Concept
  - PLP Equipment
- Panel Level Process
  - Test Vehicle
  - RDL Process
  - Adaptive processing
- Conclusion
- Acknowledgements

Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

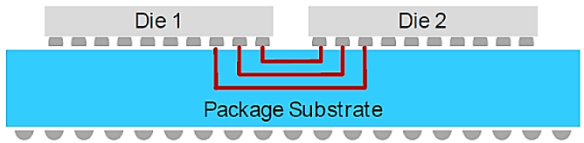
Introduction



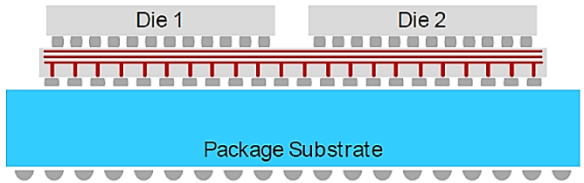




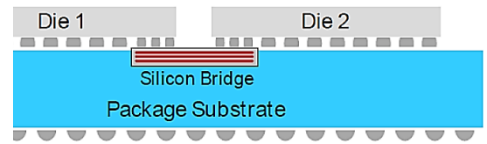
Multi-Chip Package



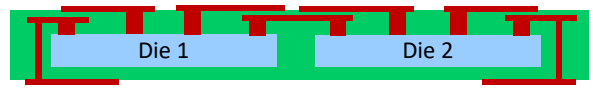
Silicon Interposer



Embedded Multi-Die Interconnect Bridge



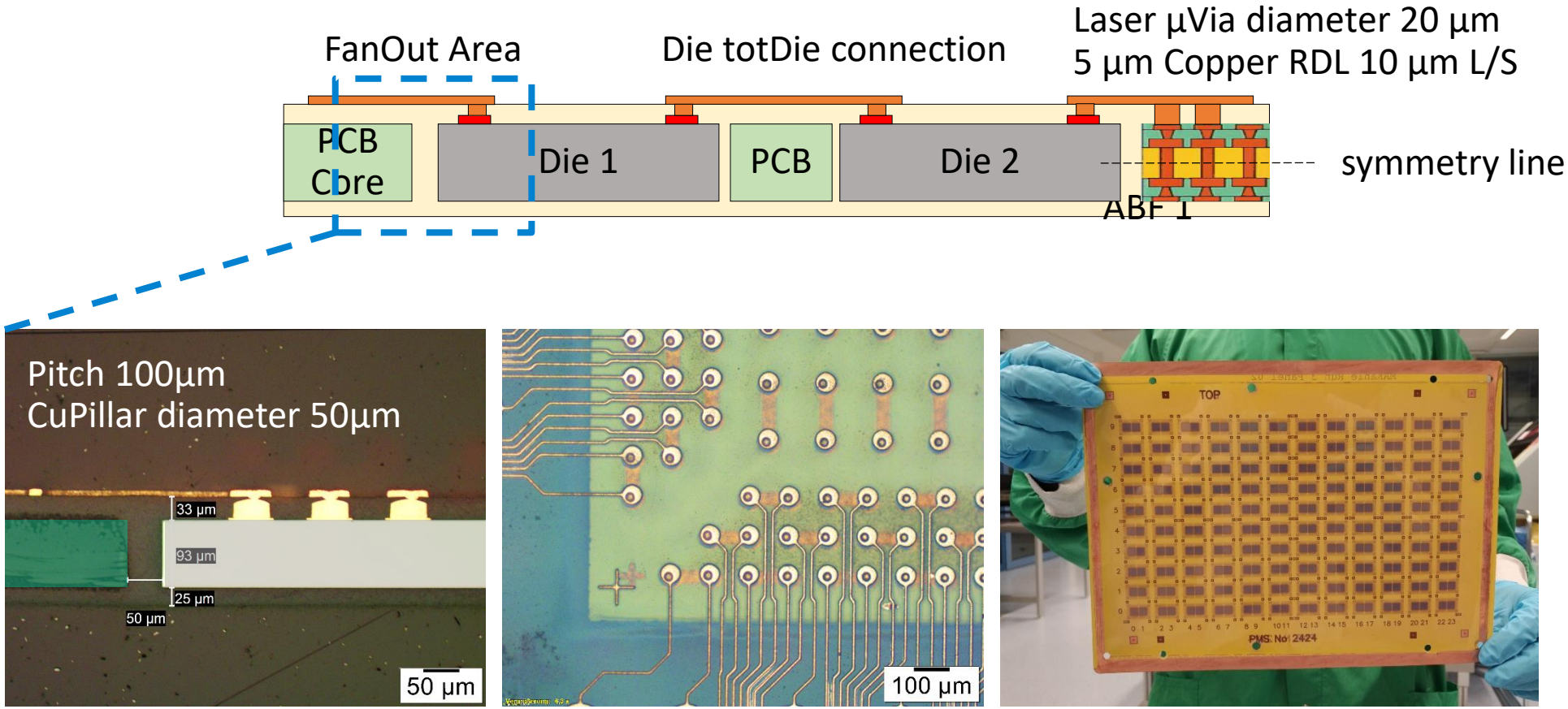
Embedded into substrate



- Low cost processes with organic materials
- Short die to die distance < 100 µm
- Poor yield ↔ high failure-costs

Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

Packaging Concept



Cross section

Top View

Prototype production panel 12“ x 9“

000221

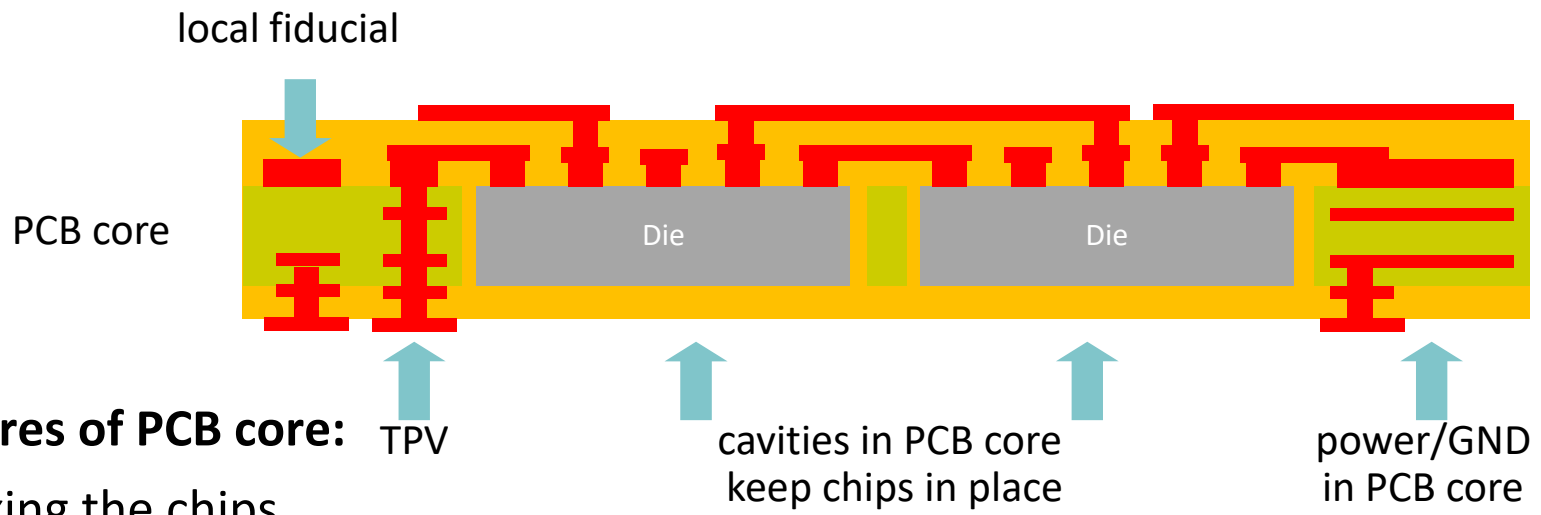
Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

Fraunhofer IZM

PLP Embedding Concept

Process concept

- Use of a laminate (PCB) core for embedding of the dies in order to provide a high handling stability and limitation of die shift
- Through holes can already be provided by the core
- No via to dies → direct connection Cu pillar with RDL line
- Adaptive imaging in order to compensate die shift / placement tolerances



Possible features of PCB core:

- Holes for fixing the chips
- Global and local fiducials for die attach
- Pre-manufactured through-vias
- Pre-manufactured conductors e.g. for power supply

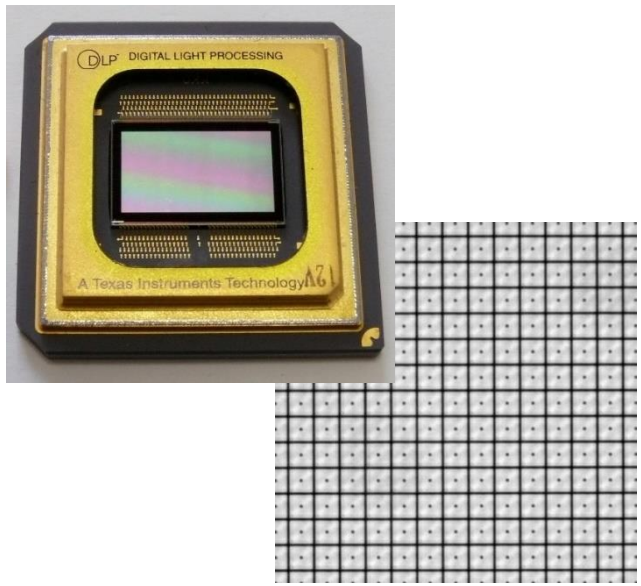
Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

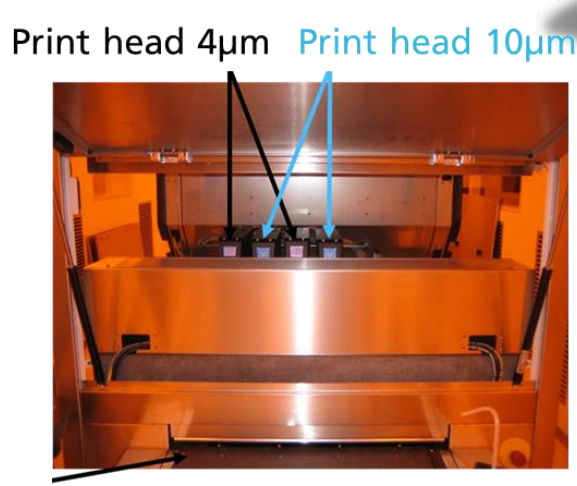
PLP Equipment – Direct Imaging

Micro mirror Digital Imaging (MDI)

- Matrix of micro mirrors (DMD = digital micromirror device)
  - Print heads:
    - 2x 10µm LLS10: 1920 x 1080 , Subpixel size 0,9µm
    - 2x 4µm LLS4: 2560 x 800, Subpixel size 0,36µm
    - 6x 2µm LLS2: 2560 x 800, Subpixel size 0,21µm

Forschungsfabrik Mikroelektronik Deutschland

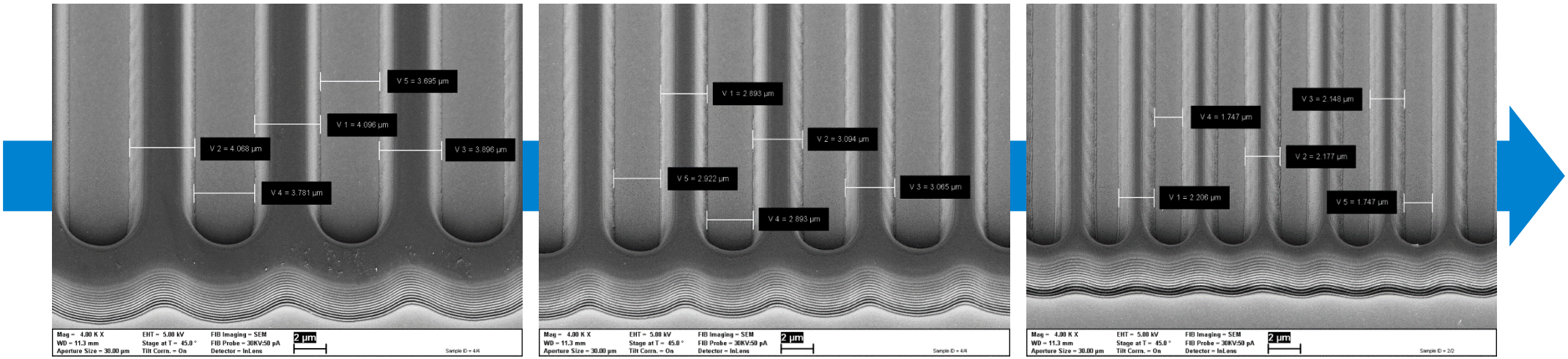




Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

PLP Equipment – Direct Imaging

- Development towards 2µm L/S
  - Most recent results exposure 2µm MDI system
  - Thin positive tone liquid PR, 2µm thickness



4µm L/S | 3µm L/S | 2µm L/S

Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

Fraunhofer IZM

PLP Equipment – Wet processing / RIE

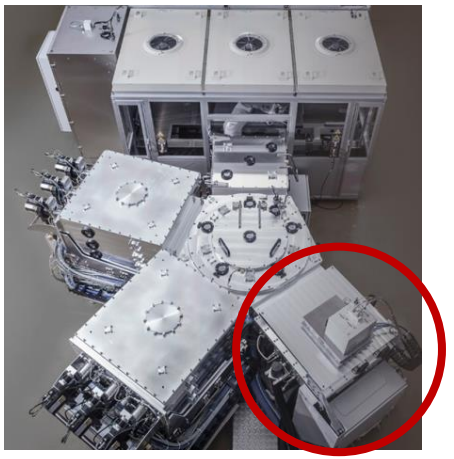
Forschungsfabrik Mikroelektronik Deutschland

Wet processing

- Cu plating tool
- Photoresist development/strip
- Cu plating
- Ti and Cu differential etch

Evatec: Reactive Ion Etching chamber

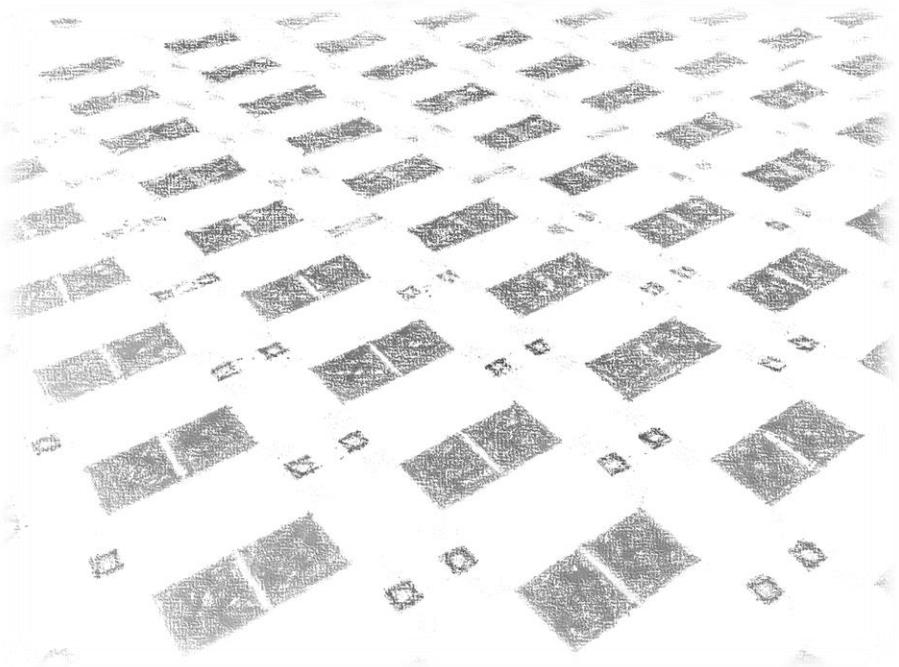
- Resist descum
- Dielectric etch
- Surface activation
- …
- Four gases: N2, Ar, CF4, O2



Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

Fraunhofer IZM

Outline

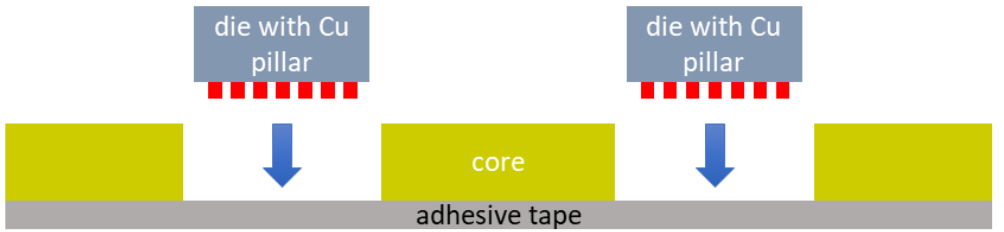


- Introduction
  - Packging Concept
  - PLP Equipment
- Panel Level Process
  - Test Vehicle
  - RDL Process
  - Adaptive processing
- Conclusion
- Acknowledgements

Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

PLP Embedding Process Flow

a) Placement of chips into cavities in PCB core



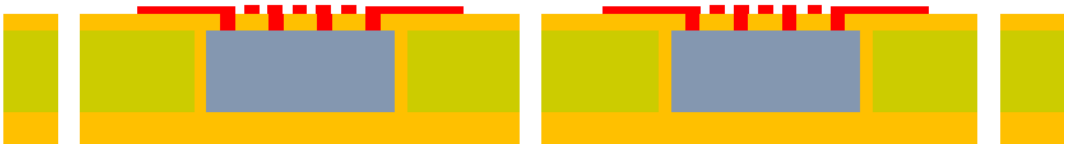
b) vacuum lamination of dielectric film - embedding

c) Removal of adhesive film & 2nd vacuum lamination

d) RIE etching of dielectric

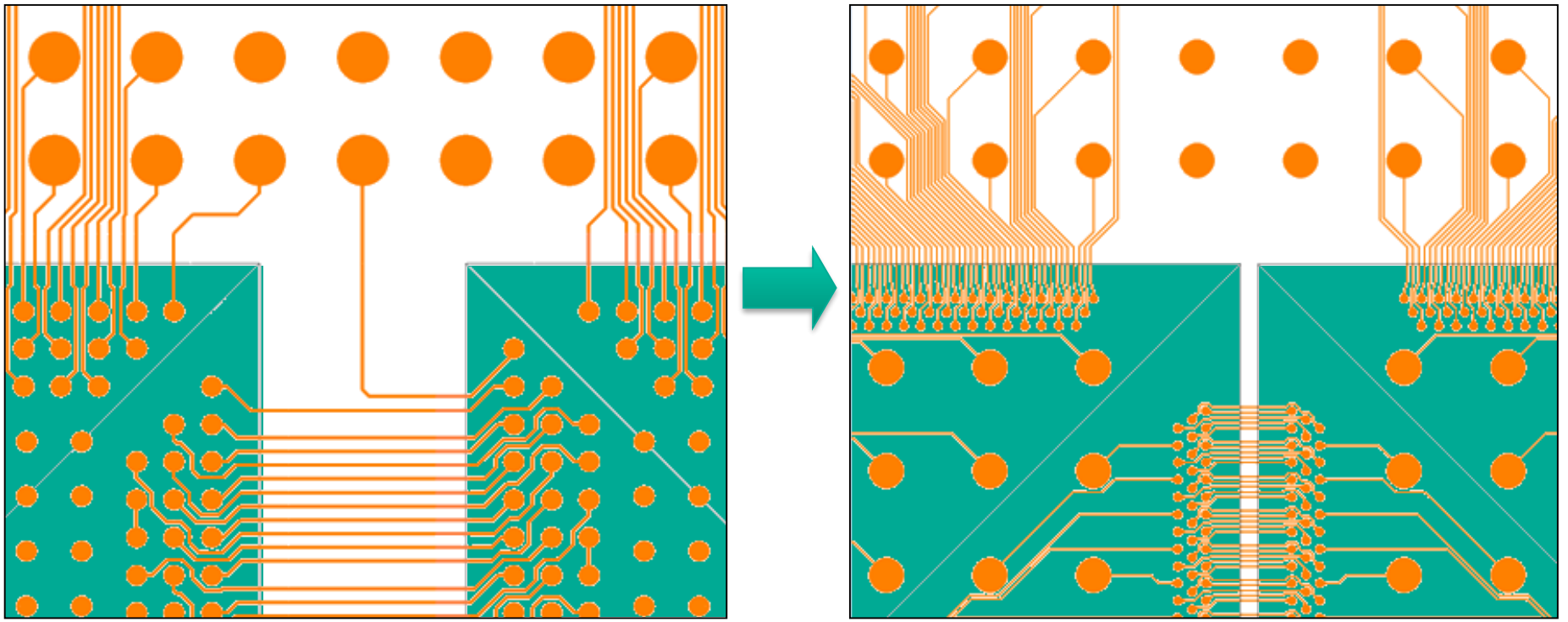
e) RDL formation by SAP Cu plating

f) package separation



Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

Test Vehicle – Chip pitch 100µm → 50µm

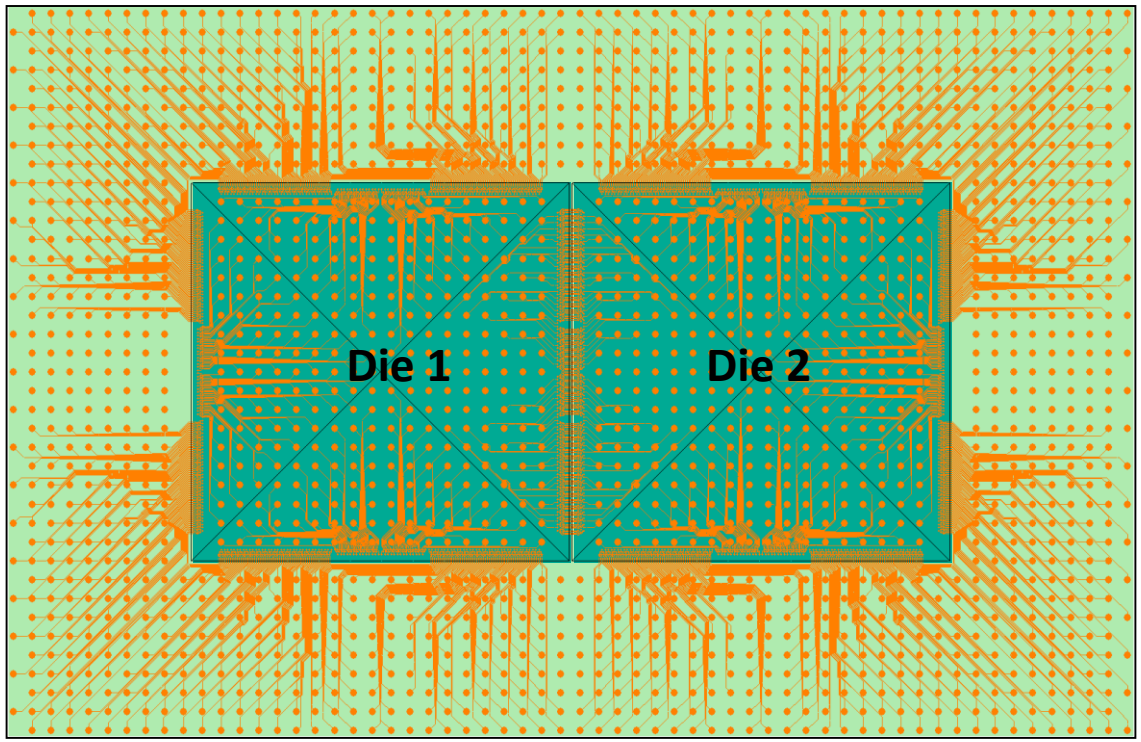


- peripheral pads in 3 rows
- 100 µm pitch / 50 µm pad size
- 10 µm RDL line width
- 550 µm die-to-die gap

- peripheral pads in 3 rows
- 50 µm pitch / 25 µm pad size
- 5 µm RDL line width
- 50 µm die-to-die gap

Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

Test Vehicle – Package Layout



- Two Chips per package
- Chip size 6x6 mm²
- Gap between PCB frame and chips 50 µm
- Gap between chips 50 µm
- Thickness of chips and PCB frame 100 µm
- package thickness 120 µm with one RDL

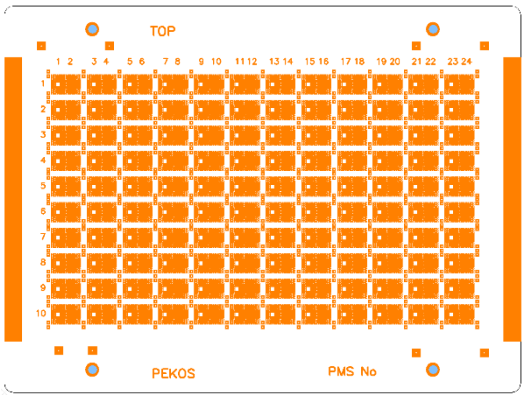
Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

Fraunhofer IZM

Test Vehicle – Panel Layout

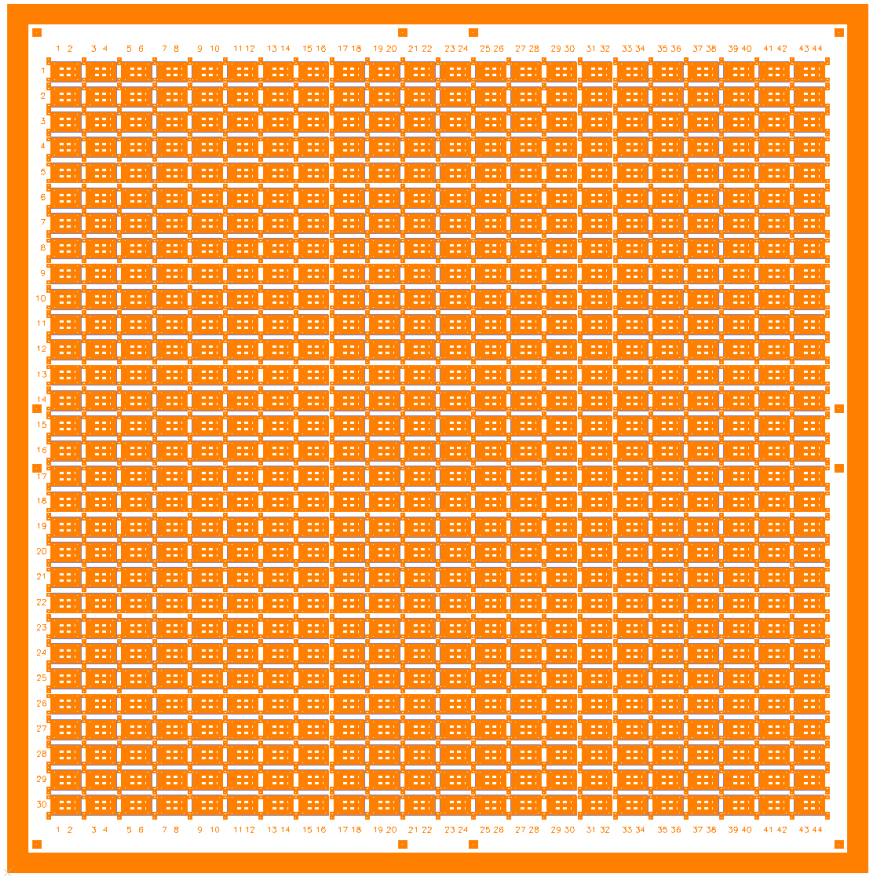
Panel for single process tests

- size 305 x 228 mm²
- 120 modules per panel (240 chips)



Panel for process development

- size 510 x 515 mm²
- 660 modules per panel (1320 chips)

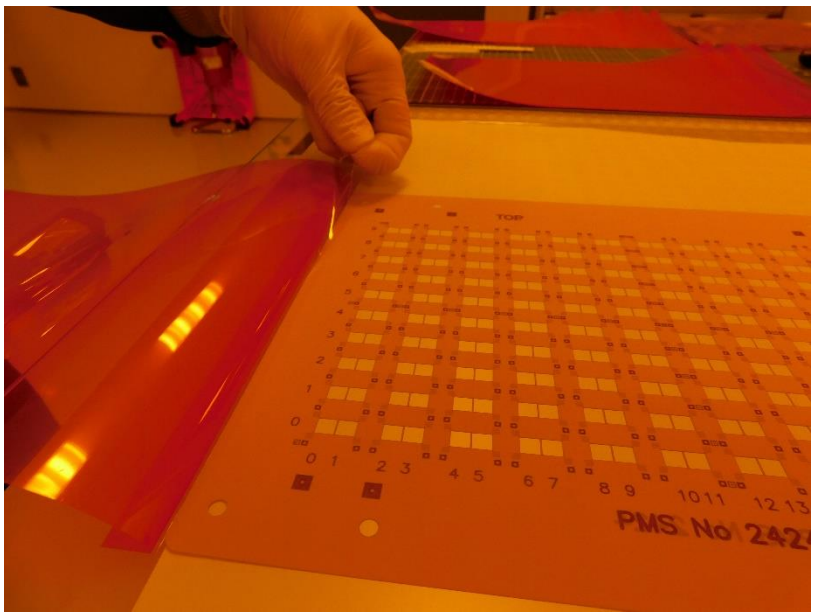


Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

PLP Embedding – Core

Core preparation

- Thin 100µm core material
- Low CTE at 4 – 6ppm/K and high Tg of >260°C
- High precession laser cut cavities for dies
- Lamination of core to adhesive film – no carrier is required

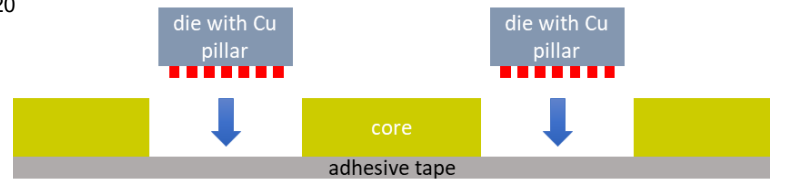


PCB Core with openings

Layup for adhesive tape lamination

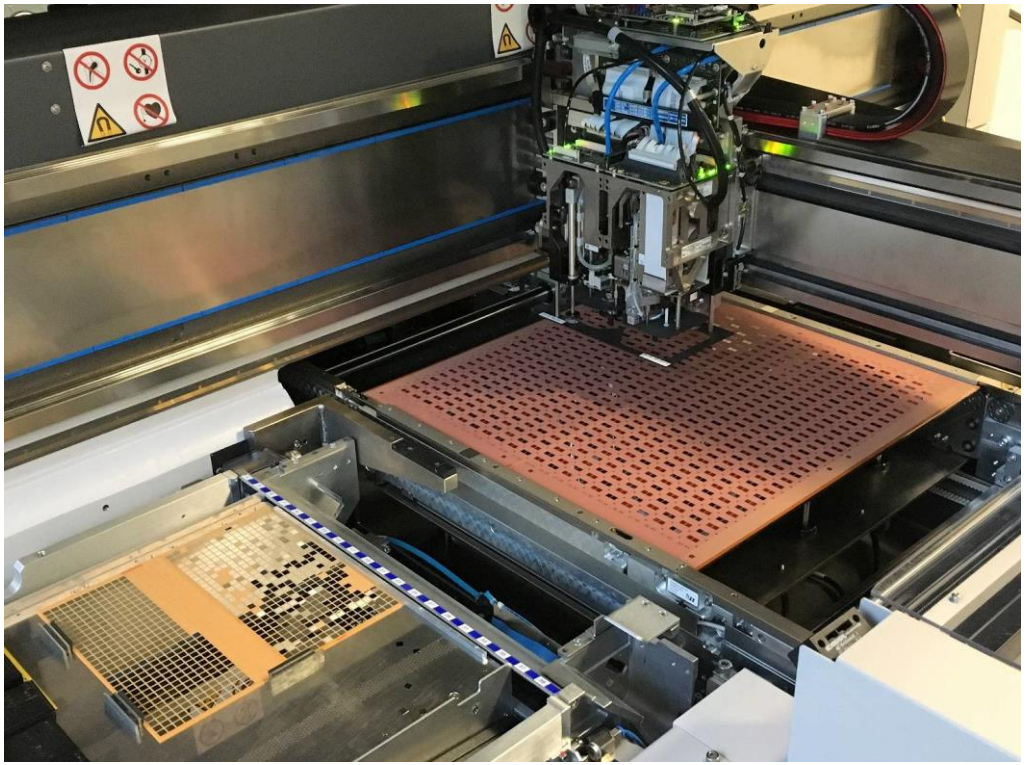
Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

PLP Embedding - Assembly



Die Placement

- Face down die placement into the opening of the core thin 100µm core material
- Core provides narrow gap (20µm around dies) to limit possible die shift

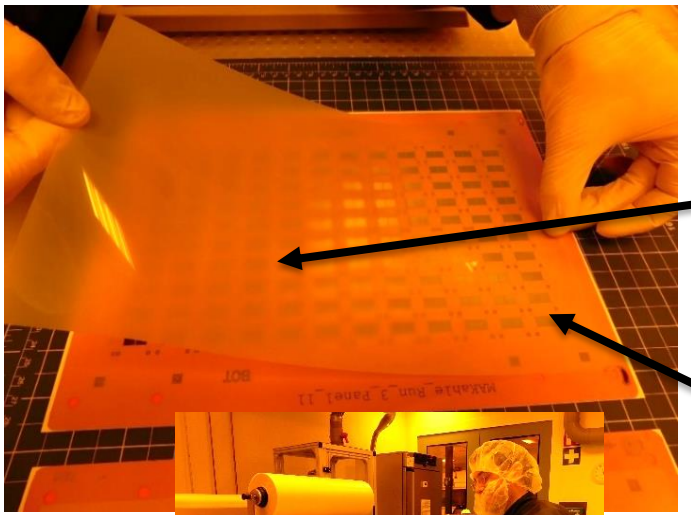


Face down assembly in PCB core

Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

PLP Embedding – Dielectric lamination

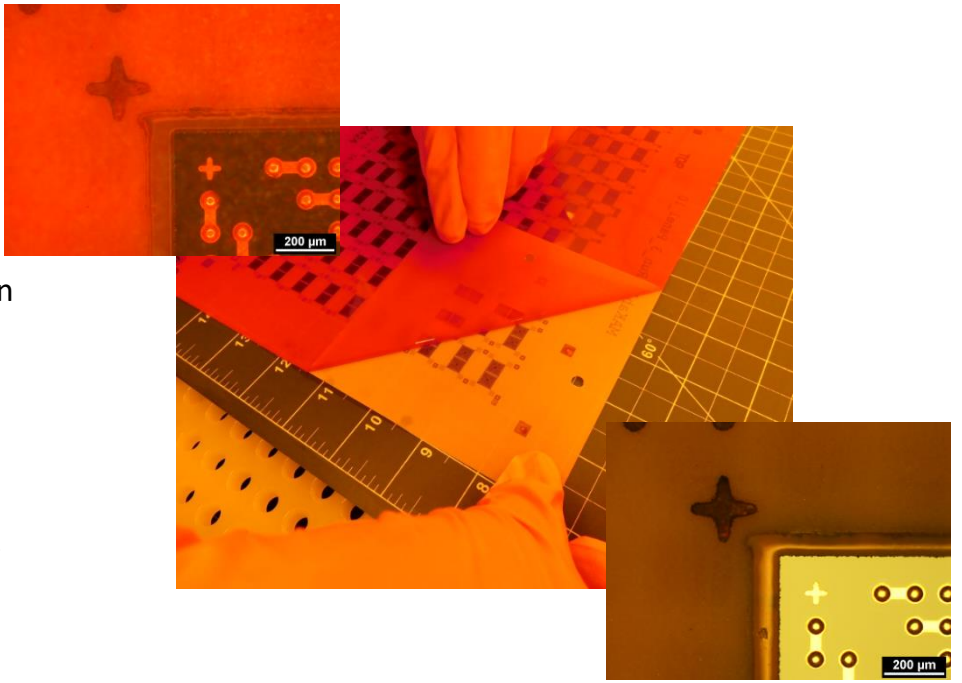
- Vacuum lamination of ABF film (backside)
- Pre cure of dielectric film
- UV – exposure for tape release



ABF- film with PET liner

Core with face-down assemble chips dies

Competent IZM engineer

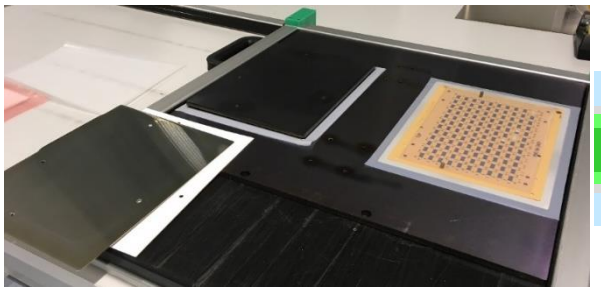


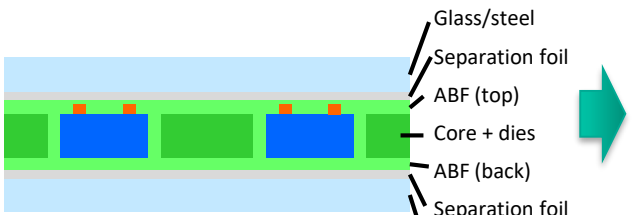
Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

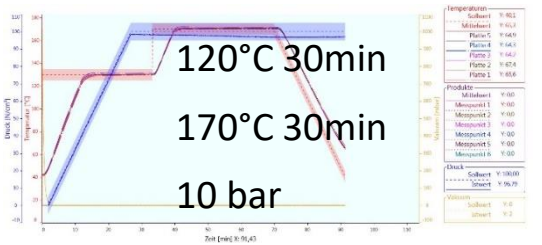
Fraunhofer IZM

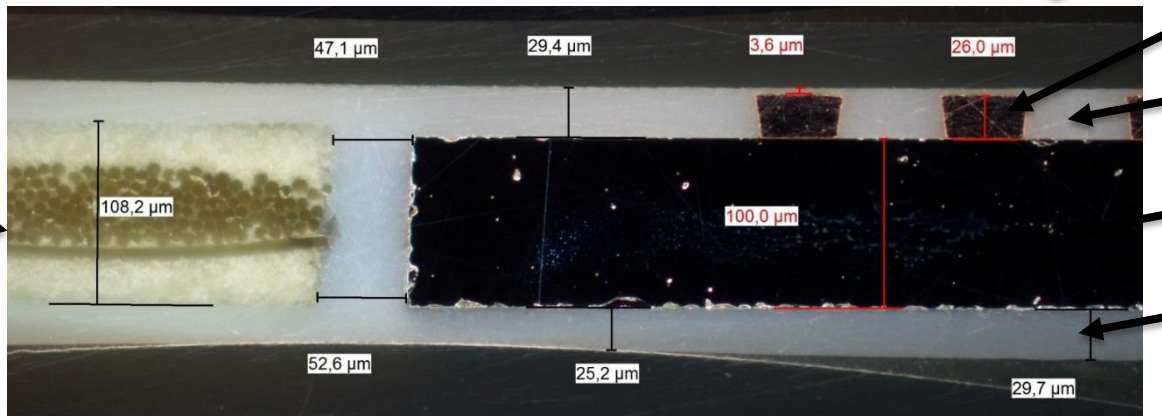
PLP Embedding – Dielectric lamination

- Vacuum lamination of ABF film (frontside)
- Final lamination and embedding in multilayer press









Reinforced PCB core

Bump

ABF

Die

ABF

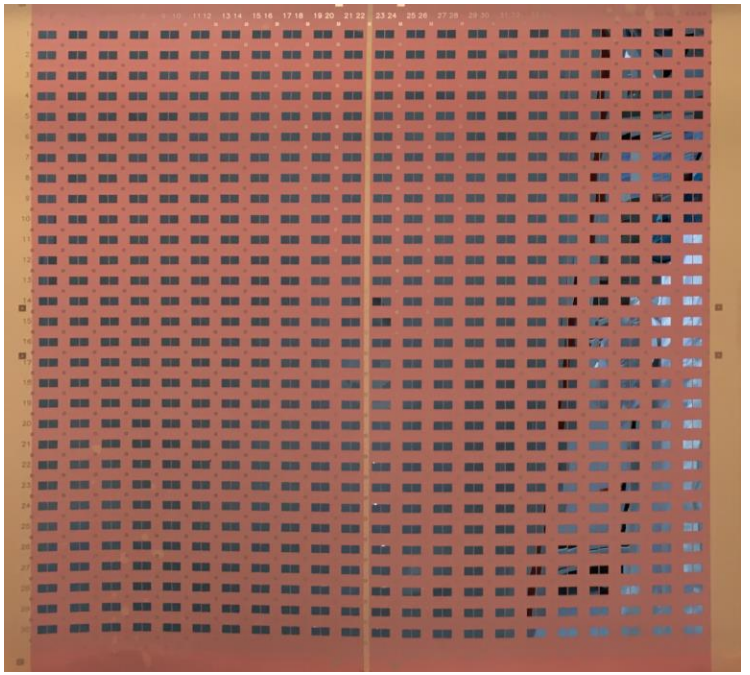
Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

PLP Embedding – Dielectric lamination

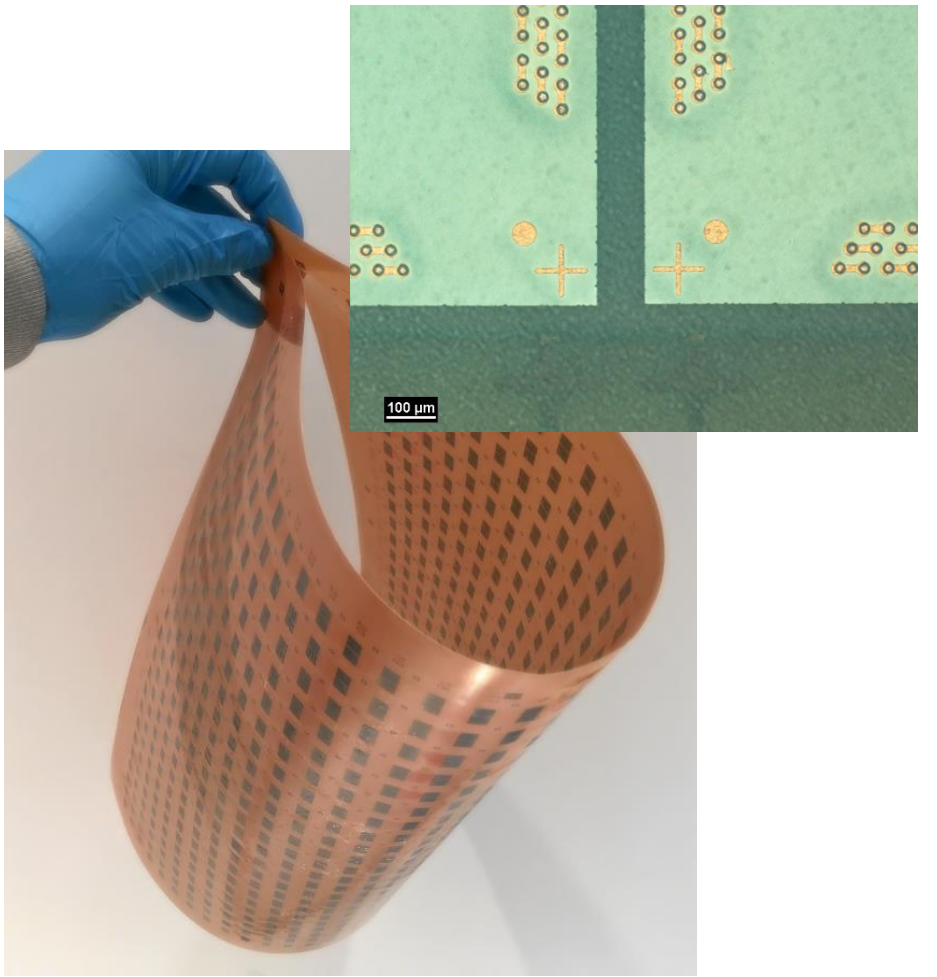
- Use of ABF dielectric film 25 µm thickness
- Application to top and bottom side

total thickness 150 µm (1 RDL layer)

panel warpage measured < 1 mm



Panel with attached chips
before lamination

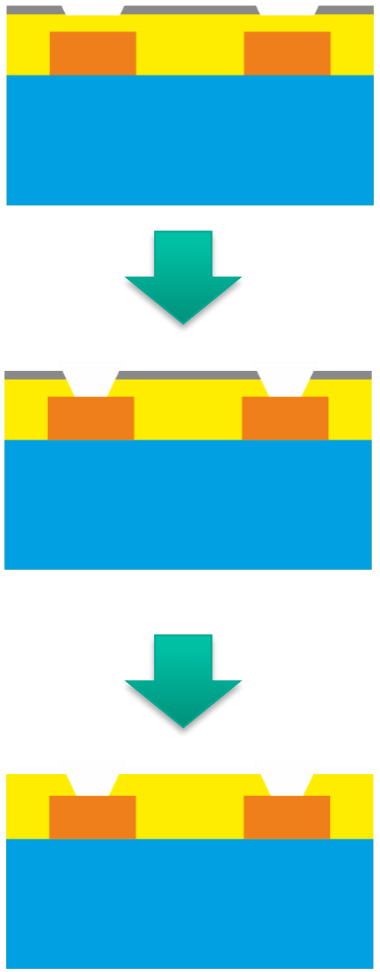


Panel after ABF lamination
Robust substrate allows easy handling

Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

Fraunhofer IZM

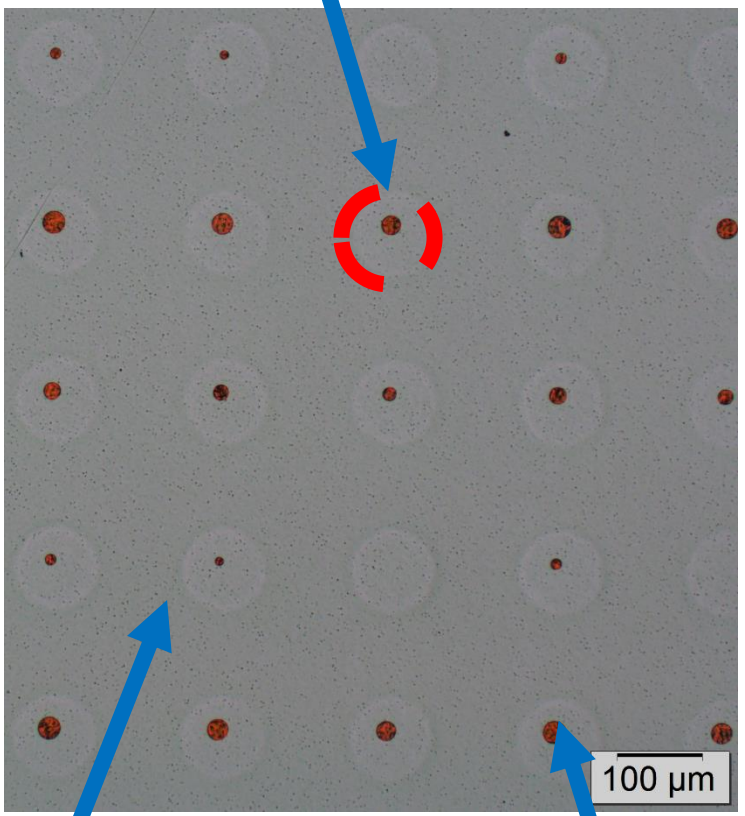
PLP Embedding – Plasma via



Hard mask Formation

Etching of dielectric (RIE)

Removal of metal hard mask

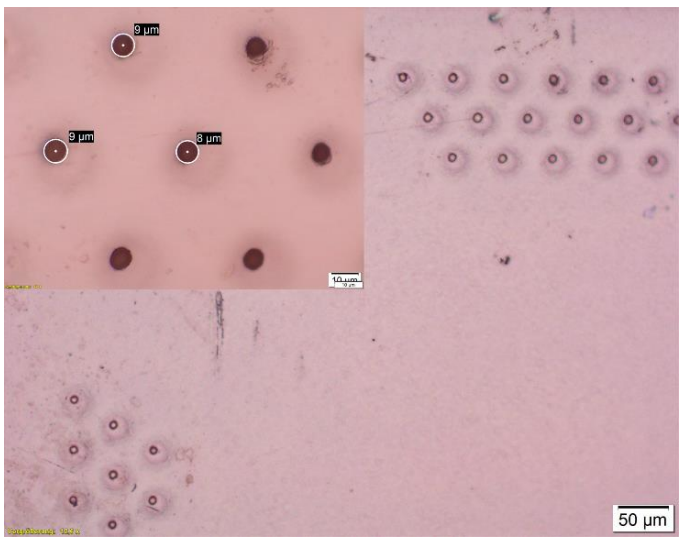


Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

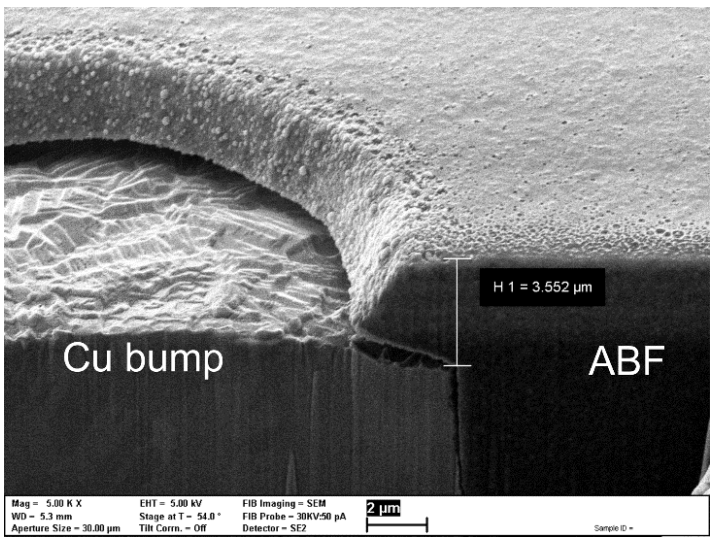
Fraunhofer IZM

PLP Embedding – Plasma via

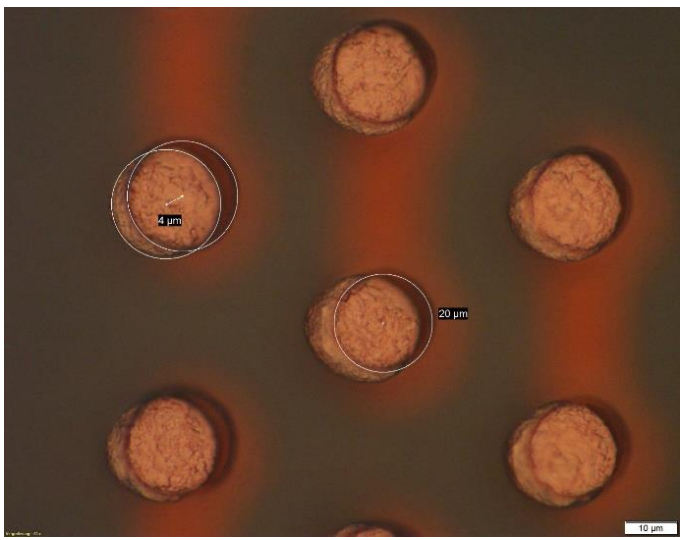
- Ti/Cu hardmask for plasma via
- Adapted imaging of via openings
- RIE etching of ABF above tall Cu pillar structures



Ti/Cu hard mask for plasma via formation



FIB cut of plasma via to embedded die



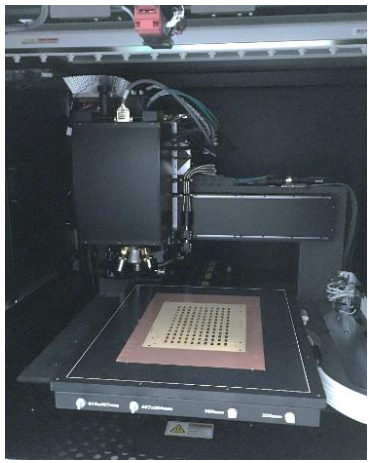
Top view of plasma via to embedded die

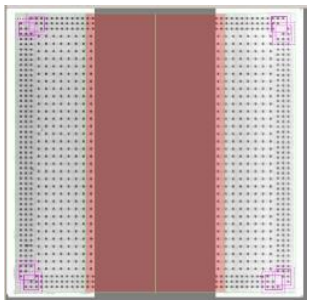
Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

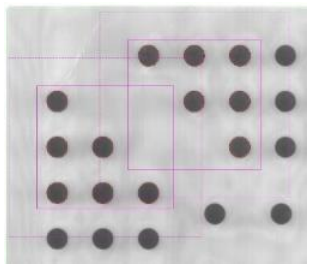
Fraunhofer IZM

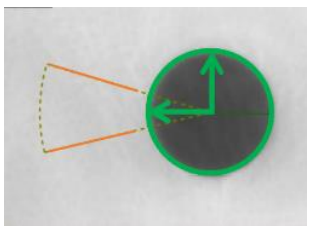
Implementation Adaptive Processing - Method

1. Coordinate Measurement (CMM)

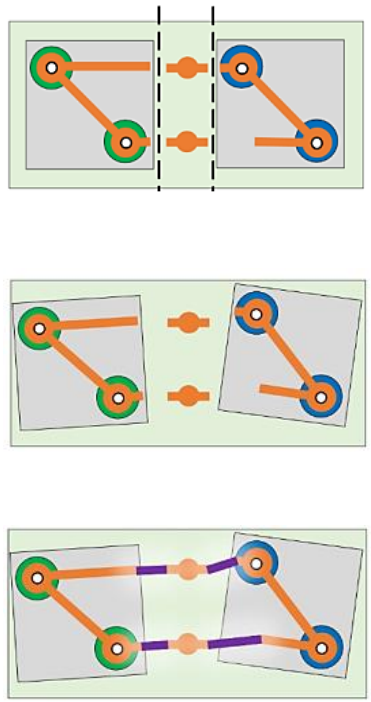


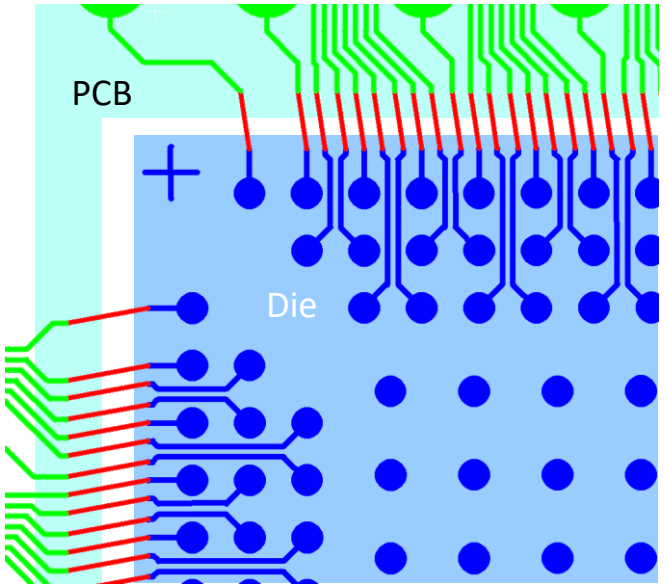






2. Artwork / CAM Data Manipulation





(red) flexible traces

(blue) artwork rotated +translated

(green) artwork fixed

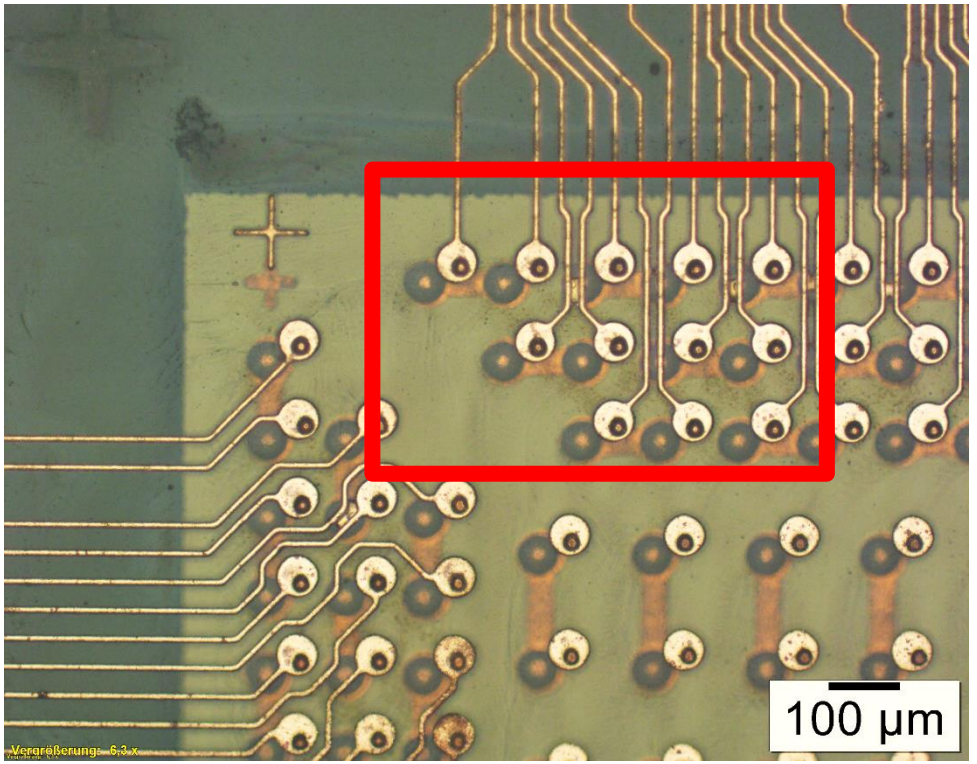
- Time inspect (240 dies) approx. 60s
- Time calc (1 panel, 120 Packages, 4 *gbr layers) < 30s

Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

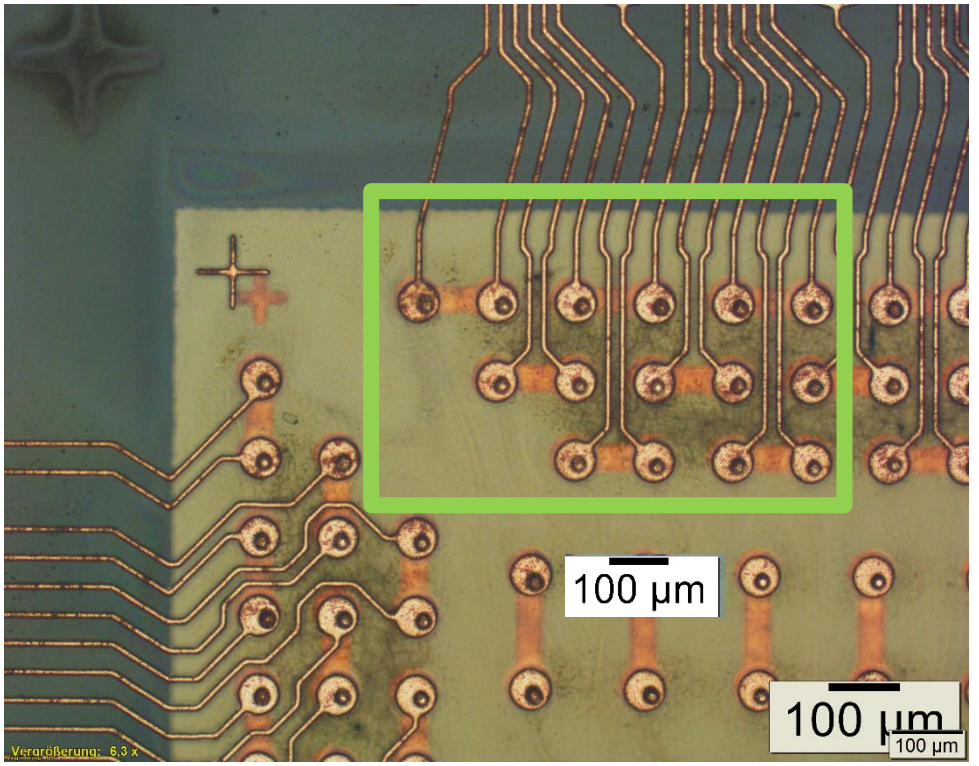
Fraunhofer IZM

Implementation Adaptive Processing - Results

„Classic“ Process



Adapted Process



Yield: ↗

Process Costs: ↘

Process Time: ↘

Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

Fraunhofer IZM

PLP Embedding – RDL Formation

Semi-additive process (SAP)

Sputtering Ti barrier / Cu seed layer

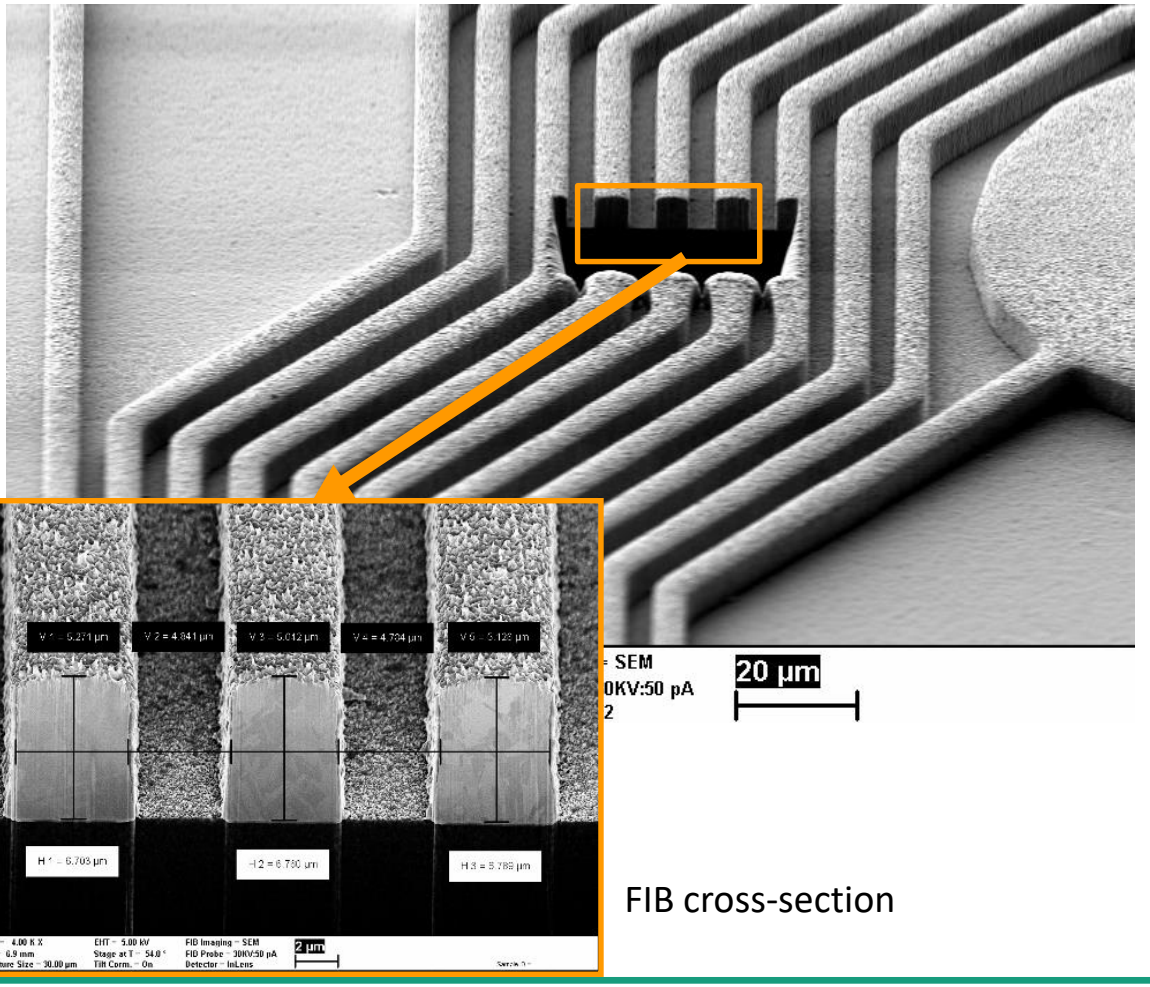
Dry film resist lamination 7 µm Hitachi RY5107

Exposure & development

Cu Plating & resist striping

Differential Ti/Cu etching

Plated Cu traces with **5 µm L/S**



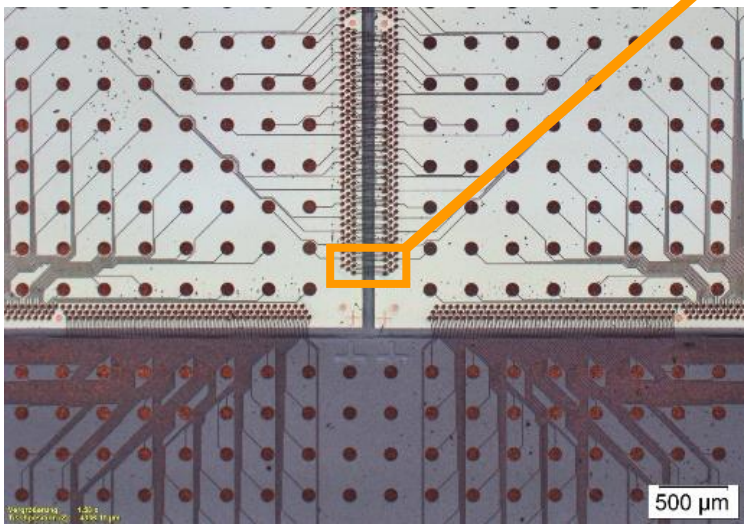
FIB cross-section

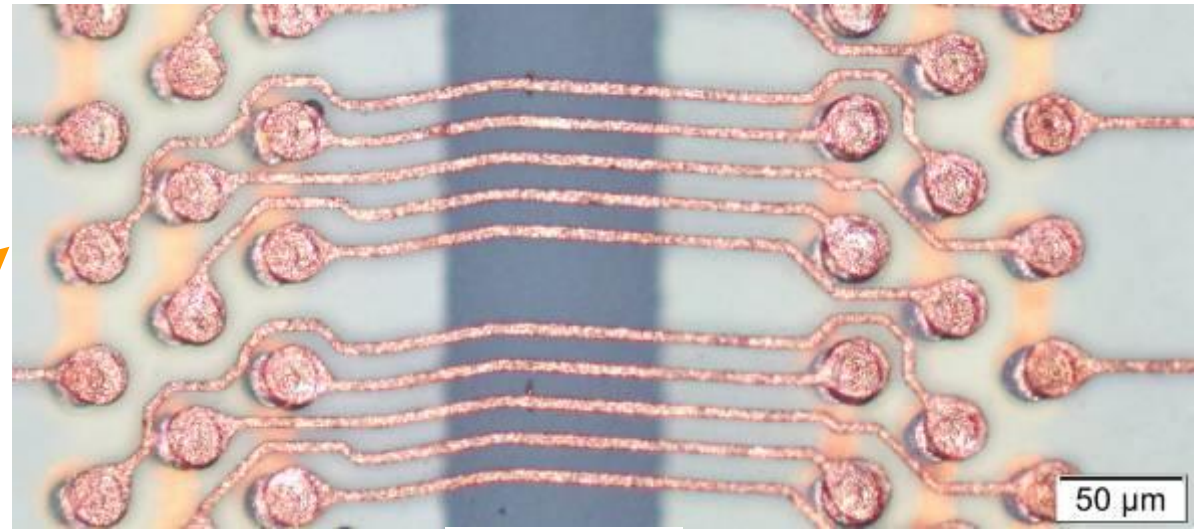
Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

Fraunhofer IZM

PLP Embedding – RDL Formation

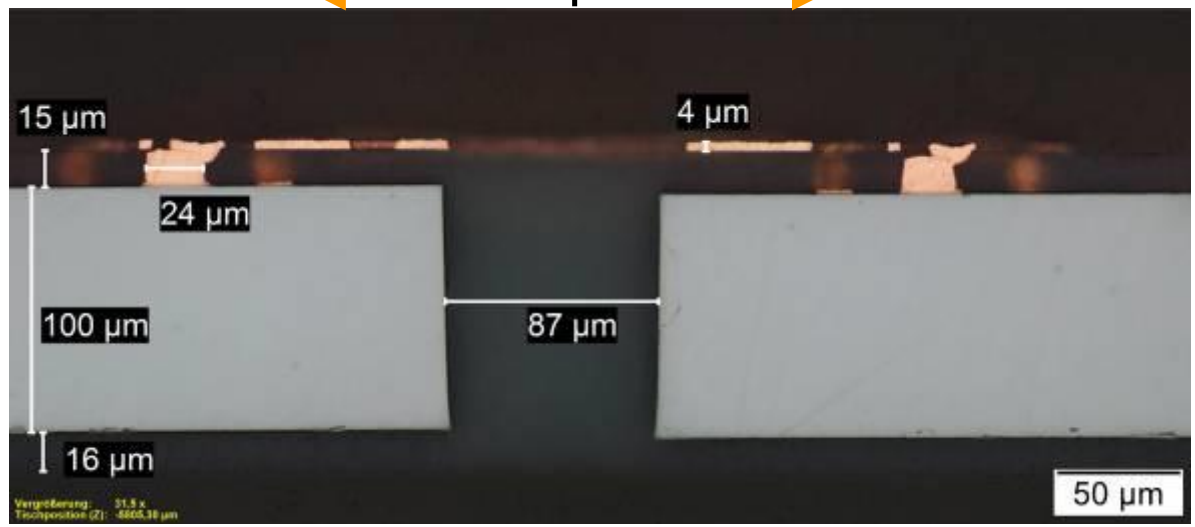
Die 1





Die 2

250 µm

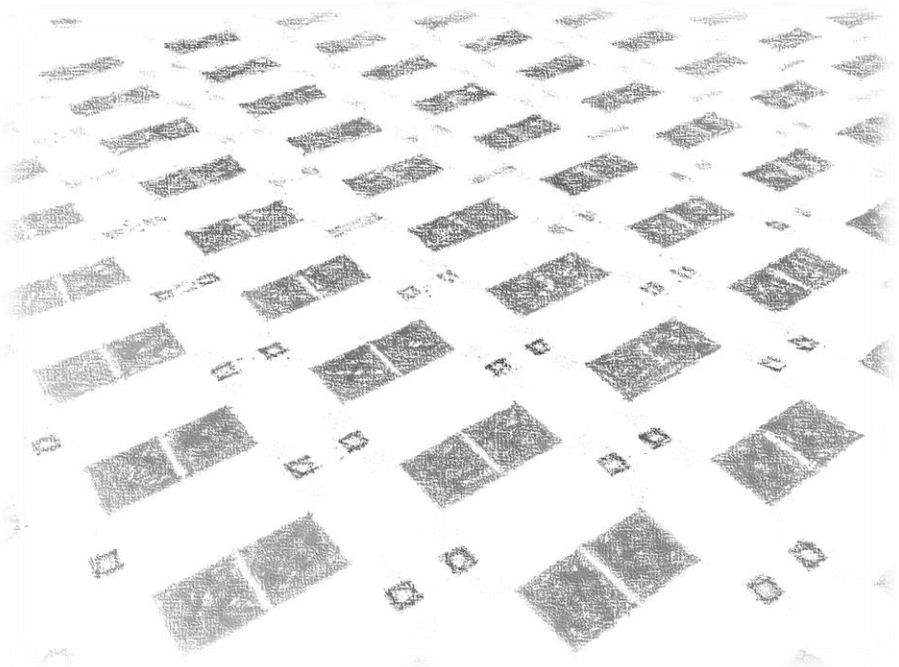


Die-to-die interconnects with 5 µm lines

Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

Fraunhofer IZM

Outline



- Introduction
  - Packging Concept
  - PLP Equipment
- Panel Level Process
  - Test Vehicle
  - RDL Process
  - Adaptive processing
- Conclusion
- Acknowledgements

Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

Fraunhofer IZM

Conclusion

- A new approach for PLP, which focuses on laminate cores and thin dielectric films is currently developed
- Embedding in laminates is an alternative which offers additional features
- A Fan-out PLP process using PCB Cores for multiple chip embedding with 50 µm pitch was demonstrated
- Adaptive Imaging of 5 µm L/S RDL in semi-additive process shown
- Future work will focus on:
  - Yield improvement & process cost reduction
  - RDL wiring down to 2 µm L/S / 5 µm via formation
  - Improvement of Adaptive Processing software

Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de

Fraunhofer IZM

Fraunhofer IZM's Panel Level Packaging Consortia

PLC 1.0 – 2017/2018

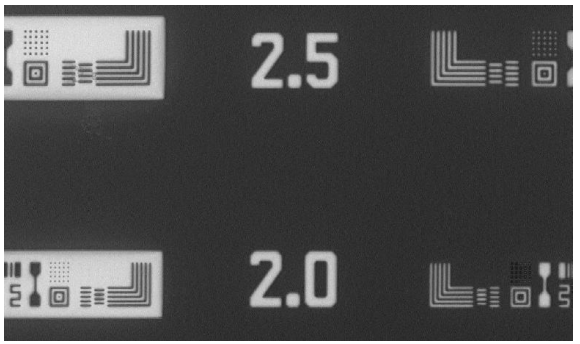
- Chip-first, face-down PLP
- 10 µm L/S RDL
- 610x456 mm² panel format

PLC 2.0 – 2020/2021

Technical goals

- RDL from 5 µm to 2 µm L/S
- Litho & plating towards 1 µm
- Adaptive processing
- 610x456 mm² panel format

Consortium partners can still join



lars.boettcher@izm.fraunhofer.de

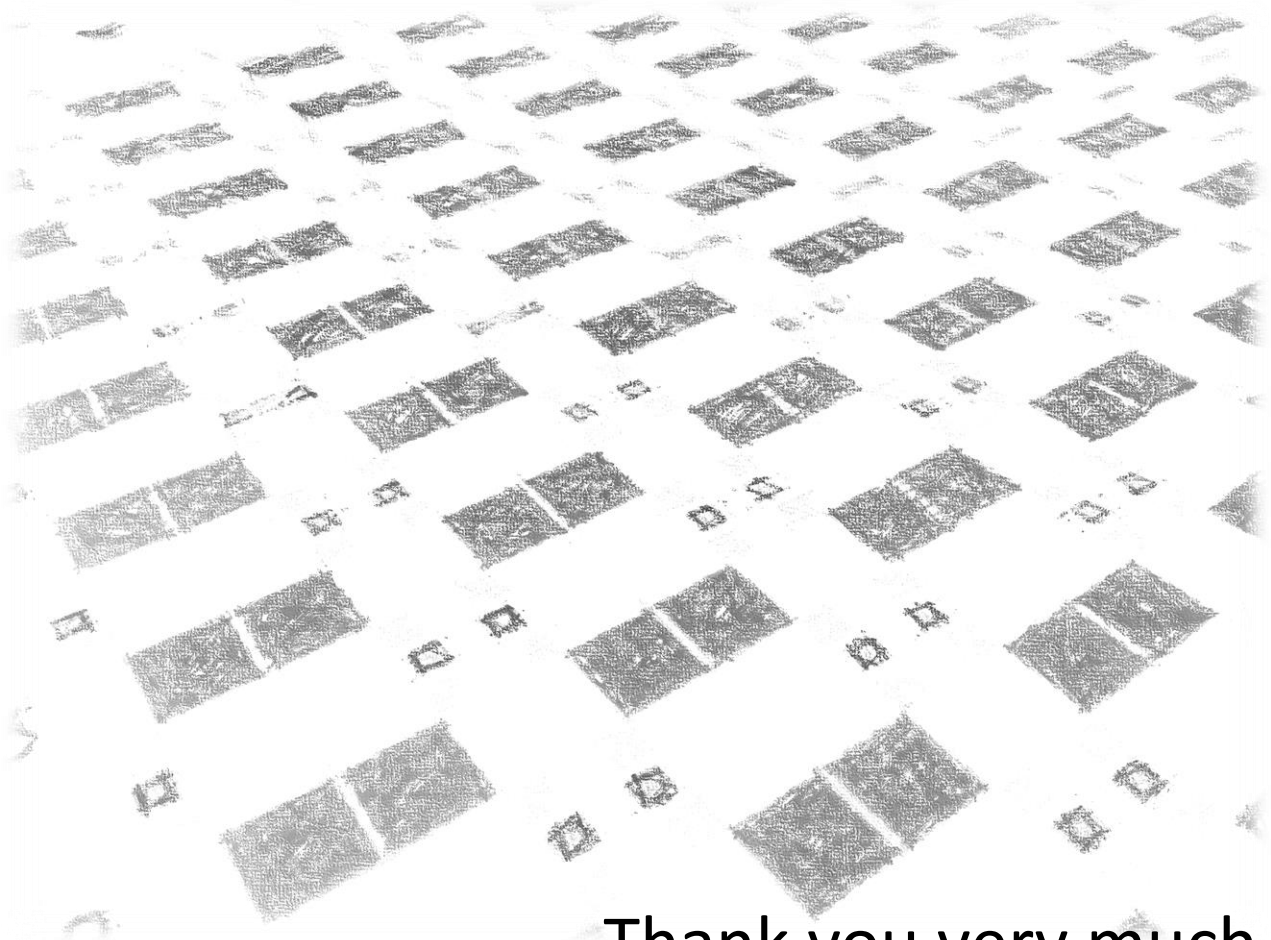
Acknowledgement

- German “Federal Ministry of Education and Research” for the financial support of the:
  - PEKOS project (FKZ 16ES0718K)

GEFÖRDERT VOM

Bundesministerium
für Bildung
und Forschung

Lars Böttcher, System Integration & Interconnection Technologies
lars.boettcher@izm.fraunhofer.de



Thank you very much for your attention!

Contact: Lars.Boettcher@izm.fraunhofer.de