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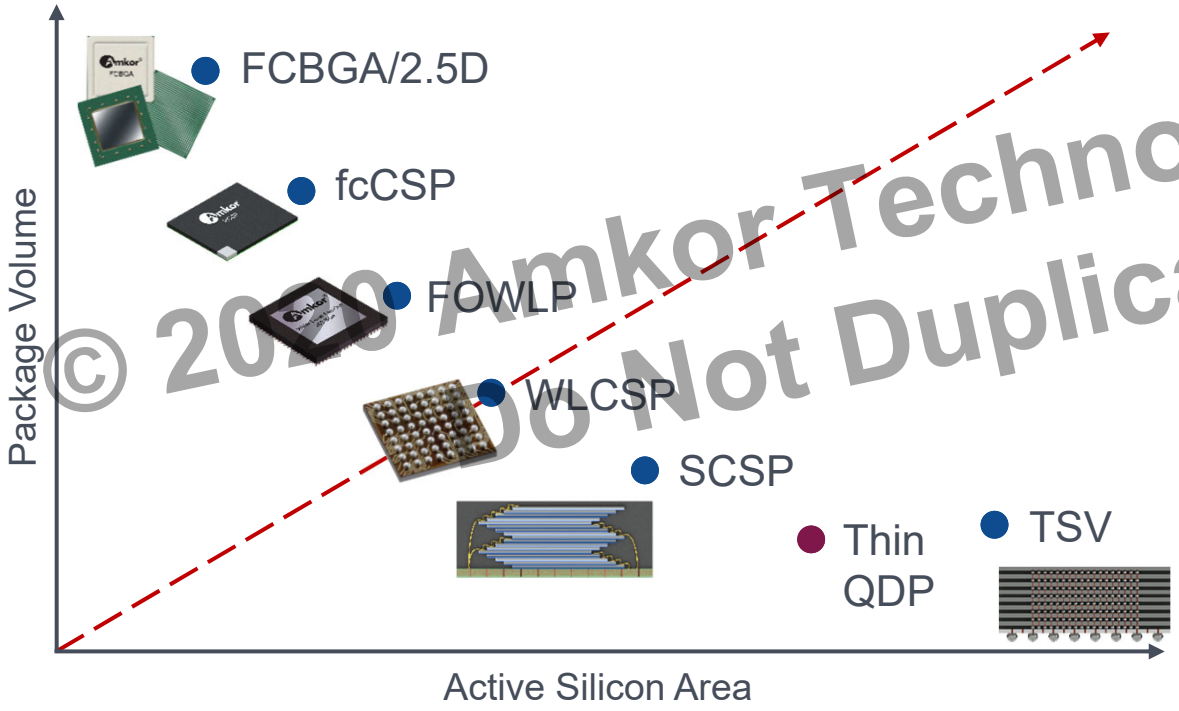
Thin Quad Die Package (QDP) Development

Shaun Bowers I VP
Mainstream Advanced Package Integration

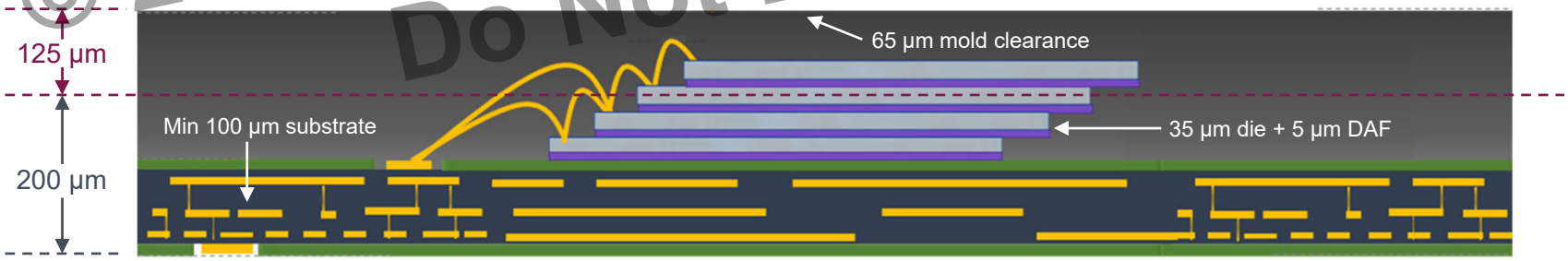
3D Integration Does Not Have to be TSV



- In memory packaging, bit density: Si area density
- Capability for low I/O density, high Si area packaging
  - Less I/O dense than TSV memory
  - Smaller package volume

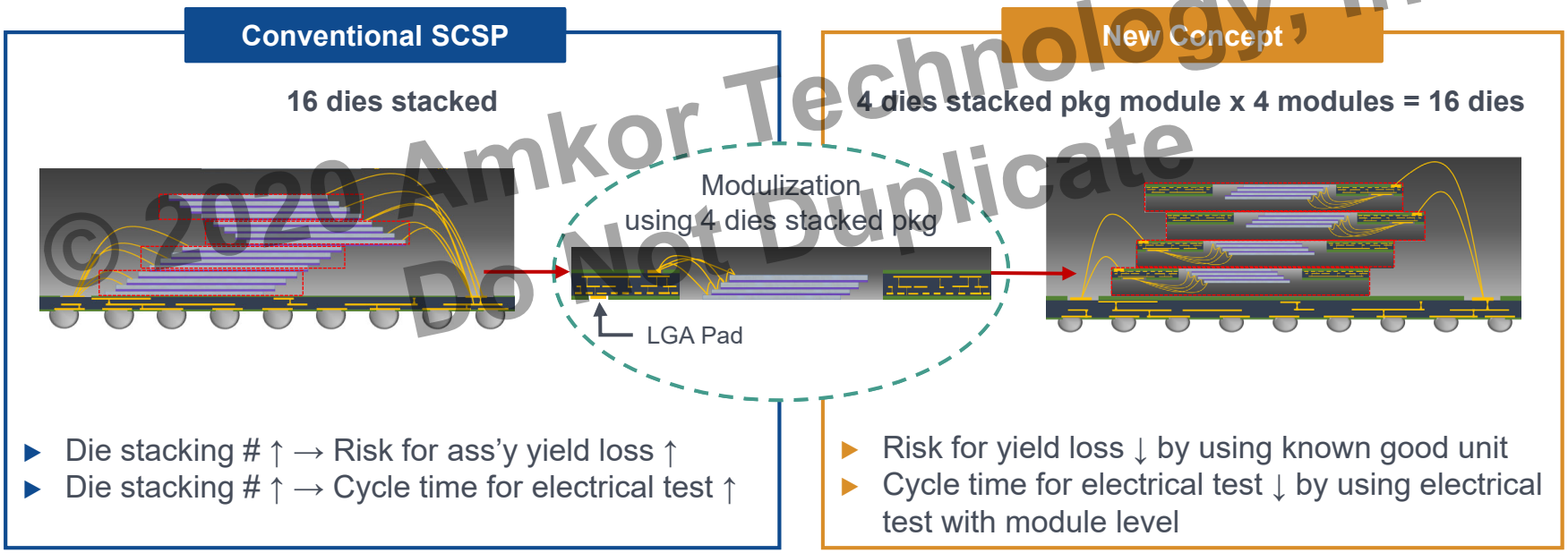
The Challenge

- Four die stacked (QDP)
- 200 µm package thickness
  - Reduce from ~325 µm thickness
- Ability to integrate multiple QDP into a larger package



Ultra-thin QDP Concept

- Modularization using 4 dies stacked package

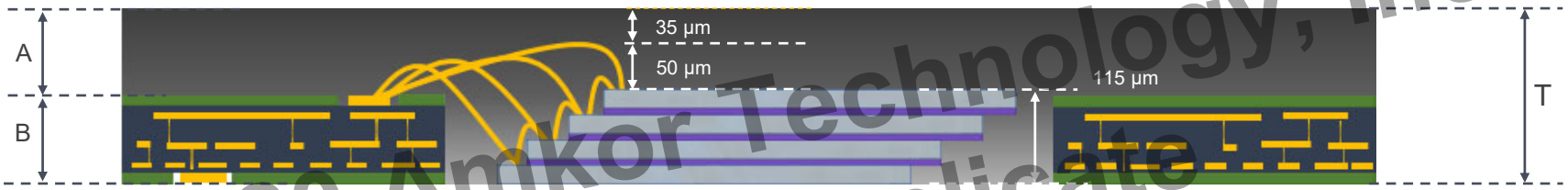


- Die stacking # ↑ → Risk for ass'y yield loss ↑
- Die stacking # ↑ → Cycle time for electrical test ↑

- Risk for yield loss ↓ by using known good unit
- Cycle time for electrical test ↓ by using electrical test with module level

200 µm QDP Design Concept Details

- Stack-up analysis (QDP)

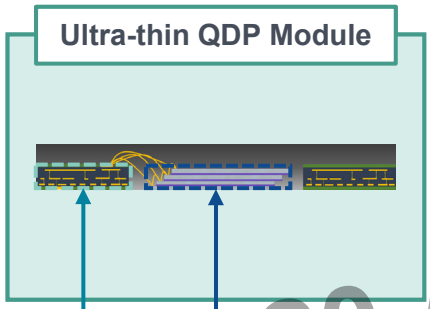


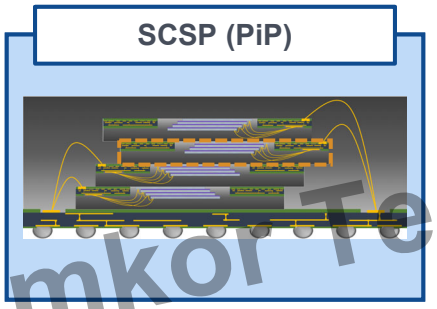
$$\text{RSS Tolerance} = \sqrt{T_1^2 + T_2^2 + T_3^2 + \ldots}$$

Symbol	Description	Unit	Nominal	Tolerance
A	Mold thickness	mm	0.100	±0.03
B	PCB	mm	0.100	±0.03
T	Total height	mm	0.200	±0.042

Additional information
- Die thickness: 25 µm
- DAF thickness: 5 µm
- Wire loop height: max 50 µm (0.8 mil)

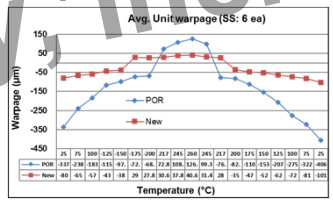
Key Technologies for QDP





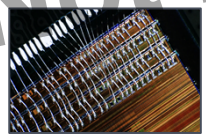
3. Warpage control for 200 µm QDP

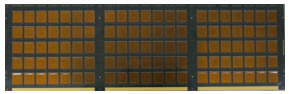
- Evaluation of architecture
  - Laminate design
  - EMC Volume
  - Si Volume
- Evaluation of EMC

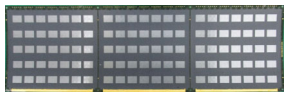


1. Full cavity substrate with TBDB

- Temporary Bonding Debonding (TBDB)
- Die stacking, wirebonding on TBDB
- Mold with full cavity substrate and TBDB

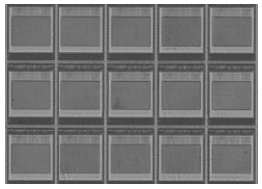






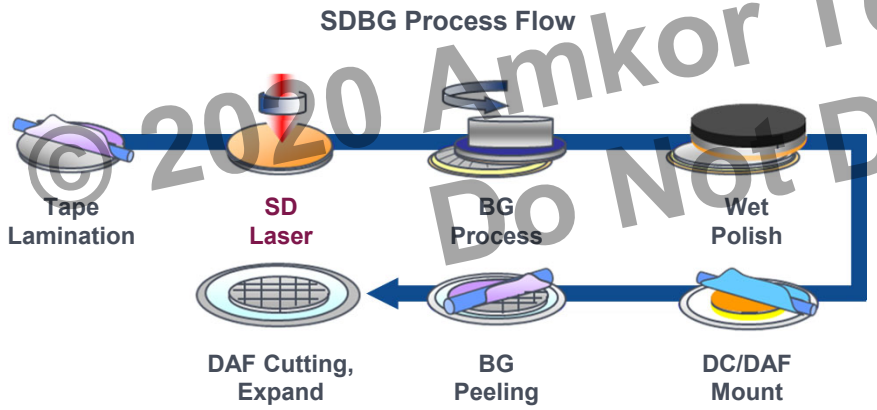
2. D/P and die stacking for ultra-thin die

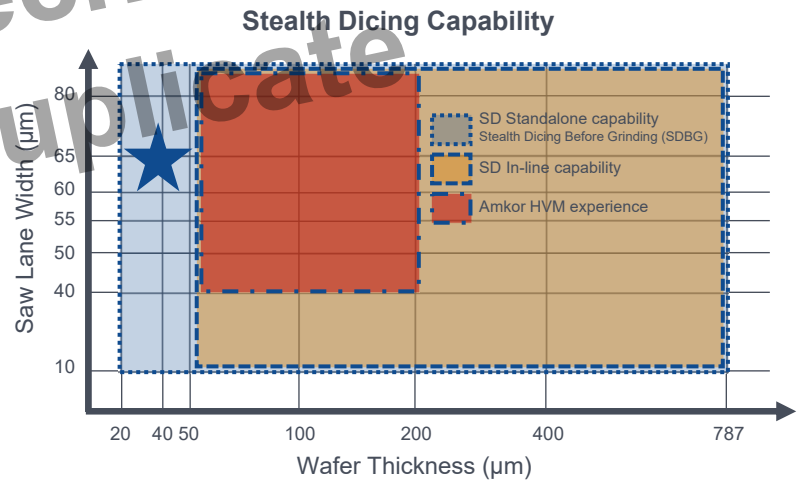
- Stealth Dicing Before Grinding (SDBG)
  - D/P Process optimization (Under 30 µm)
- Ultra-thin die stacking
  - Control of ultra-thin die warpage
  - Stacking tool development & process optimization for die crack & misalignment



Wafer Processing for thin QDP

- D/P and die stacking for ultra-thin die
  - Application of Stealth Dicing Before Grinding (SDBG)

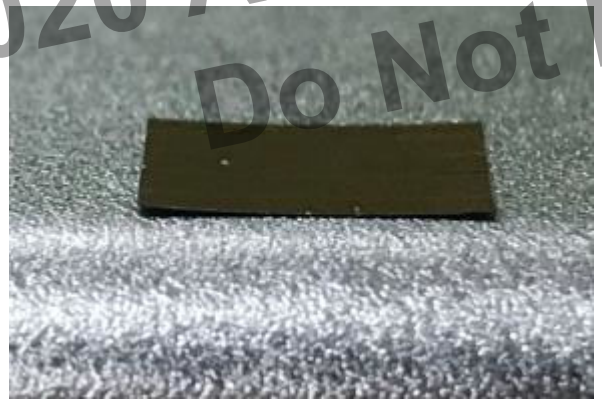




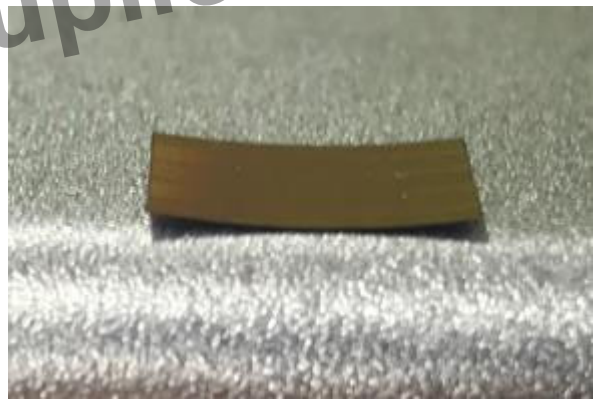
Die Warpage

	Min	Max	Avg.	St Dev
w/o DAF	87.4 µm	104.5 µm	92.16 µm	7.53 µm
w/DAF	275.3 µm	292.3 µm	277.7 µm	13.77 µm

w/o DAF (1st Stacked Die)

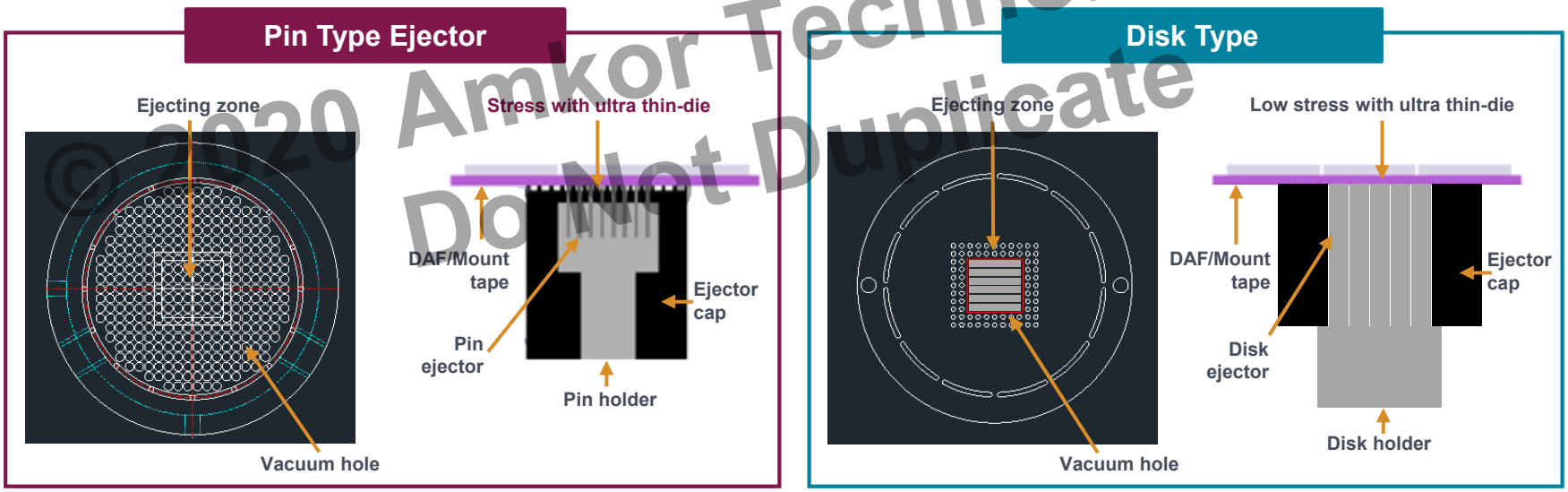


DAF (2nd~4th Stacked Die)

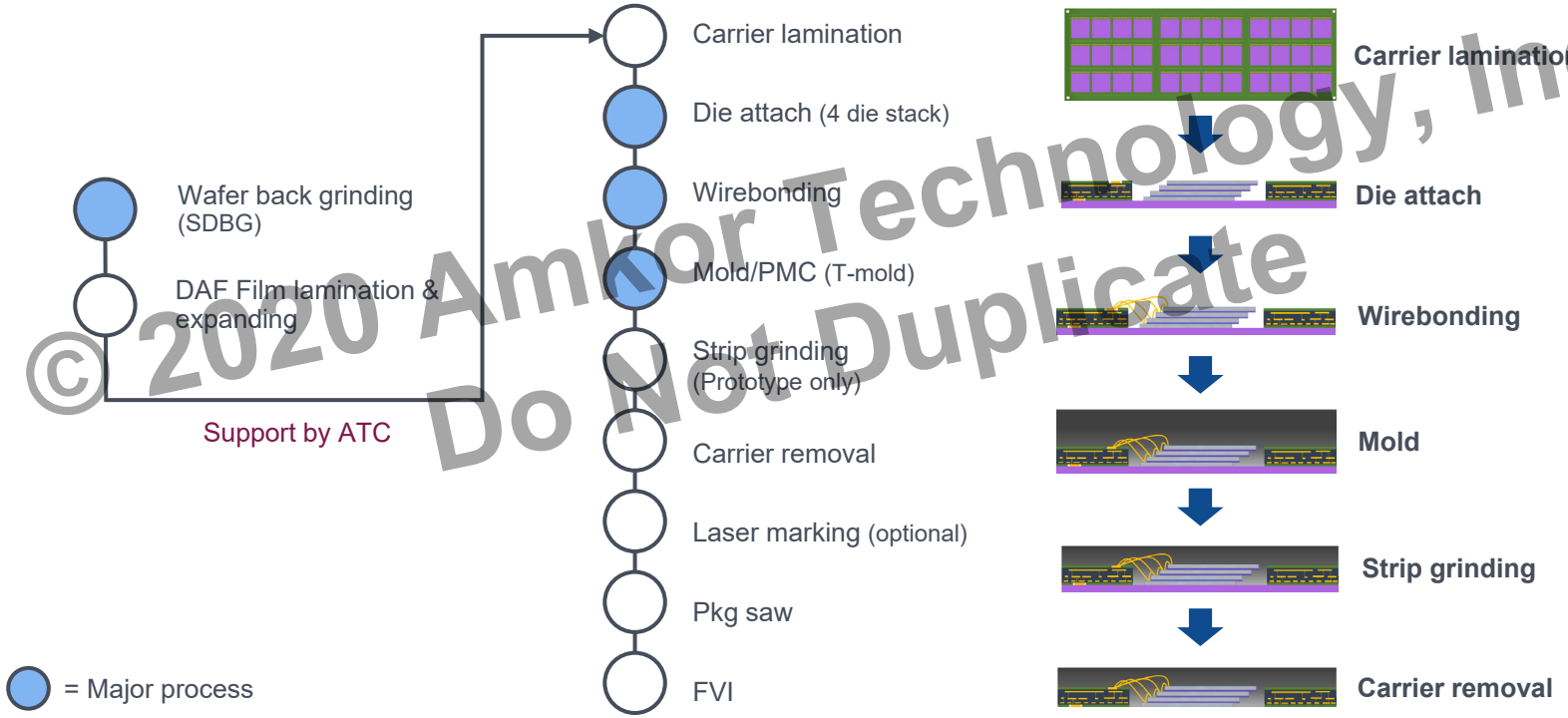


Die Processing for Thin QDP

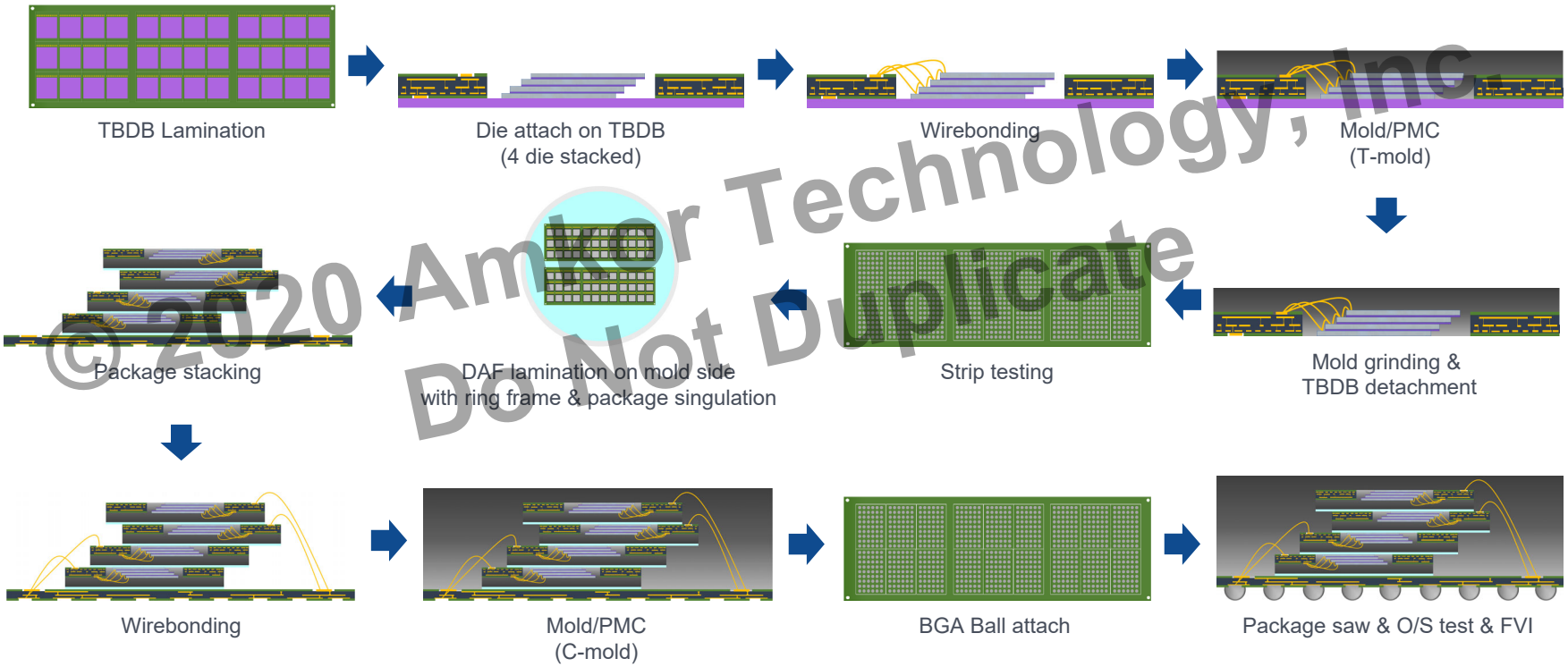
- D/P and die stacking for ultra-thin die
  - Applicated disk type ejector to prevent die crack
    - Less die stress during die ejecting from large surface and step ejecting



200 µm QDP Package Process Flow

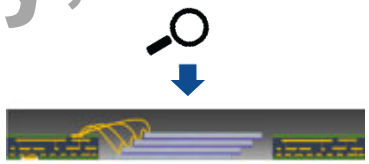


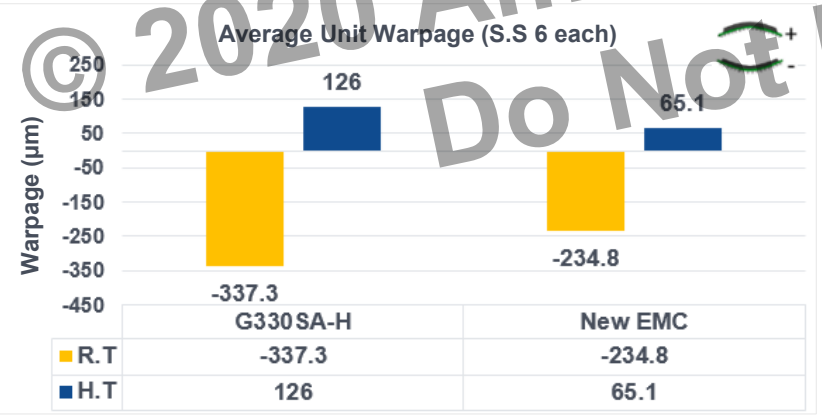
200 µm QDP and ODP Process Flow



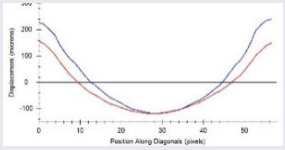
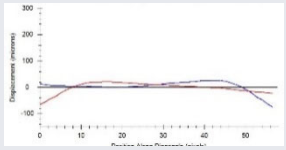
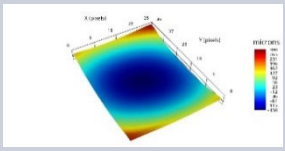
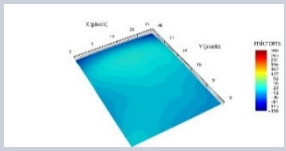
Initial Warpage Result Summary

- **Showed severe smile unit warpage at R.T**
  - G330SA-H: Avg. -337.3 µm @ R.T, Avg. 126 µm @ H.T
    - Avg. -115.8 @ 125°C (QDP stacking process temp. for ODP)
  - New EMC: Avg. -234.8 µm @ R.T, Avg. 65.1 µm @ H.T
    - Avg. -104 @ 125°C (QDP stacking process temp. for ODP)

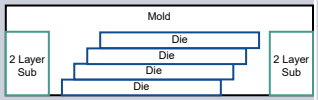
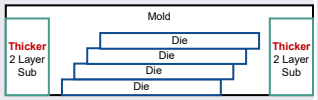
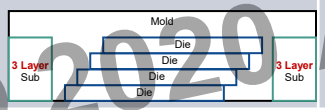
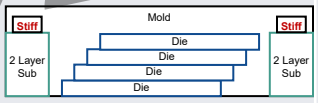


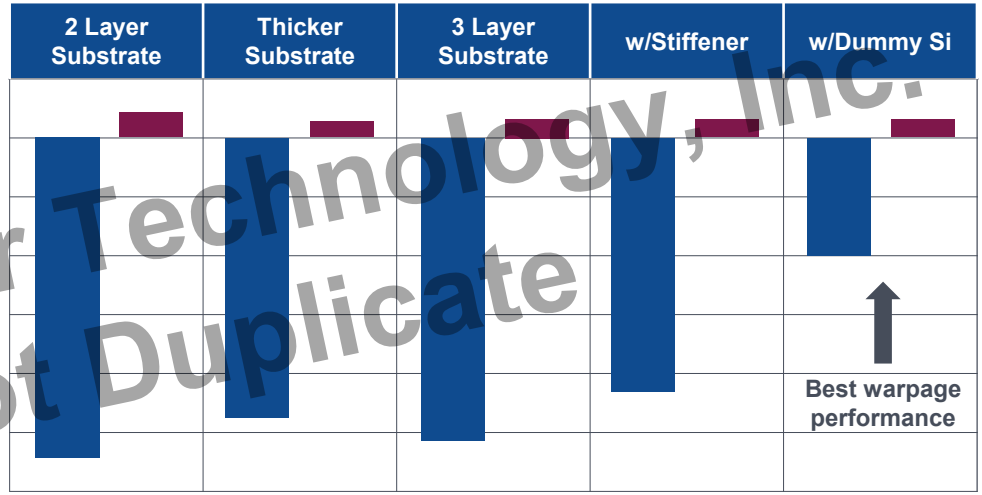


	G330SA-H	New EMC
R.T	-337.3	-234.8
H.T	126	65.1

Warpage Mode (G330SA-H, mold side)	@ R.T	@ H.T
2D Image		
3D Image		

Thin QDP Warpage Countermeasures

Leg	Package Structure	
1		2 Layer substrate
2		Thicker substrate (100 µm → 120 µm)
3		3 Layer coreless
4		With stiffener (60 µm T.)
5		With dummy (65 µm T.)



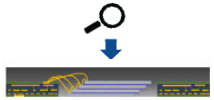
Plots showing relative difference in warpage for various legs

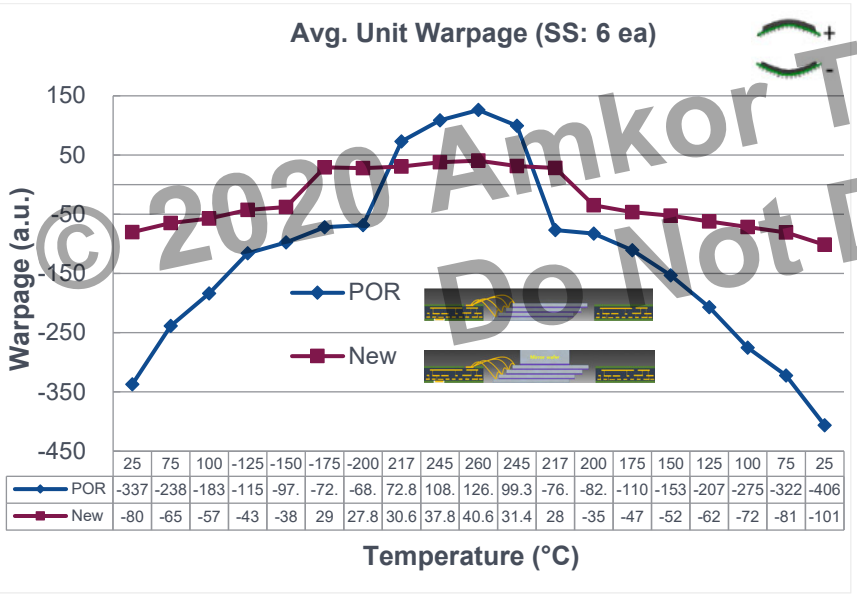
Dummy Si showed better unit warpage performance among the 5 legs

Dynamic Warpage FEA Data for QDP and ODP

Unit warpage for QDP & ODP

QDP Unit Warpage

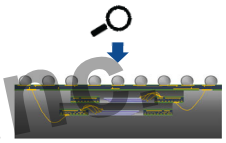


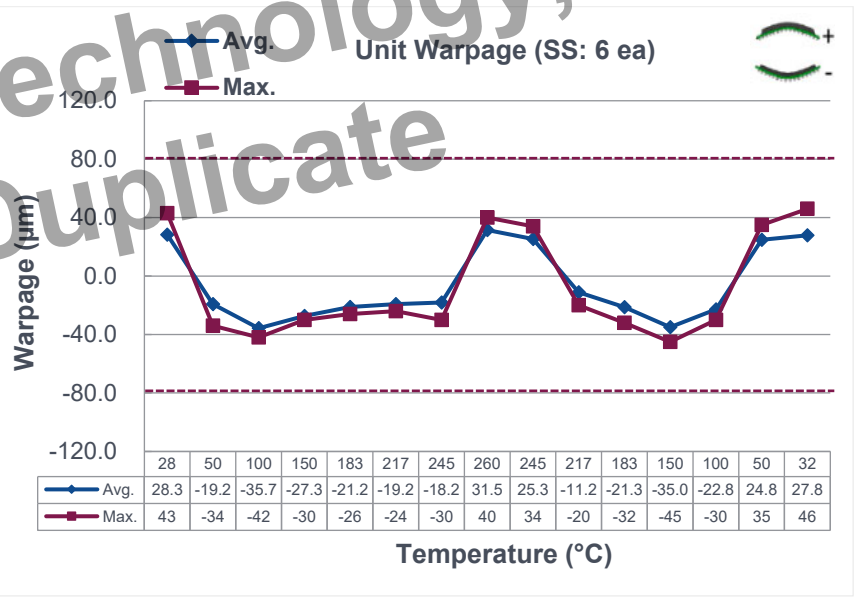


	25	75	100	-125	-150	-175	-200	217	245	260	245	217	200	175	150	125	100	75	25
POR	-337	-238	-183	-115	-97.	-72.	-68.	72.8	108.	126.	99.3	-76.	-82.	-110	-153	-207	-275	-322	-406
New	-80	-65	-57	-43	-38	29	27.8	30.6	37.8	40.6	31.4	28	-35	-47	-52	-62	-72	-81	-101

Temperature (°C)

ODP Unit Warpage



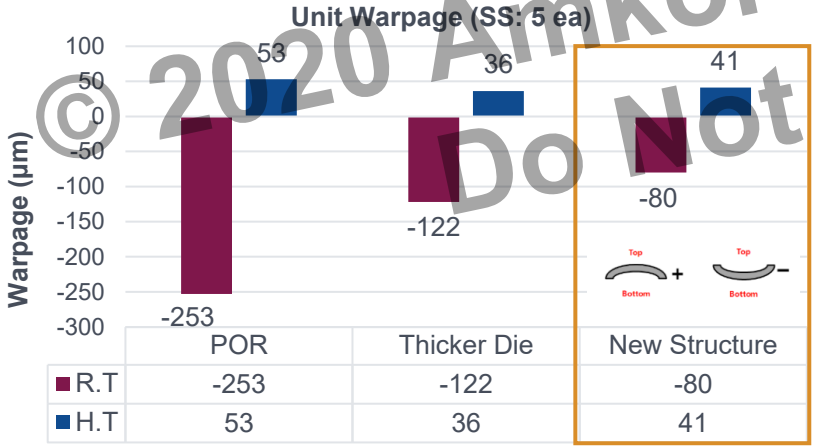


	28	50	100	150	183	217	245	260	245	217	183	150	100	50	32
Avg.	28.3	-19.2	-35.7	-27.3	-21.2	-19.2	-18.2	31.5	25.3	-11.2	-21.3	-35.0	-22.8	24.8	27.8
Max.	43	-34	-42	-30	-26	-24	-30	40	34	-20	-32	-45	-30	35	46

Temperature (°C)

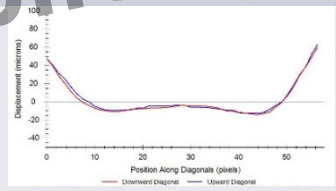
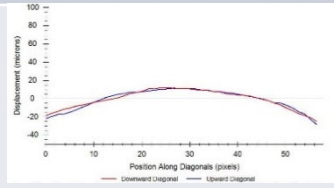
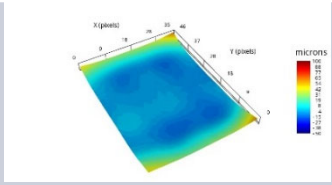
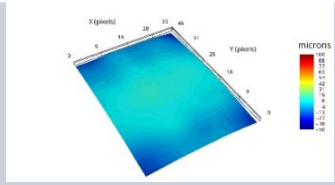
Preliminary Test for New Structure

- Unit warpage
  - Showed excellent unit warpage performance compared to POR structure
    - Avg. 80 µm, max 92 µm @ R.T
    - Avg. 41 µm, max 48 µm @ H.T



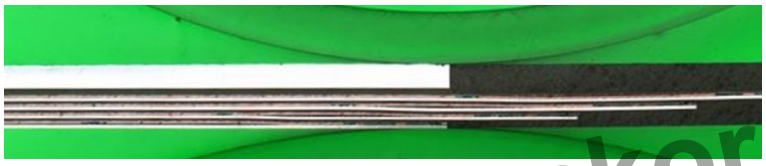
	Thin QDP (New Proposal)	ODP (Thin QDP)	QDP (3D NAND)	ODP (3D NAND)
Unit Warpage	80 µm	45 µm	75 µm spec (50 µm observed)	75 µm spec (50 µm observed)
Strip Warpage	2 mm	Almost flat	3~4 mm	3~4 mm

Warpage Mode with New Structure (Mold Side)

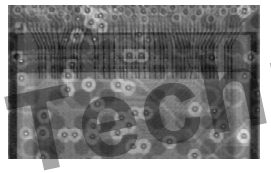
	@ R.T	@ H.T
2D Image		
3D Image		

Reliability Performance for QDP

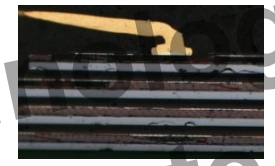
Passed all items



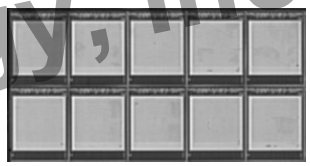
X-ray Image



Cross-section Image



SAT Image



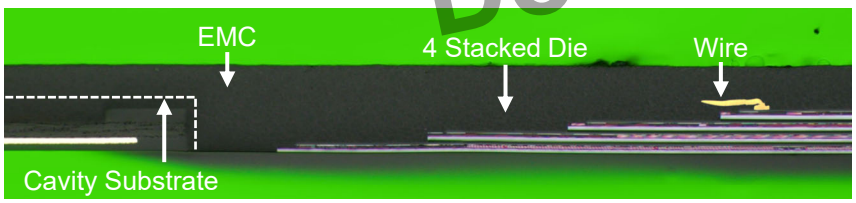
Test Items		Condition	SS (ea)	Reject Qty (ea)	Result	Remark
MRT	L3	30°C/60% 192 hrs	22	0/22	Pass	N/A
Rel. only	HTS	150°C/1000 hrs	22	0/22	Pass	N/A
Rel. with Precon.	HAST	130°C/85%RH, 96 hrs	22	0/22	Pass	N/A
Rel. with Precon.	T/C B 1000x	-55/125°C	22	0/22	Pass	N/A

Stack-up Analysis for Thin QDP

Design vs. Actual

Design

Actual



S/S: 5 units (µm)

Symbol		Design	Actual
T	**Total**	**200**	**203.5**
A	Mold thickness	100	99.2
A1	Wire to mold top clearance	35	28.3
A2	Wire loop height	50	56.7
B	4 Die stacked thickness	115	113.2
B1	W/B Die thickness	25	23.1
B2	DAF Thickness	5	4.25
C	PCB Thickness (2 layer)	100	104.3

Development Details

- Conclusion
  - Within 4u of the target thickness
  - Ability to integrate into Package in Package (PiP)
  - Package warpage and reliability within standard SCSP limits

W/B with 4 die stack

Top & BTM view of QDP

Cross-section image of QDP (Design vs. Actual)

Wirebonding side

Opposite side

	Symbol	Design	Actual
T	Total	200	203.5
A	Mold thickness	100	99.2
A1	Wire to mold top clearance	35	28.3
A2	Wire loop height	50	56.7
B	4 Die stacked thickness	115	113.2
B1	W/B Die thickness	25	23.1
B2	DAF Thickness	5	4.25
C	PCB Thickness (2 layer)	100	104.3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