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International Microelectronics
Assembly & Packaging Society

An Embedded Planar-Foil Capacitor Material, FPGA Based Interposer, Aimed at Improving System Performance and Reduce Board Size for Space Based Electronics

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Ben Cheng (EE)

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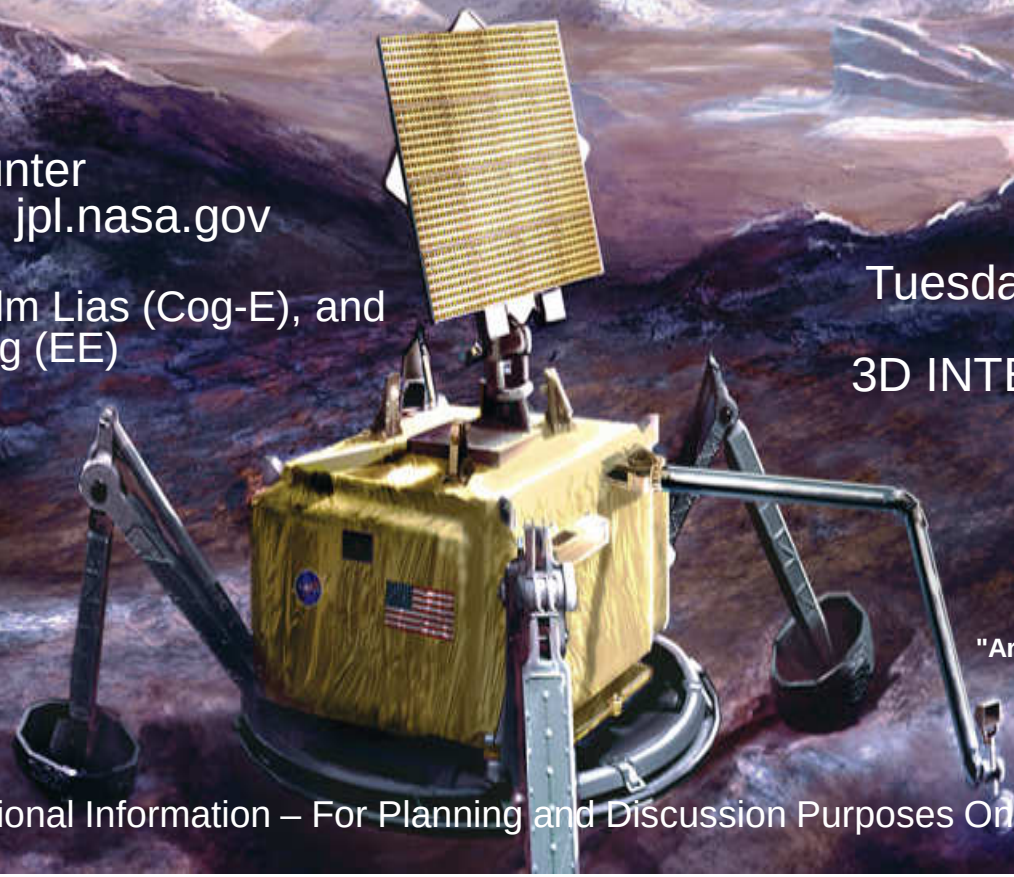
3D INTEGRATION Track
016



"Artist's Concept"

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Rating

G	General Audience
Anyone is invited	

NDR	Not a Design Review
Questions are welcome	

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Agenda

- Introduction
- Architecture
- Key technology Development
- PWB Design
- System Integration
- Validation and Analysis
- Conclusion
- Wrap Up and Questions

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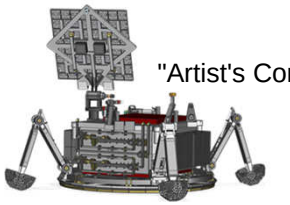
Introduction

- This work is part of the JPL/NASA Europa Lander's Technology Maturation effort, with the focused on a miniaturized next generation Motor Control.
- Europa Lander - Ocean World Missions require a spacecraft launch mass 7-10X the landed mass due to the required propellant to get the payload to the surface.
- Our technology effort supports the decrease in landed mass by utilizing advanced substrate and System-in-Package (SiP) technologies that can be configured into a compact yet versatile avionics topologies that significantly reduces Size, Weight, and Power (SWaP) over previously flown SoP avionics assemblies.
- The use of planer-foil capacitors technology systems are not new to the industry. The focus of our planar-foil based capacitor interposer and integrated FPGA topology follows the SiP theme, by developing a standardized integrated solution, resulting in an overall reduction in our Printed Wiring Board (PWB) area and system Motor Control system mass.
- We will show how this freed space traditionally used for bypass capacitors will be leveraged when developing highly integrated avionics solution.

Leverage past flight experience and high-TRL tech development to reduce mission risk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Introduction

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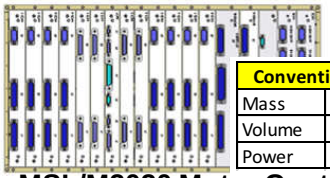
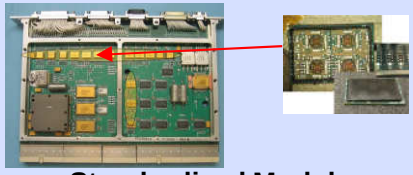


Conventional Motor Control		
Mass	14.13	Kg
Volume	11250	cc
Power	26	W

MSL/M2020 Motor Controller

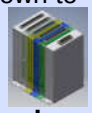
- *Non modular design*
- *Conventional electronic packaging*
- *Card cage and backplane interconnect*

NEW INSIGHTS



Standardized Modules

- Flight electronic design have similar designs repeated many times
- Making standardized multi-chip modules can lead to 10x reduction in board area
- i3's packaging allows for packaging at the die level and for survival temperatures down to -180C.



Slice based packaging

- Slice based design and serial board to board connections eliminates need for chassis and backplane

ACHIEVEMENT

Motor Control Modules:

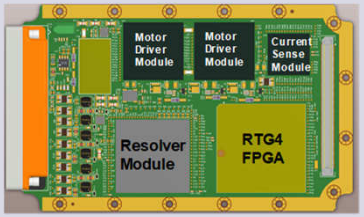
- Modules developed for all motor control functions:
  - Motor Driver
  - Resolver
  - Current Sensor
  - Point of Load

Resolver Module

Motor Driver Module

Motor Control Card:

- Incorporates modules mentioned above
- Can control up to 3 Brushless DC Motors
- One motor being operated per card
- Europa Lander Baseline



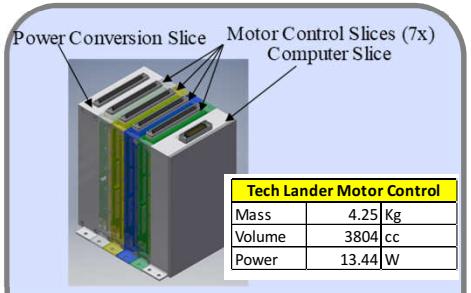
Europa Lander Motor Control Card (10cm x 16cm)

Cold Survivable Distributed Motor Controller (CSDMC)

- Controls 1X - 3A Brushless DC Motor
- -180C storage Temperature
- (under development)

Proposed Cold Survivable Distributed Motor Controller (10cm x 10cm)

QUANTITATIVE IMPACT



Tech Lander Motor Control		
Mass	4.25	Kg
Volume	3804	cc
Power	13.44	W

Europa Lander Motor Control Controller

MAJOR IMPACT ON Missions:

- 4x reduction in volume
- 3x reduction in mass
- Survival heater energy eliminated

END-OF-TASK OBJECTIVES

- **Increased science return**
  - **More room for science instruments**
  - **Longer mission life through more room for batteries**

Funding Sources: NASA GCD, NASA COLDTECH, JPL R&TD, Europa Lander Focused Technology.

Partners: i3 Electronics

4x reduction in volume and 3x reduction over SoP. More science return!

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Architecture

- To achieve reduced fluctuations on the power supply lines, FPGA devices require a large number of discrete bypass capacitors as close as possible to the power pins.
  - Requirements for power supply decoupling for CG1657 = (qty: 125 of 0.01uF and qty: 163 of 0.1uF)
- State of Practice places decoupling capacitors on the top and or bottom of the PWA, requiring use of a large area of the board.

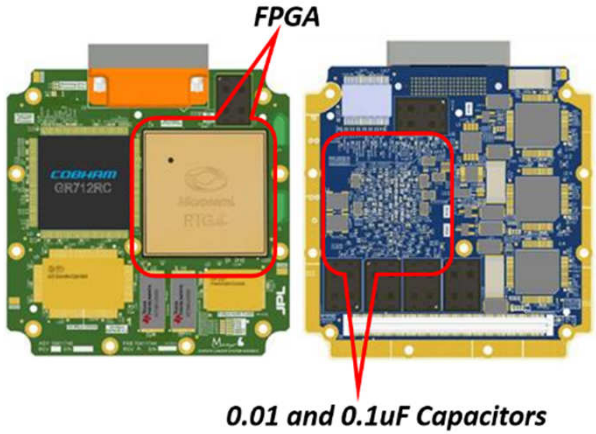

FIGURE 1: Typical SoP implementation of FPGA and bypass capacitors

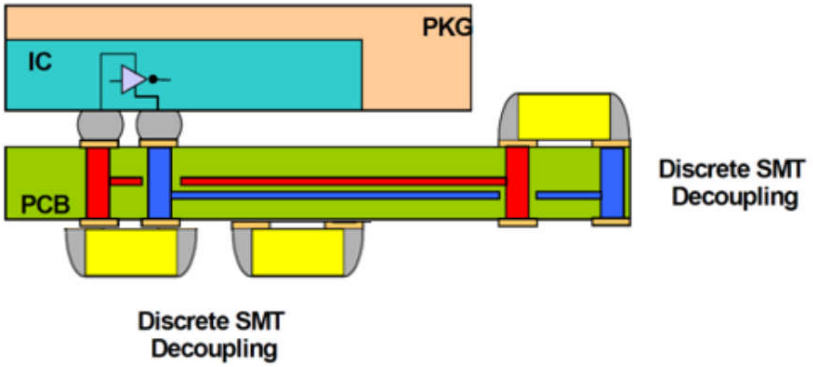

FIGURE 2: Schematic representing State of Practice

- This packaging topology is typical, mass and volume reduction is difficult to achieve.

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Key technology Development

- Goal: implement a SiP themed solution leveraging volume within the FPGA area.
- Solution: leverage foil capacitor technology and design suitable for and driven by the need to leverage PWB area typically used for the Bypass Capacitors.

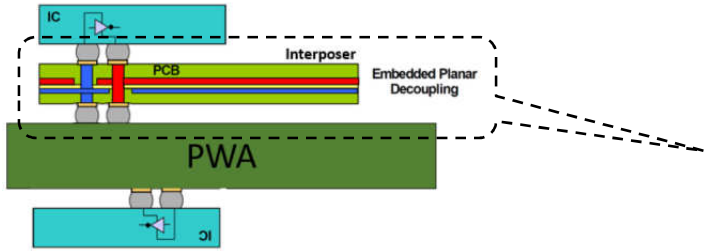
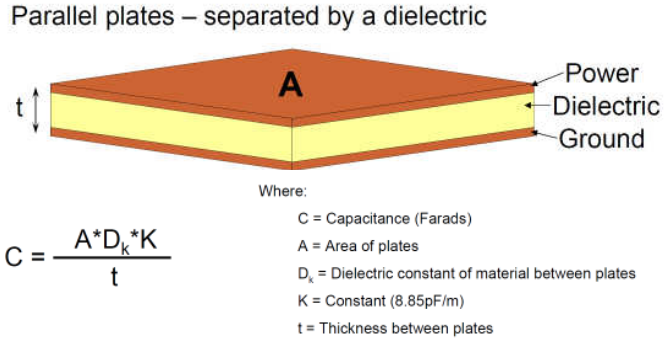


FIGURE 3: Schematic representing SoA using COTS planar-foil technology between the FPGA and PWA, allowing more function to be place behind the FPGA



- The use of planer-foil capacitors technology systems are not new to the industry. Efforts have demonstrated a few hundred Nanofarads of embedded low inductance capacitance can eliminate large number of surface mount decoupling capacitors.
- Three foil manufactures were evaluated: Oak-Mitsui – FaradFlex Technology [3], 3M – Embedded Capacitance Material (ECM) Technology [4] and TDK – Ferroelectric foil Technology [5]. Selection Criteria:
  - Performance: *Capacitance Density and operating voltage.*
  - Cost: *Materials are commercially available / <2 week lead time / <$25/panel (12in x 18in)*
  - Producibility: *Compatible with standard multi-layer PWB processing.*

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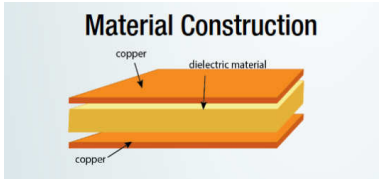
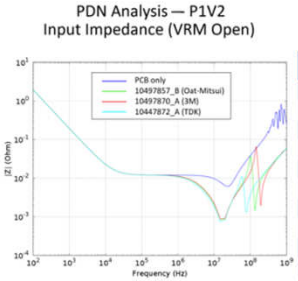
Key technology Development



Three foil manufactures were evaluated:

1. ***Oak-Mitsui*** *– FaradFlex Technology*
2. ***3M*** *– Embedded Capacitance Material (ECM) Technology*
3. ***TDK*** *– Ferroelectric Foil Technology*



Input Impedance (VRM Open)

Impedance (mΩ)

Frequency (MHz)	PCB only	10497857_B (Oat-Mitsui)	10497870_A (3M)	10497872_A (TDK)
0.001	194.37	193.28	193.32	193.09
0.01	22.78	22.69	22.69	22.67
0.1	12.1	12.09	12.09	12.07
1	11.92	11.14	11.2	10.9
10	9.76	2.15	2.23	1.86
20	6.38	0.89	0.91	0.85
40	11.08	3.83	3.78	4.24
60	20.31	7.05	6.58	11.14
80	29.41	13.14	9.86	1.35
100	38.4	37.21	14.54	3.74

Power Density Analysis results, representative of the 1.2V FPGA power pin impedance, analytically showing foil performance for all three capacitive technologies meet motor control performance.

Development Timeline

Motor control system impedances where calculated based on the RTG4 specification for the worst-case power voltages and allowable performance at 24 MHz

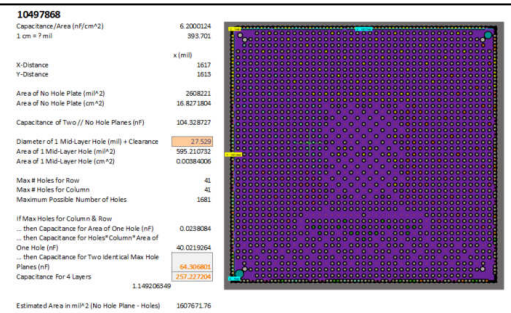
Capacitance / Area was calculated to determine number of layers required for each power-bank voltages

Nominal Dissipation

Name	min(V)	nom(V)	max (V)	Allowable Ripple (%)	Desired Ripple (%)	Supply Current (A)	Target Impedance(Ω)
P1V2	1.14	1.2	1.26	5%	5%	0.7	85.7E-3
P2V5	2.375	2.5	2.625	5%	5%	0.1	1.25
P3V3	3.15	3.3	3.45	5%	5%	0.2	750.0E-3
VDDMEM	2.375	2.5	2.625	5%	5%	0.1	1.25
VDDB12	2.375	2.5	2.625	5%	5%	0.1	1.25
VDDB78	2.375	2.5	2.625	5%	5%	0.1	1.25
P3V3A_PLL	3.15	3.3	3.45	5%	5%	0.01	15

Maximum Dissipation

Name	min(V)	nom(V)	max (V)	Allowable Ripple (%)	Desired Ripple (%)	Supply Current (A)	Target Impedance(Ω)
P1V2	1.14	1.2	1.26	5%	5%	1.34	44.8E-3
P2V5	2.375	2.5	2.625	5%	5%	0.3	416.7E-3
P3V3	3.15	3.3	3.45	5%	5%	1	150.0E-3
VDDMEM	2.375	2.5	2.625	5%	5%	0.3	416.7E-3
VDDB12	2.375	2.5	2.625	5%	5%	0.3	416.7E-3
VDDB78	2.375	2.5	2.625	5%	5%	0.3	416.7E-3
P3V3A_PLL	3.15	3.3	3.45	5%	5%	0.01	15



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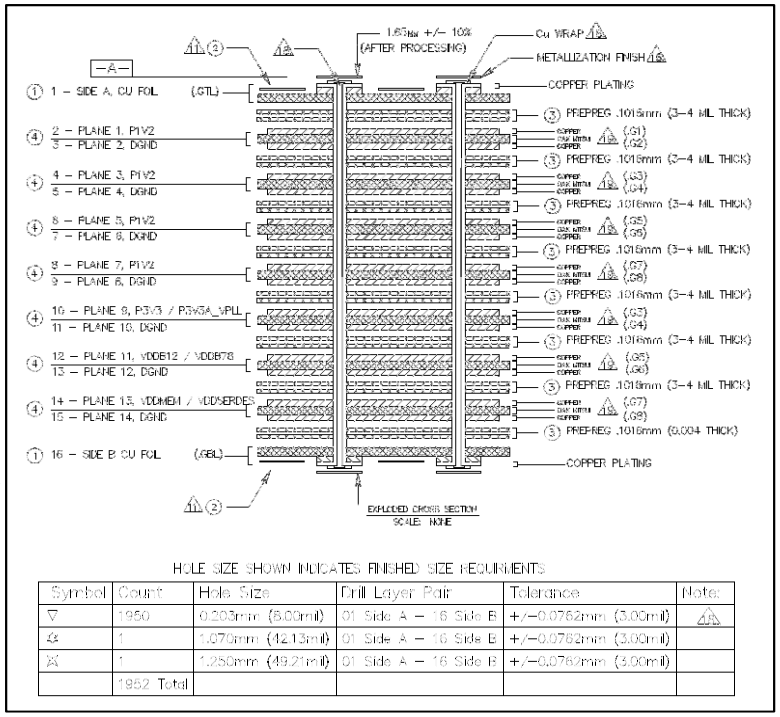
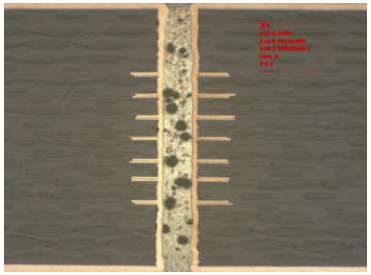
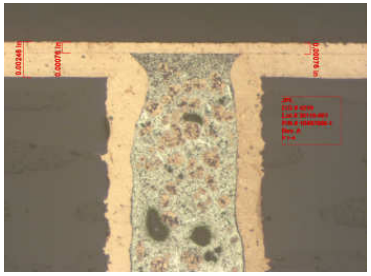
PWB Design

- Leveraging the results of the PDM analysis and capacitance area study, a multiplane stackup was created using four foil layers for the 1.2V plane and one each foil plane layer(s) for the balance of the power-bank voltages.
  - Rigid Polyimide Core for the outer layers per IPC4101/41 and Polyimide Pre-Preg per IPC4101/P41
  - Oak-Mitsui planar-foil was used for all internal plain layers
  - Via-in-Pad design with Tatsuta AE3030 hole-fill, Cu wrap plated and capped.
  - PWB finish metallization – ENEPIG (electroless nickel - palladium / immersion gold) per IPC-4556

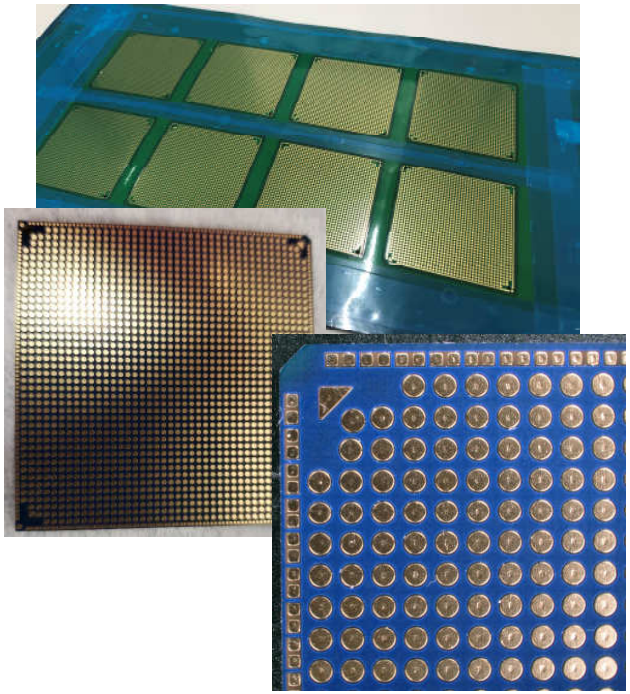




Typical Via
Showing Capacitor *Foils*



Typical Via
Hole-fill and cap



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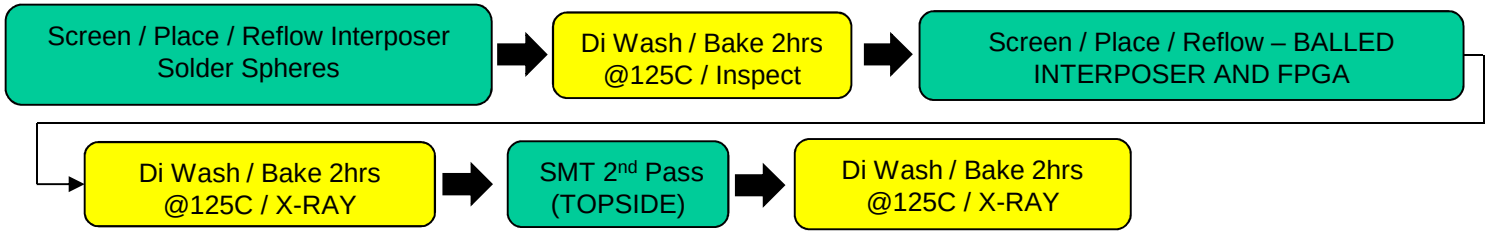
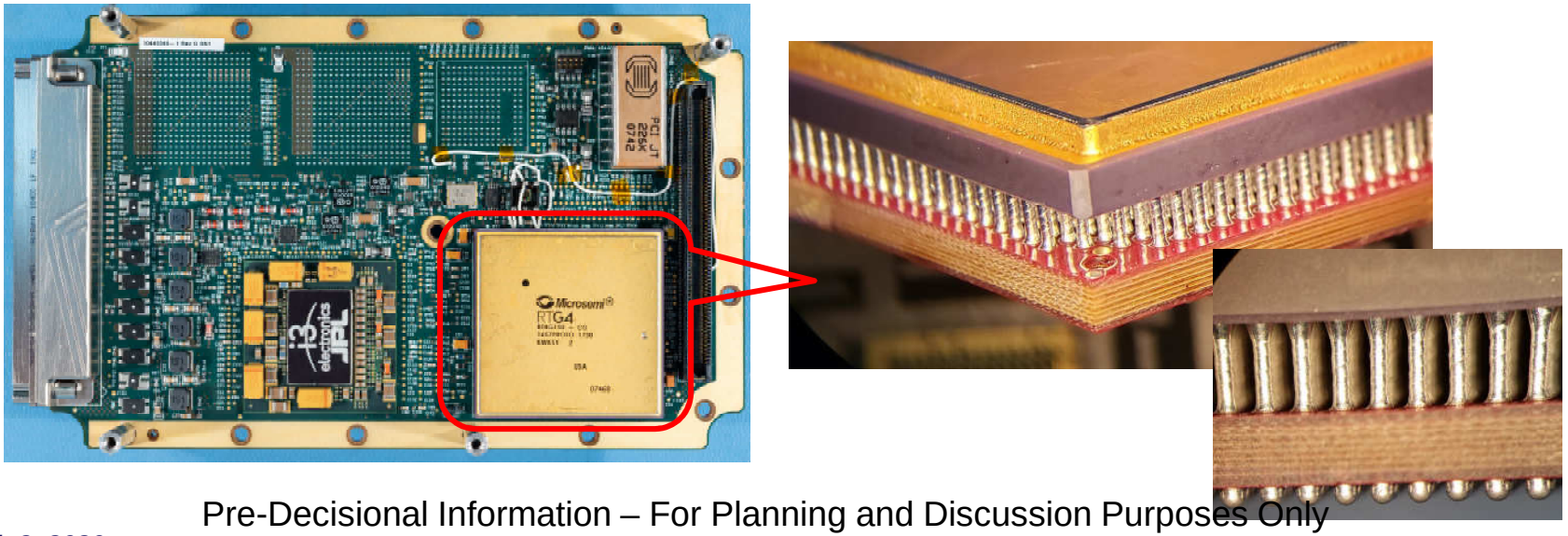
System Integration

- The goal of this Interposer/FPGA SiP solution required a direct infusion into the Europa Lander's Motor Control PWA. This infusion needed to be a repeatable application for any PWA incorporating an FPGA based electronic design.
- Process Flow:





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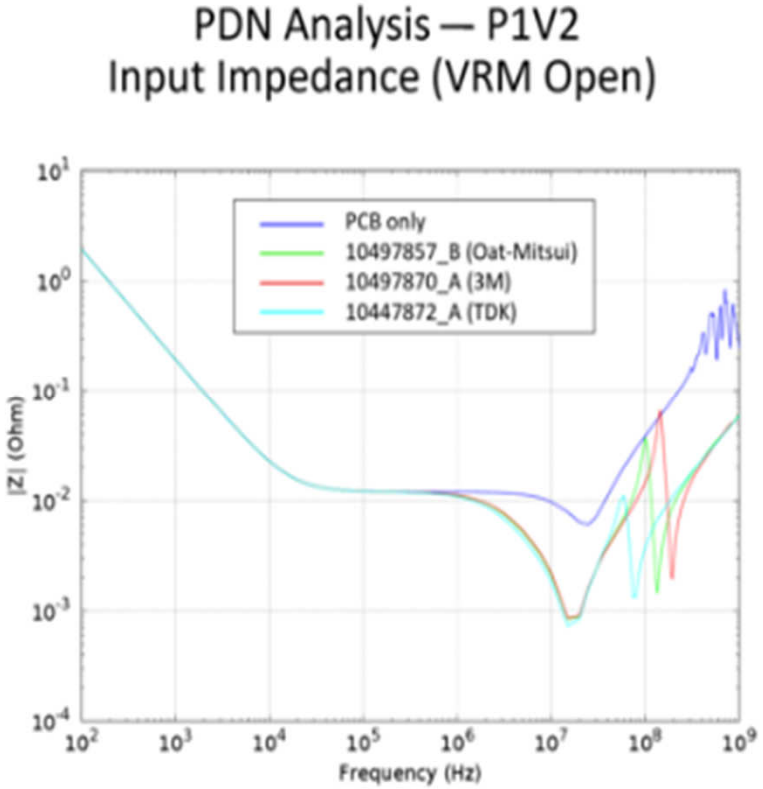
Validation and Analysis

- A power distribution analysis was performed on our Motor Control Card with the three different types of capacitive foils: TDK, Oak-Mitsui and 3M.
- Analysis revealed two solution options:
  - Current Interposer configuration is sufficient for the motor control application.
  - For future applications more capacitance will be needed for the Oak-Mitsui and 3M approaches.



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100	38.4	37.21	14.54	3.74

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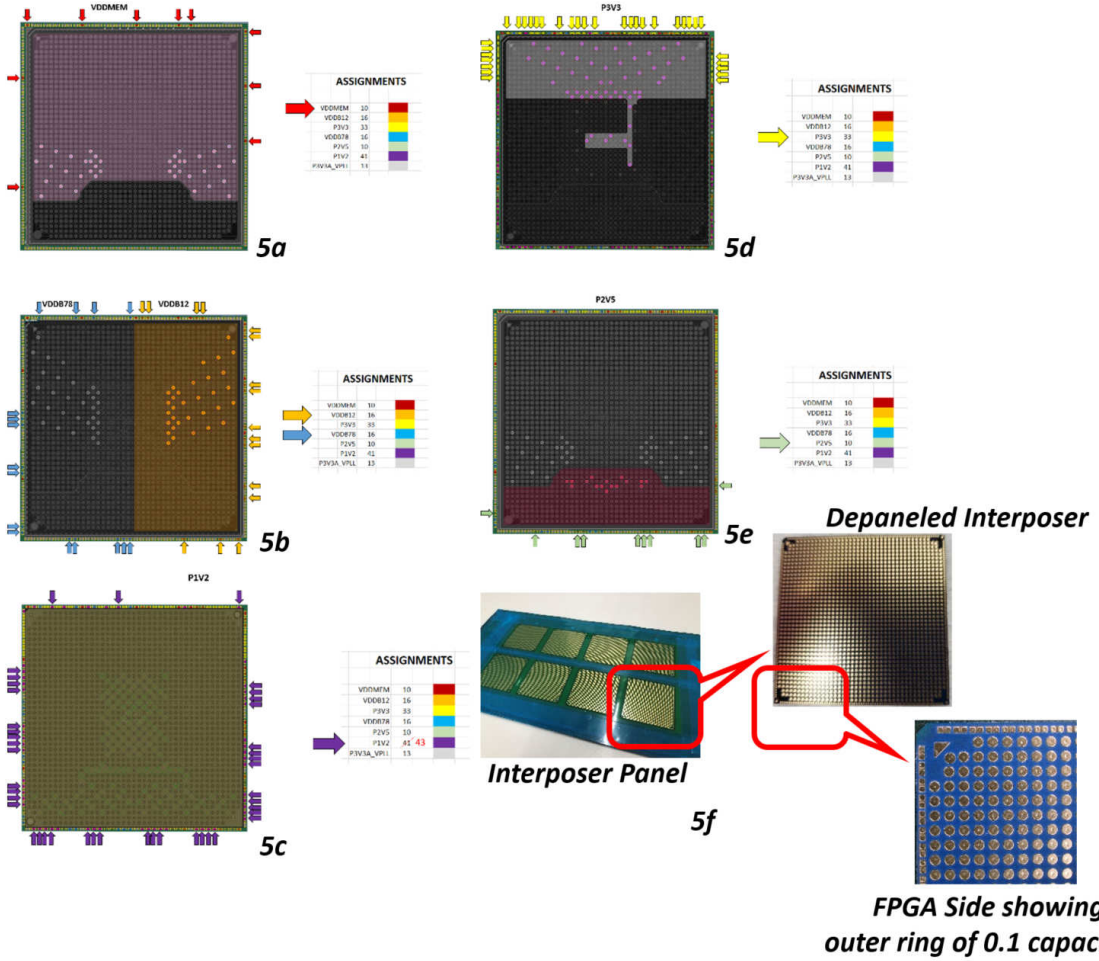
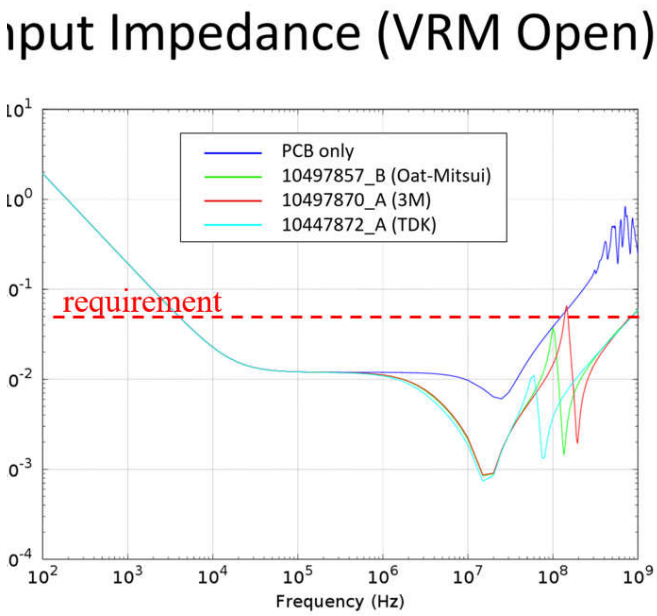
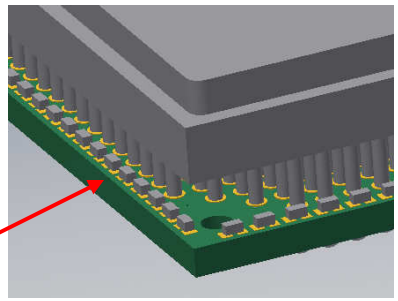
Validation and Analysis

- New PWB design layout showing how the discrete capacitors are connected to a specific voltage power-bank. This solution improved total capacitance capability.







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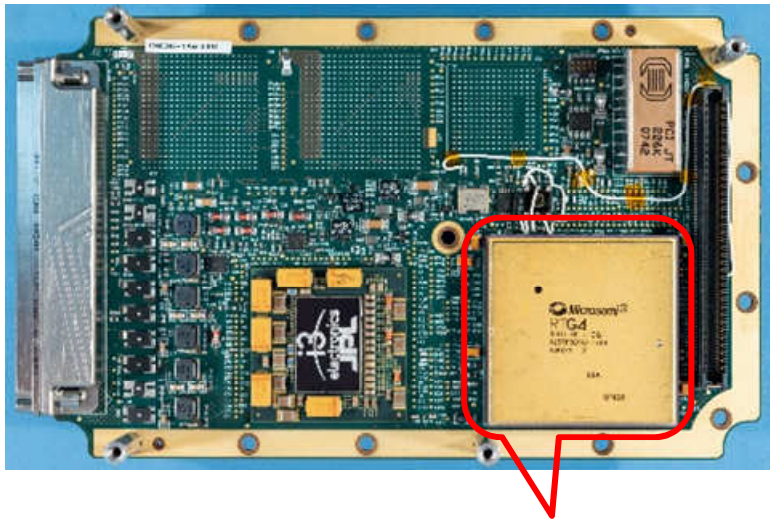
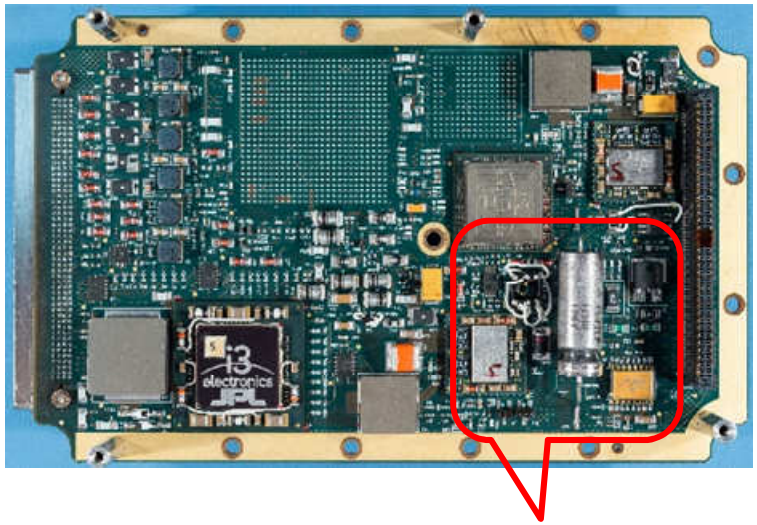
Conclusion

- Key goals have been meet.
- We demonstrated design, fabrication, assembly and testing of a planar-foil Interposer/FPGA SiP technology.
- Met the goals of improved functionality and demonstrated overall reduction in Printed Wiring Board (PWB) area over present state of practice.
- Future functional tests of the Europa Lander Motor Control Assembly will provide confidence that the Interposer/FPGA SiP is ready to be incorporated into future designs.



Interposer/FPGA



Area used for additional circuity

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Acknowledgments

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The author would like to thank the Europa Lander Technology Maturation Management Team for their continued support. Our development Team would also like to thank **Dynamic Design International** for their support with Motor Control PWB and Interposer design and general PWB knowledge. **Aurora–Systems** for their signal and power integrity analysis and consulting support. The **i3 Electronics and the i3 support staff** for their efforts and partnership in this COTS technology infusion. **TDK Corporation - Japan Inc. and U.S. Inc**. and support staff for their custom foil delivery and technical support. **3M Corporation**. **Oak-Mitsui FaradFlex Technologies** for their hands-on technical support and customer service accessibility. **Careertech-US** for their dedicated PWB fabrication and delivery support. All their invaluable contributions added to the success of this task, and we look forward to working with them in the near future.

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Wrap Up and Questions