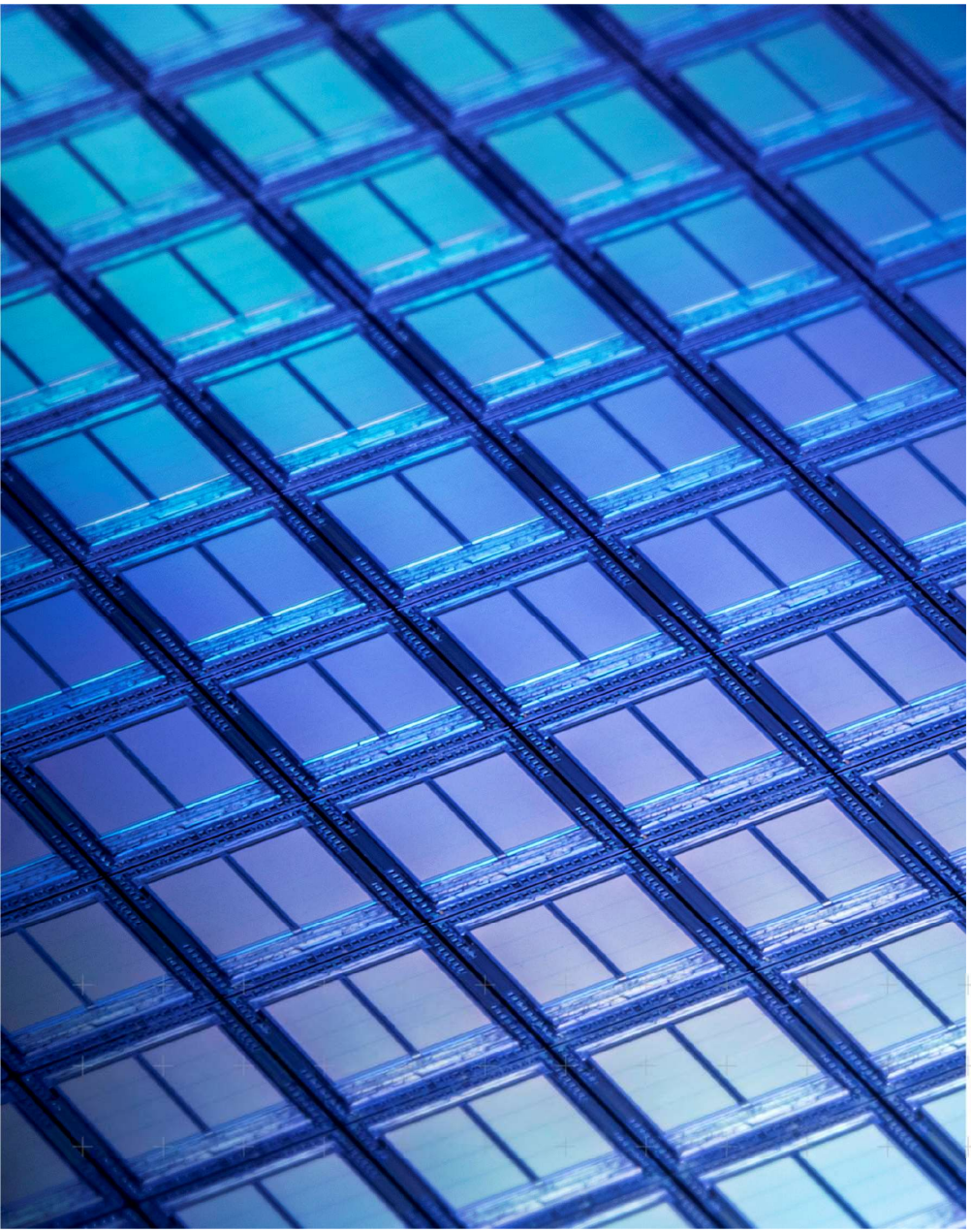

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Through silicon via undercut profile optimisation for 3D packaging applications

Paul Gray – IMAPS Device Packaging

March 3rd 2020

Contents

- What is a Through Silicon Via (TSV)?
- Device packaging
- TSV profiles
- Undercut formation
- Project scope
- Experimental method
- Results
- Conclusions

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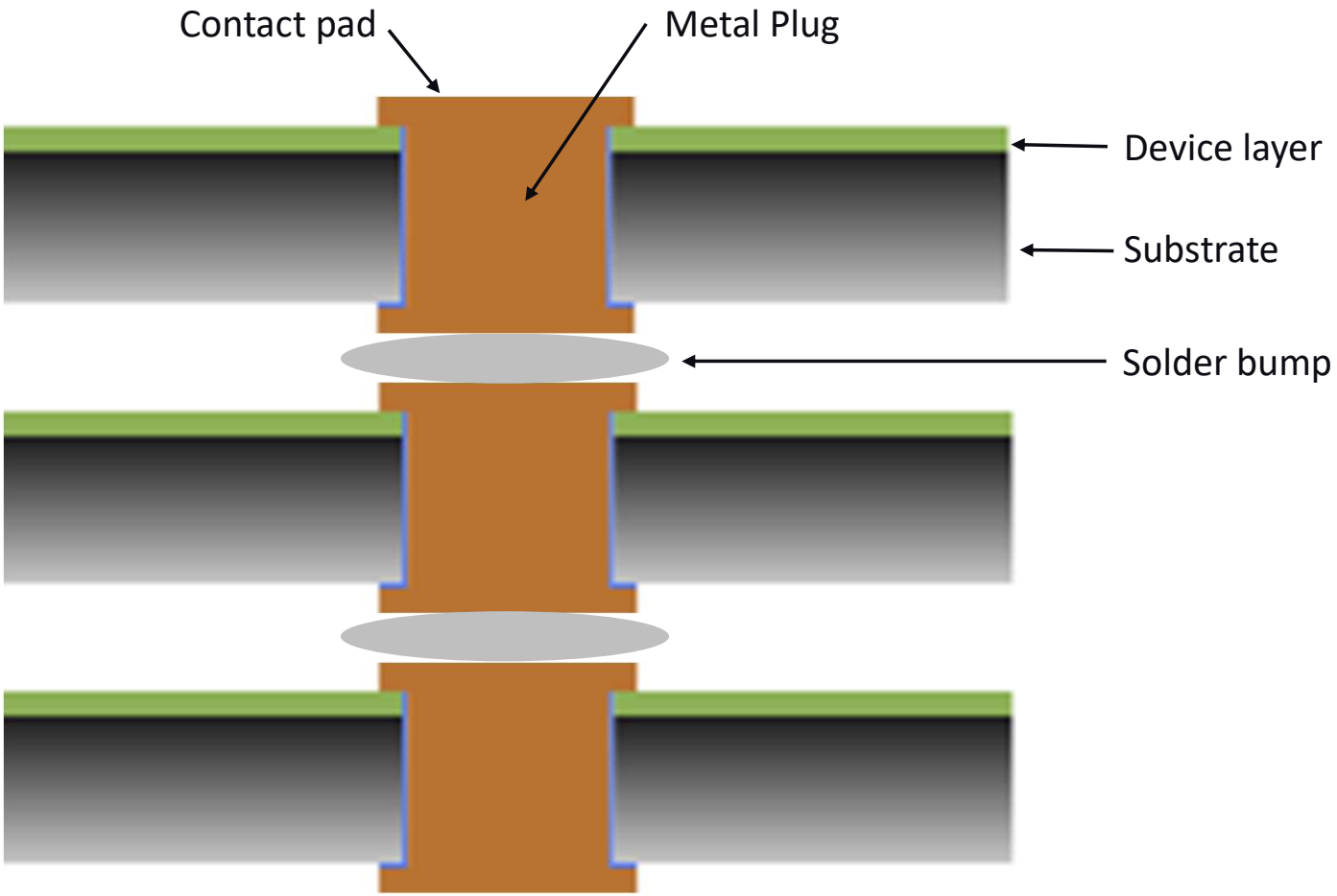
What is a TSV (Through Silicon Via)?



"The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000."

—Gordon Moore; Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, April 19, 1965, pp.114 ff

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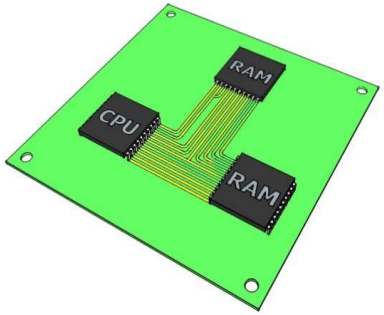
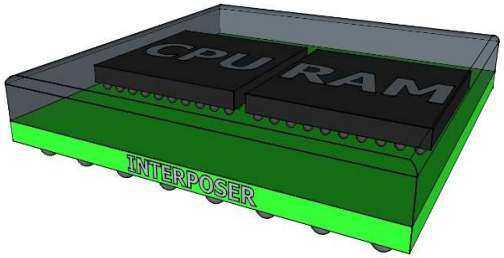
Device Packaging

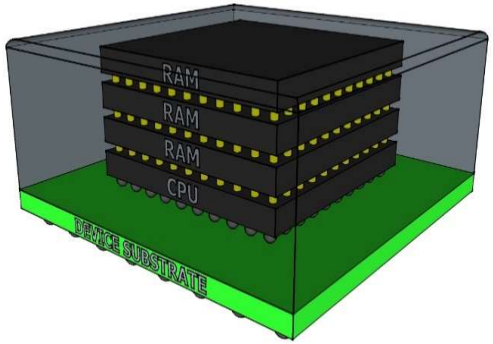
Traditional

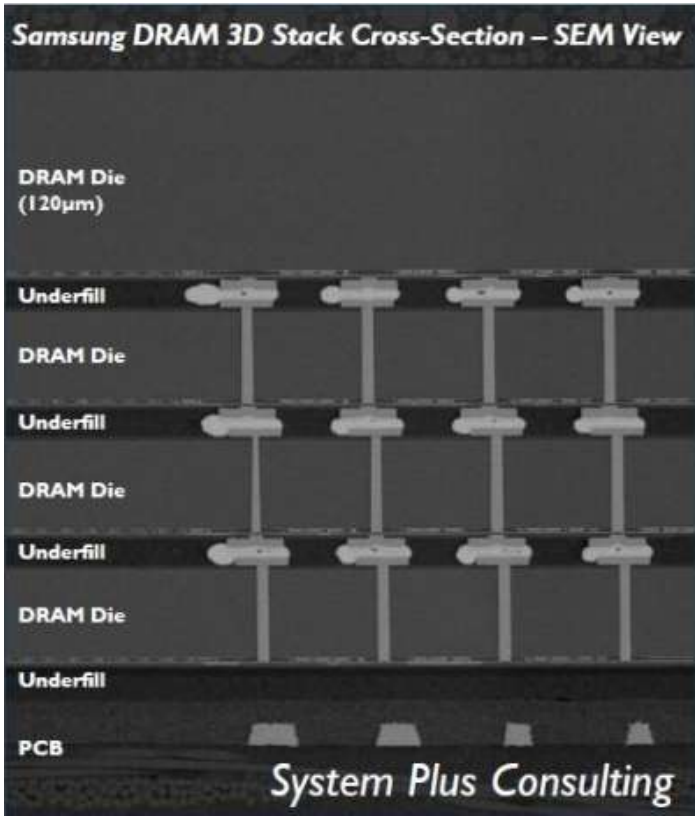


2.5 D with Interposer



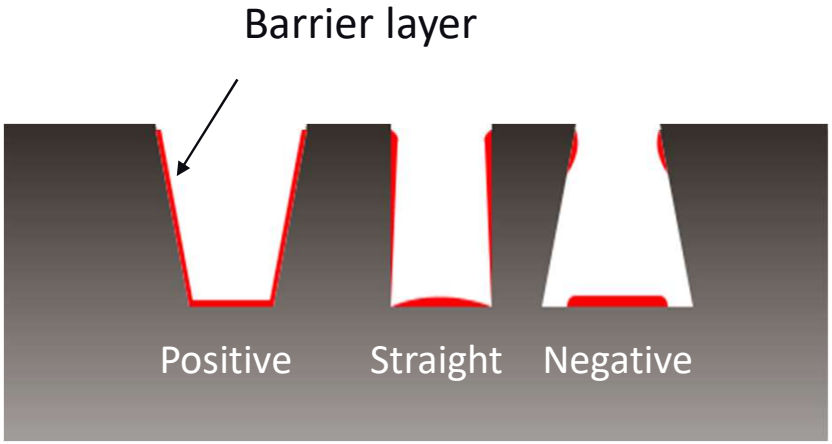
3 D

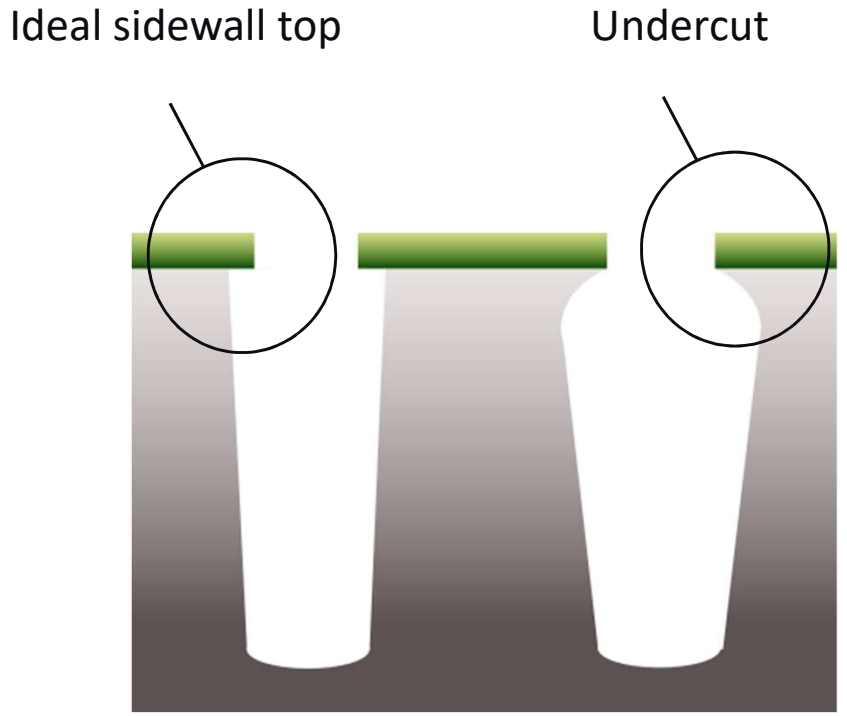




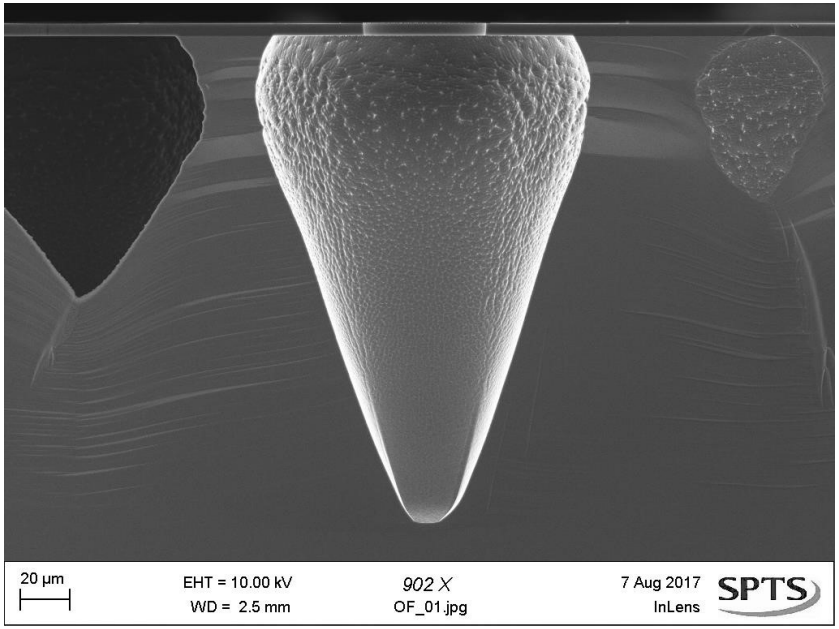
Samsung DDR4 DRAM Memory Stack (Source: Samsung 3D TSV, Stacked DDR4 DRAM report – System Plus Consulting, 2015.)

TSV Profiles





TSV Profiles



Remove mask

- Plasma bulk etch removal or grinding
- Second process is additional cost
- Increases yield, reduces throughput

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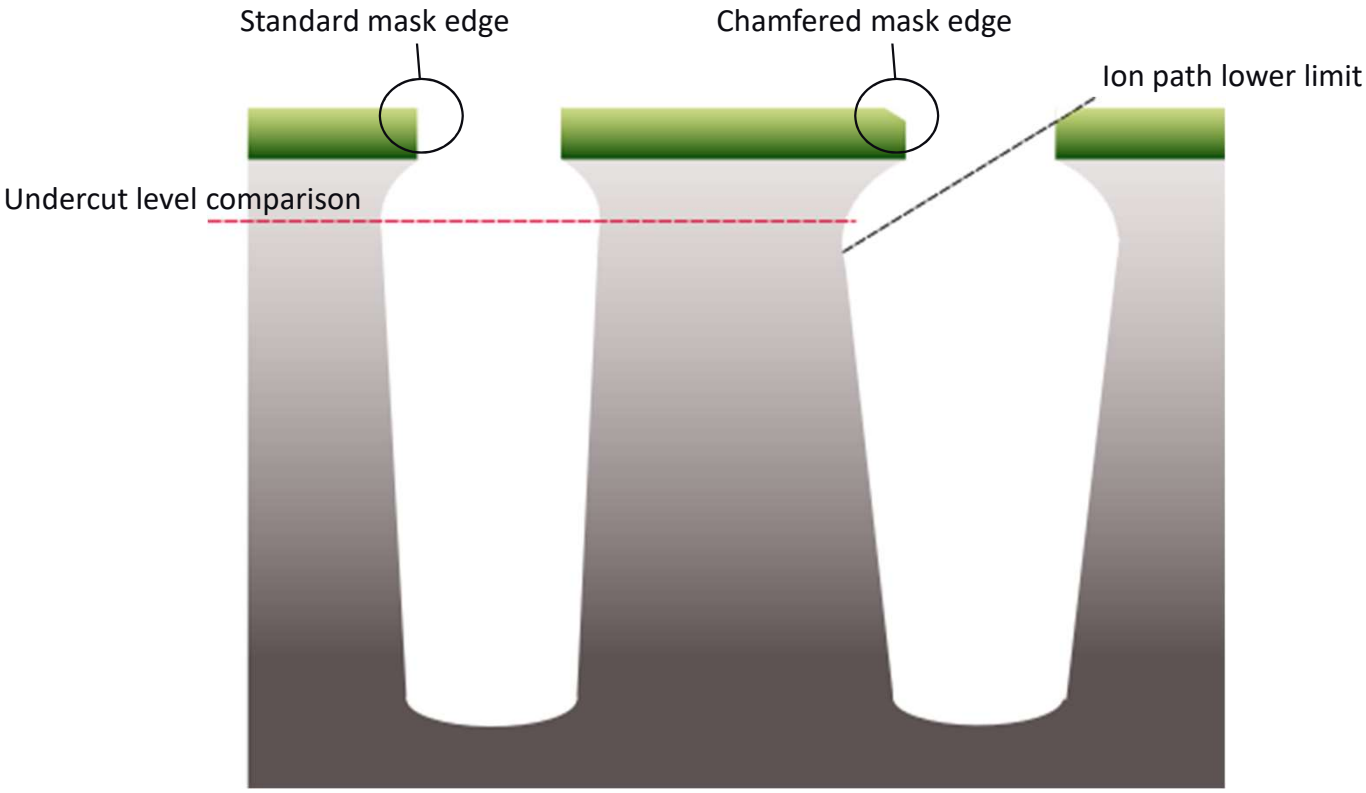
Undercut Formation



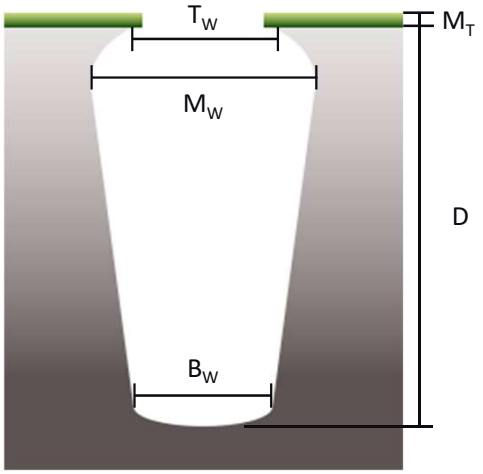
M. Boufnichel 2003, T. Maruyama 2010

- Adjusting O_2/SF_6 ratio produces tapered sidewalls due to lateral etching.
- F radicals preferentially etch the top of the structure.
- Chamfered mask edges enhances the effect by ion scattering

Project Scope

- The purpose of this work was to investigate the combination of process parameters that affect the dimensions of the ‘undercut’, and improve centre to edge uniformity.
- The ideal outcome would be a set of parameters that would allow an engineer to manipulate undercut formation.
- A single step O_2/SF_6 recipe was used (i.e. non-switched), as it is one of the standard process chemistries used to manufacture this type of feature.
- 150mm test wafer with a 3.28% open area.

Experimental Method



Recipe Setting	*Parameter Value*
Process Time	15'00"
Process Pressure	90mTorr
SF_6	156 sccm
O_2	80 sccm
Ar	42.5 sccm
Coil Power	3.35 kW
Platen Power	135 W (13.56 MHz)
Platen Temperature	20°C
Helium Backside Pressure	10Torr

- DoE run using an L16 (4^5) Taguchi Array.
- Each parameter tested had four data points that were equally divided across the range.
- All process runs performed on an SPTS Pegasus™ DRIE.
- Parameters in red/green identified as being most likely to alter the undercut dimensions
- Ratio between gasses was fixed, only total gas flow changed.

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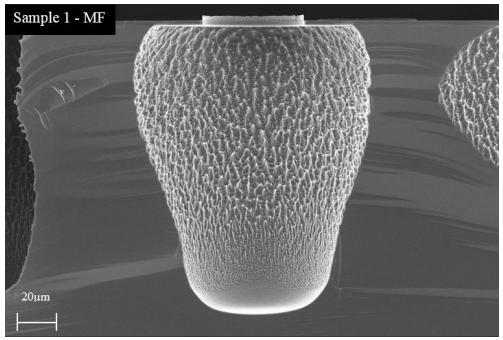
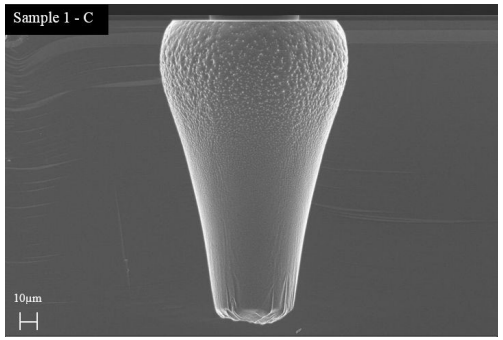
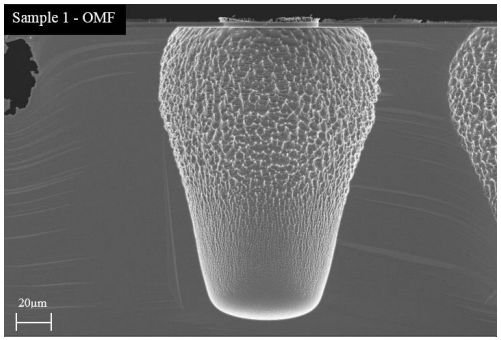
Variation Between Process Runs

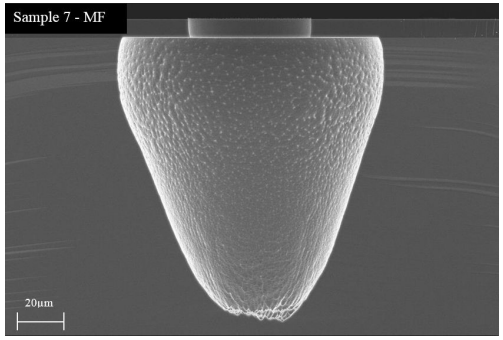
MF Edge | Centre | OMF Edge

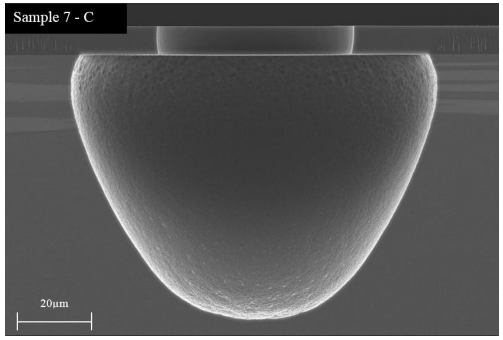


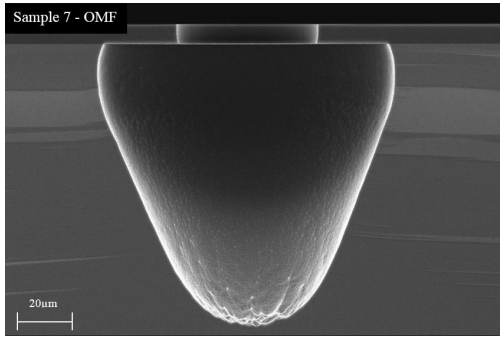




Sample 1 (base process)







Sample 7

Pictures not to scale

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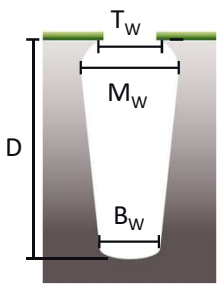
Results



	Process Pressure ↑	Total Gas Flow ↑	Platen Temperature ↑	Coil RF Power ↑	Platen RF Power ↑	Platen RF Power ↓
Depth C	↓↓	↑↑				
Depth MF	↑					
Depth Uni	↑↑					
TW C		↑↑				
TW MF	↑	↑↑				
TW OMF	↑	↑↑				
TW Uni	↑	↑↑	↓↓			↓
MW C		↑↑				
MW MF		↑↑				
MW OMF		↑↑				
MW Uni	↑↑	↑↑	↓↓			
BW MF	↓↓	↑↑			↑↑	
BW OMF	↓↓	↑↑		↑	↑↑	

- Table shows all relationships that have a p-value of less than ≤0.05 which are statistically significant
- Double arrows show a large effect, single arrows a small effect
- The results show that there is no definite trend within the scope of this work that would allow a user to solely manipulate the undercut dimensions.

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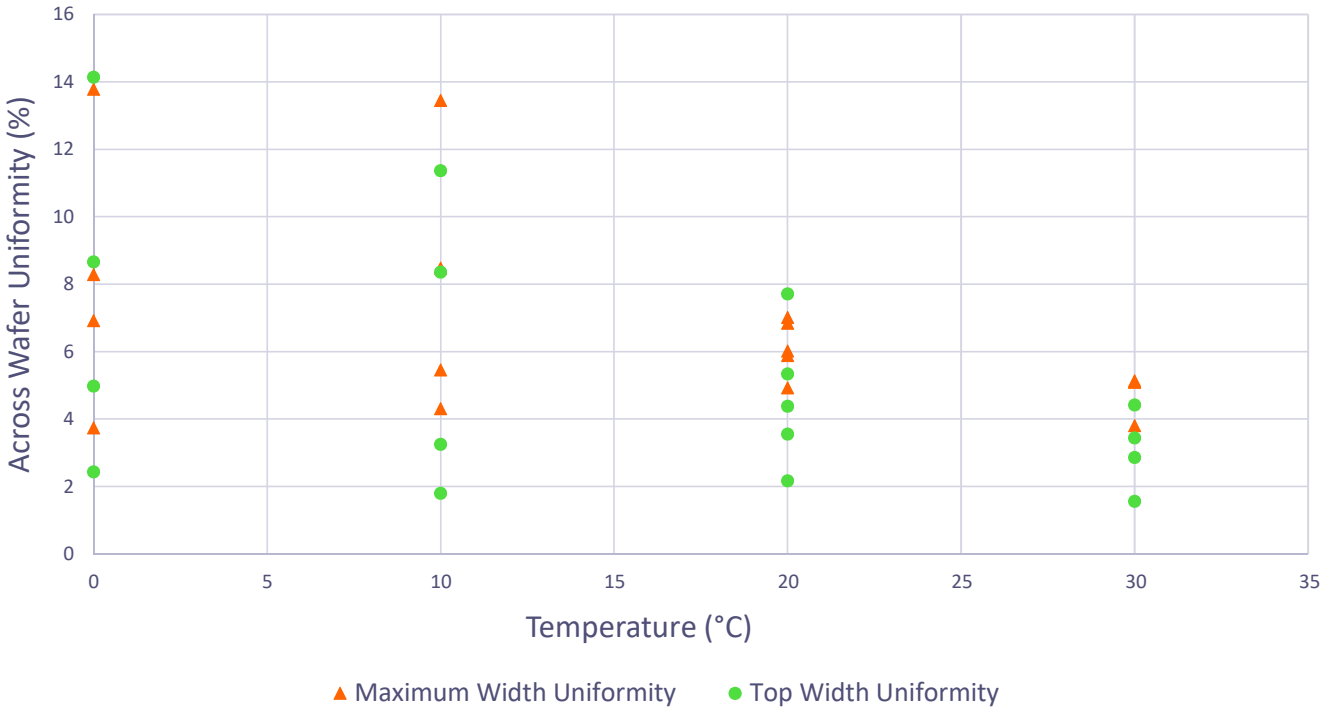
Across Wafer Non-Uniformity

$\overline{x}$ = 7.86% $\overline{x}$ = 7.05% $\overline{x}$ = 5.38% $\overline{x}$ = 3.92%



- Across wafer non-uniformity is improving by ~ 1% per 5°C of platen temperature rise within the range tested.
- The effect is unlikely to continue indefinitely.
- Uniformity is an important metric as it will directly drive yield increases and will enable predictable additional manufacturing steps.

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What is causing this effect?

- Passivation of the substrate surface is dependent upon its temperature, as temperature increases passivation rate lowers thus raising the etch rate.
- Increased etch rate should be observed, but counterintuitively the vertical etch rate reduces.
- Etch rate increases across the entire exposed surface, as the volume of silicon being etched increases more species is consumed out of the chamber environment.
- This effect homogenises the etch across the whole wafer resulting in a more uniform consumption of silicon improving uniformity

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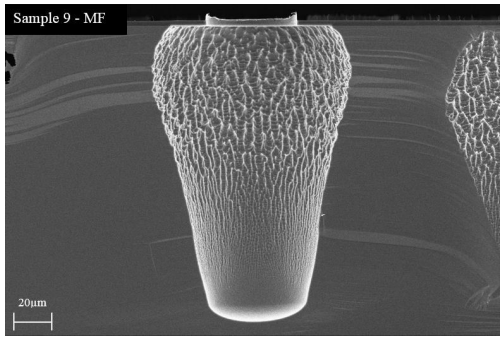
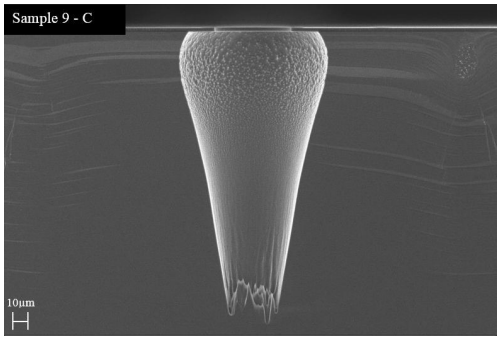
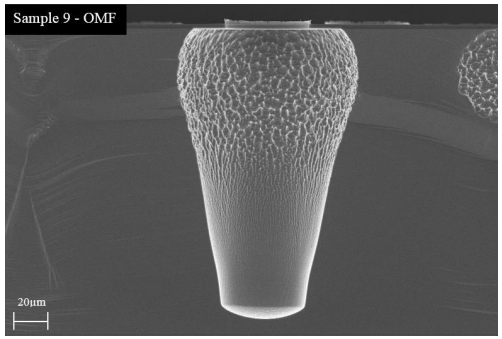
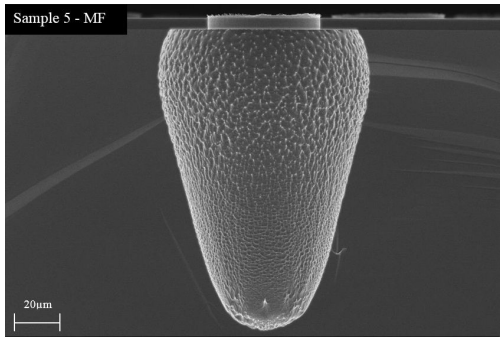
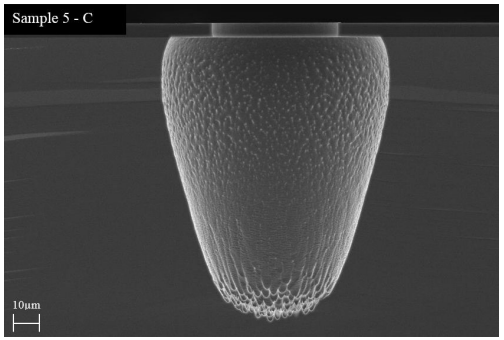
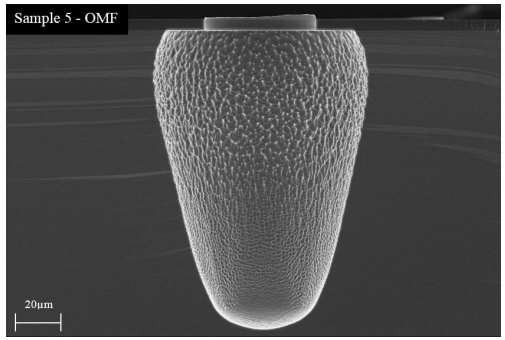
Profile Uniformity

MF Edge	Centre	OMF Edge	
			Sample 9 (0°C)
			Sample 5 (30°C)

Pictures not to scale

Summary

- A single step O_2/SF_6 process has a fine balance, any changes to the process conditions can have unintended consequences
- Increasing the platen temperature within the range 10 to 30°C has the effect of improving uniformity at ~1% per 5 °C.
- This effect has been confirmed to work on a SPTS 200mm Rapier™ DRIE.
- Future work would apply the results to identify if further optimisation could be achieved with additional mask or parameter changes.