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Heterogeneous System-in-Package (HSIP) Using Fan-Out Wafer-Level Packaging (FOWLP)

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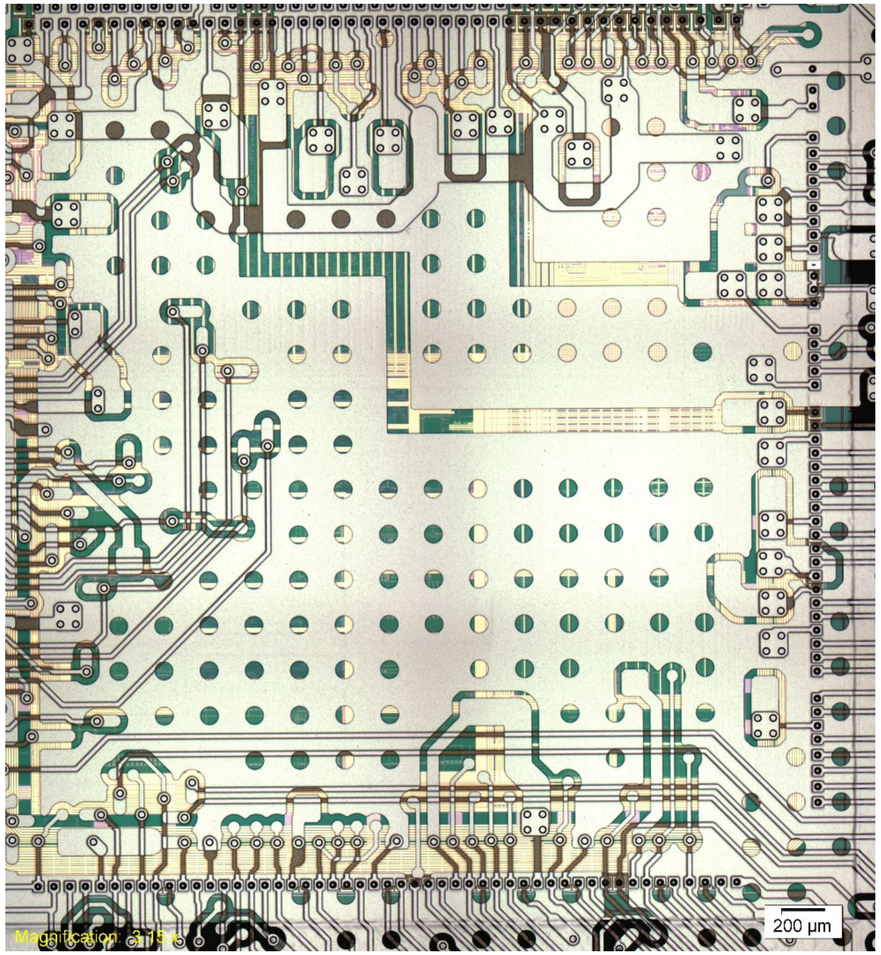

Typical Routing Layer in HSIP Technology

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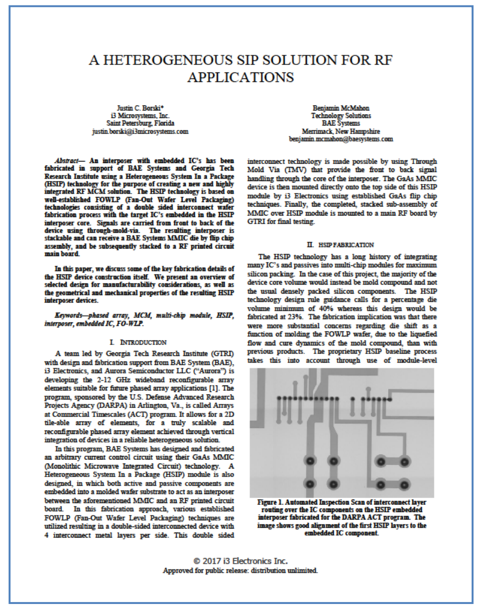
DARPA ACT Project Overview

- DARPA ACT TA2 Program (Arrays at Commercial Timescales)
- System architecture which allows a 2D tile-able array of elements, for scalable and reconfigurable phased array that is achieved through vertical integration of heterogeneous devices
- Contract # HR0011-14-C-0056
- Prime: Georgia Tech Research Institute
- Sub: BAE Systems
- **Sub: i3 Microsystems**



A HETEROGENEOUS SIP SOLUTION FOR RF APPLICATIONS

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***Abstract*— An interposer with embedded IC's has been fabricated in support of BAE Systems and Georgia Tech Research Institute using a Heterogeneous System In a Package (HSIP) technology for the purpose of creating a new and highly integrated RF MCM solution. The HSIP technology is based on well-established FOWLP (Fan-Out Wafer Level Packaging) technologies consisting of a double sided interconnect wafer fabrication process with the target IC's embedded in the HSIP interposer core. Signals are carried from front to back of the device using through-mold-via. The resulting interposer is stackable and can receive a BAE Systems MMIC die by flip chip assembly, and be subsequently stacked to a RF printed circuit main board.**

In this paper, we discuss some of the key fabrication details of the HSIP device construction itself. We present an overview of selected design for manufacturability considerations, as well as the geometrical and mechanical properties of the resulting HSIP interposer devices.

Keywords—phased array, MCM, multi-chip module, HSIP, interposer, embedded IC, FO-WLP.

I. INTRODUCTION

A team led by Georgia Tech Research Institute (GTRI) with design and fabrication support from BAE System (BAE), i3 Electronics, and Aurora Semiconductor LLC ("Aurora") is developing the 2-12 GHz wideband reconfigurable array elements suitable for future phased array applications [1]. The program, sponsored by the U.S. Defense Advanced Research Projects Agency (DARPA) in Arlington, Va., is called Arrays at Commercial Timescales (ACT) program. It allows for a 2D tile-able array of elements, for a truly scalable and reconfigurable phased array element achieved through vertical integration of devices in a reliable heterogeneous solution.

In this program, BAE Systems has designed and fabricated an arbitrary current control circuit using their GaAs MMIC (Monolithic Microwave Integrated Circuit) technology. A Heterogeneous System In a Package (HSIP) module is also designed, in which both active and passive components are embedded into a molded wafer substrate to act as an interposer between the aforementioned MMIC and an RF printed circuit board. In this fabrication approach, various established FOWLP (Fan-Out Wafer Level Packaging) techniques are utilized resulting in a double-sided interconnected device with 4 interconnect metal layers per side. This double sided interconnect technology is made possible by using Through Mold Via (TMV) that provide the front to back signal handling through the core of the interposer. The GaAs MMIC device is then mounted directly onto the top side of this HSIP module by i3 Electronics using established GaAs flip chip techniques. Finally, the completed, stacked sub-assembly of MMIC over HSIP module is mounted to a main RF board by GTRI for final testing.

II. HSIP FABRICATION

The HSIP technology has a long history of integrating many IC's and passives into multi-chip modules for maximum silicon packing. In the case of this project, the majority of the device core volume would instead be mold compound and not the usual densely packed silicon components. The HSIP technology design rule guidance calls for a percentage die volume minimum of 40% whereas this design would be fabricated at 23%. The fabrication implication was that there were more substantial concerns regarding die shift as a function of molding the FOWLP wafer, due to the liquefied flow and cure dynamics of the mold compound, than with previous products. The proprietary HSIP baseline process takes this into account through use of module-level

Figure 1. Automated Inspection Scan of interconnect layer routing over the IC components on the HSIP embedded interposer fabricated for the DARPA ACT program. The image shows good alignment of the first HSIP layers to the embedded IC component.

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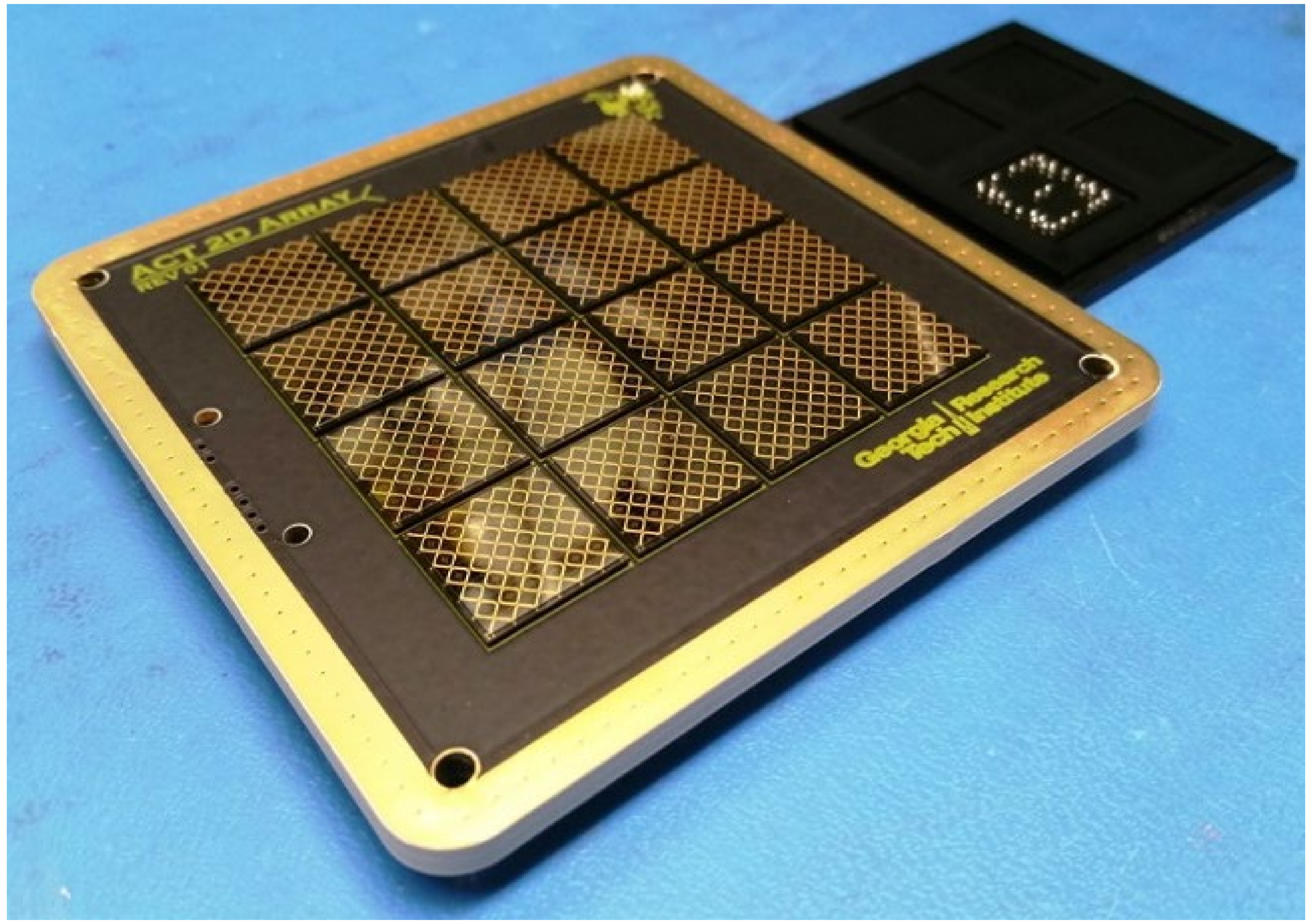

Image courtesy of Georgia Tech Research Institute, 2017

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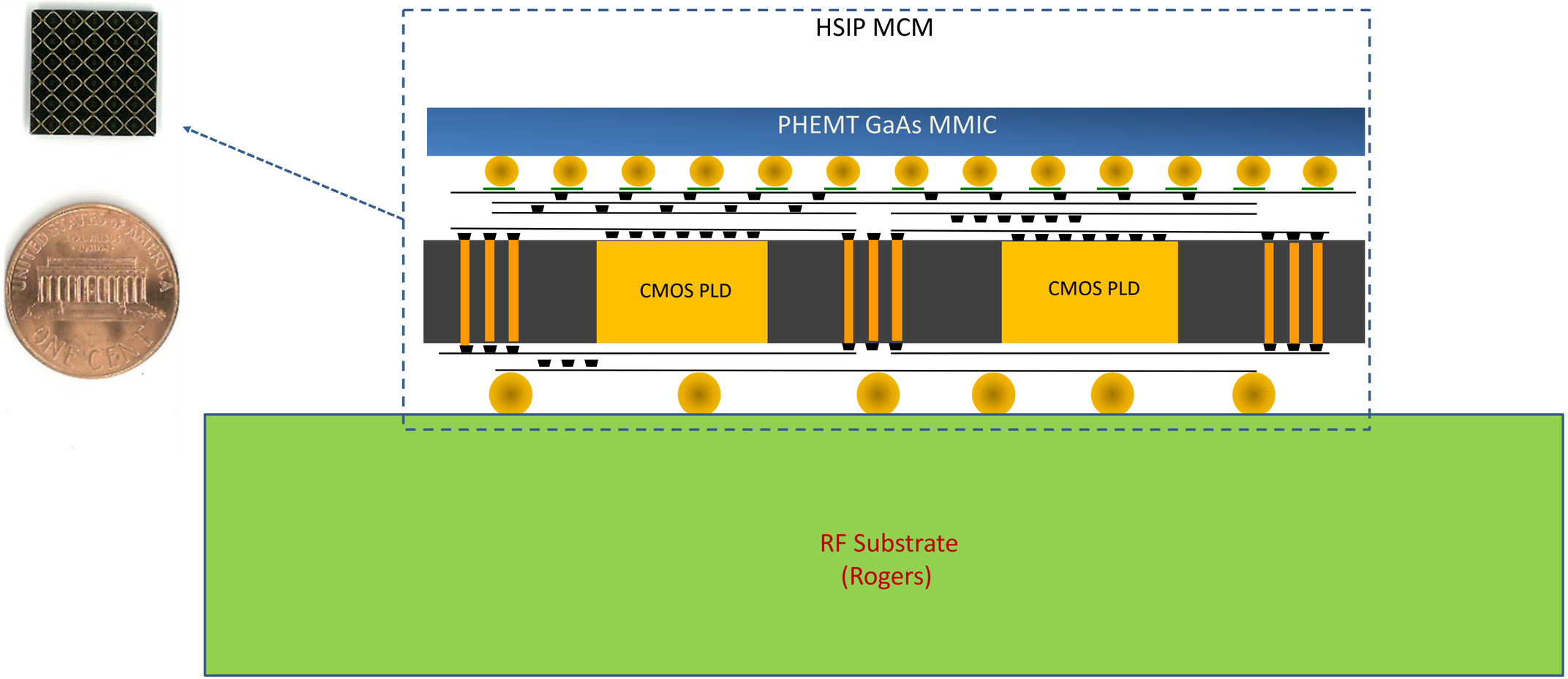
DARPA ACT Project Overview



Images courtesy of BAE Systems, 2018

i3 Microsystems

i3 Microsystems Overview

- Organizational History
  - Operation purchased by i3 Electronics in January 2018
  - Formerly operated as Aurora Semiconductor LLC since of 2016
  - Facility started up and operated by Draper Laboratory since 2009
  - ITAR Certified
  - DMEA Accredited Trusted Foundry
  - ISO-9000:2015 Certified

Our Class-100 Cleanrooms are located in Saint Petersburg, Florida

i3 Microsystems Overview

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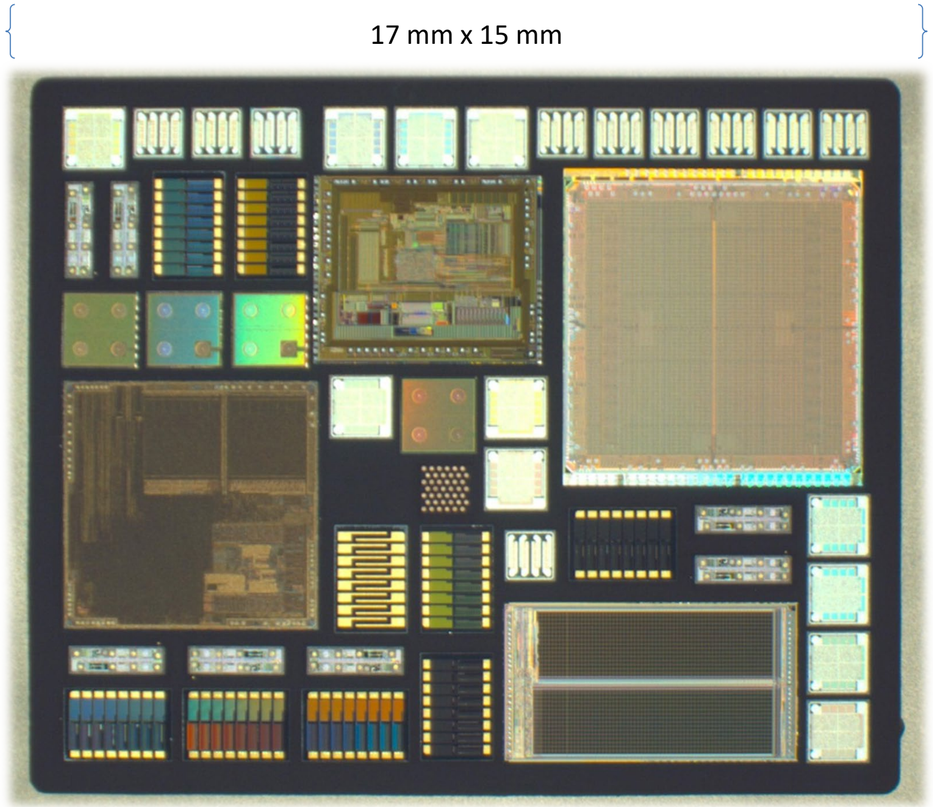
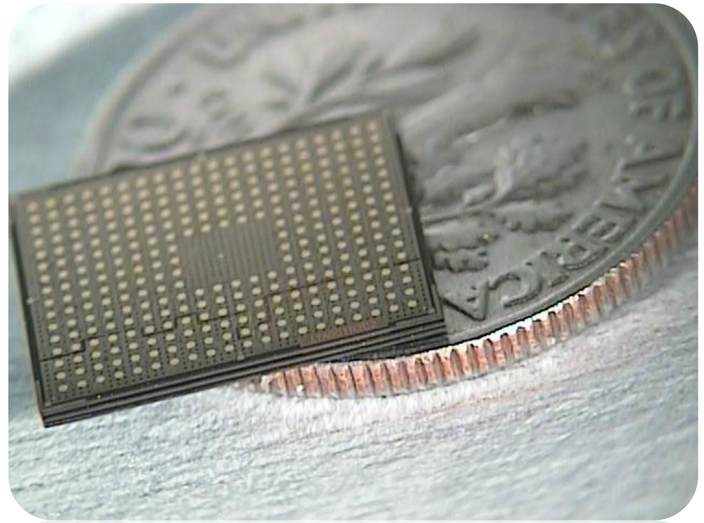
- Organizational History
  - Our HSIP is an embedded-IC interposer solution for the high-reliability DOD and Intelligence Community product spaces
  - Our technology is being deployed into a rated program and is currently fielded for special programs the past 5 years



Typical highly-integrated digital HSIP module containing heterogeneous components

HSIP Benefits

- HSIP Benefits
  - Potential to connect all device technologies – MEMs, sensors, memory, analog, controllers etc.; and all source substrates: Si, GaAs, InP, glass devices – into one package
  - Uses TMV (Thru Mold Via) with no wire bonds or separate interposers
  - Up to 7 interconnect metal layers per side
  - Able to be brought out to BGA or SMT interfaces on both sides



Stacked HSIP Module
24 Total Metal Layers
Double-Sided BGA Interface

HSIP Benefits

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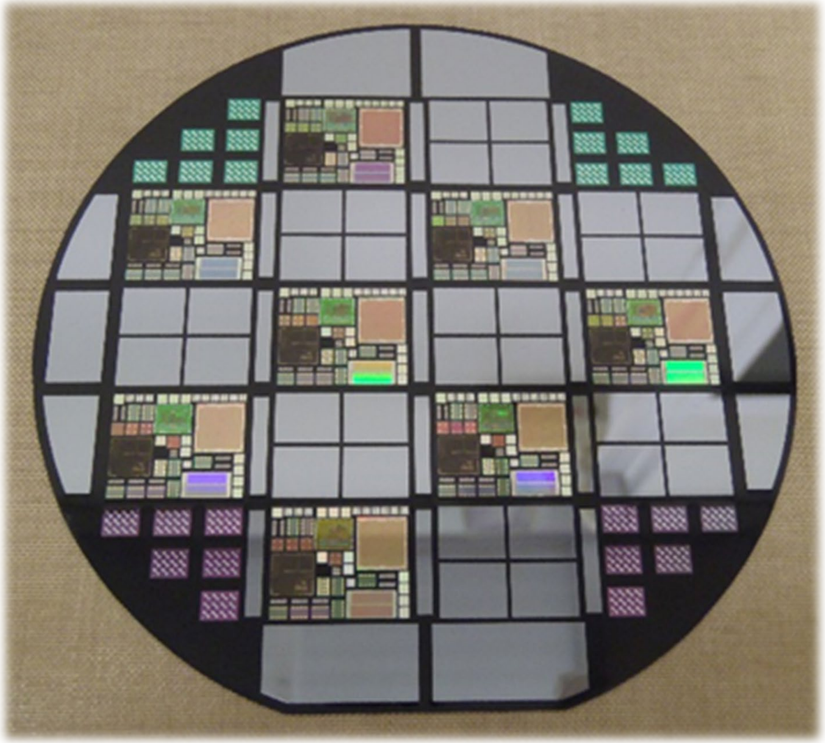
- HSIP Benefits
  - Stacks as a subsystem – up to three slices
  - Scalable to larger wafer formats for volume production demands
  - Can incorporate extracted/recovered die for faster prototyping and lower volume orders
  - Has been developed clandestinely by Draper Laboratory for DoD applications, and is now available under license for wider DoD, commercial, or industrial uses



HSIP Project Wafer, ready for our FO-WLP processing (note depopulated modules)

i3 Microsystems Overview

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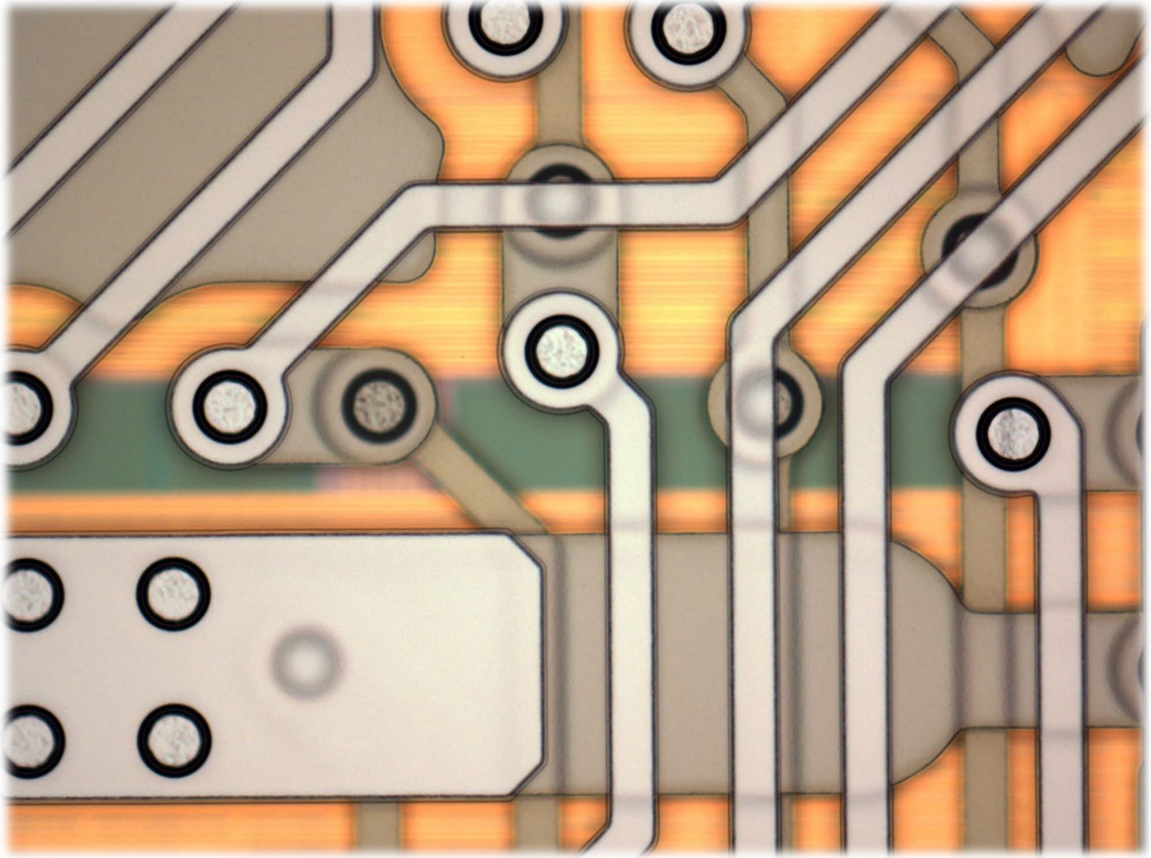
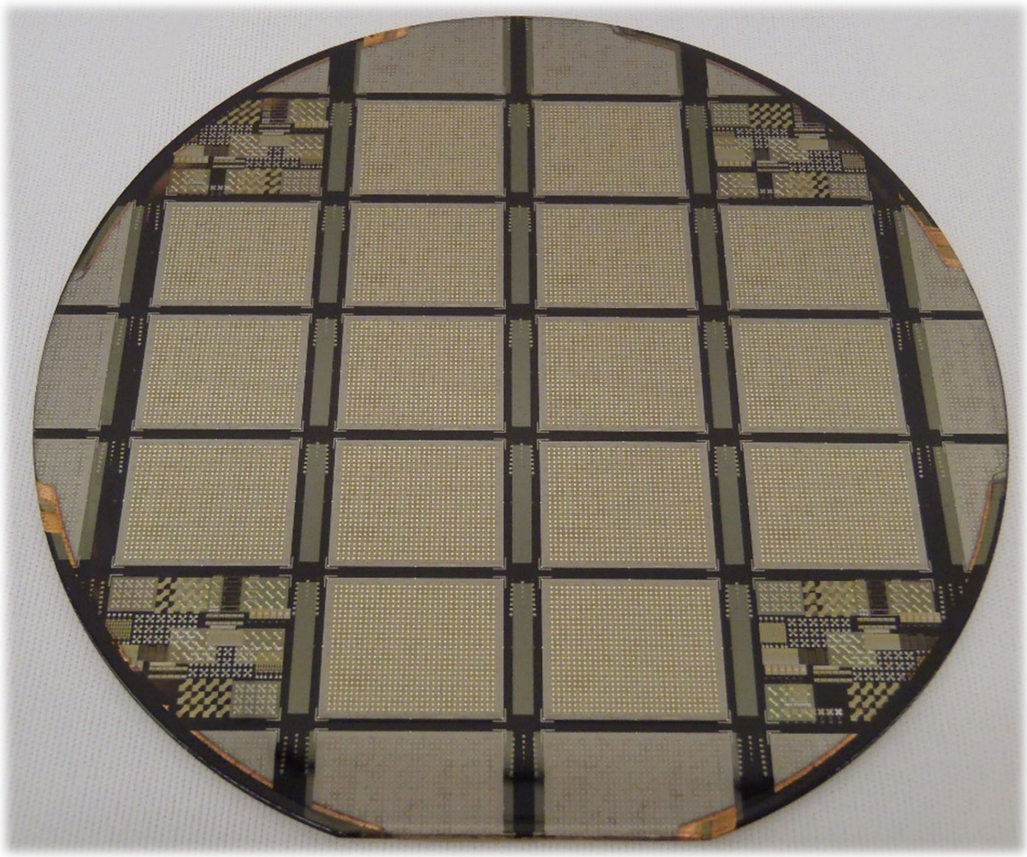


Example of HSIP interconnect routing layers with nominal 18-micron lines, 25-micron via. The image is showing three routing layers.



Typical completed HSIP wafer after 12 metal layers. 7 layers frontside, 5 layers backside.

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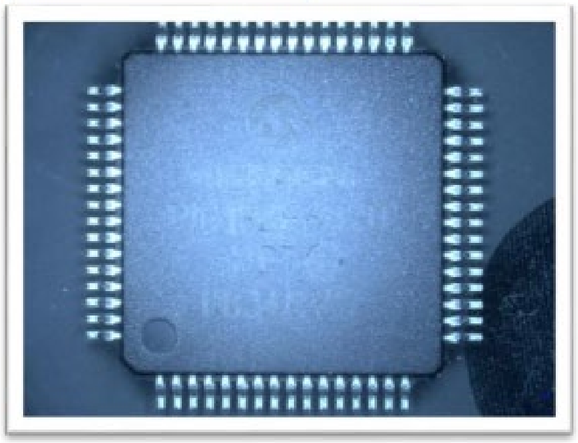
- Die Harvesting – Die Extraction & Recovery (DER) Services

From This



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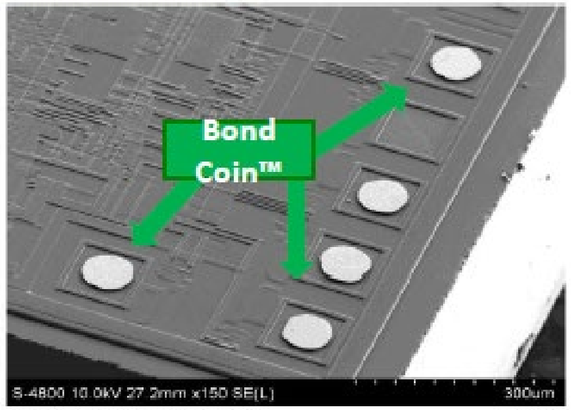
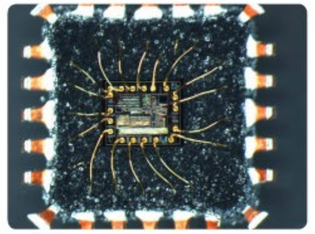
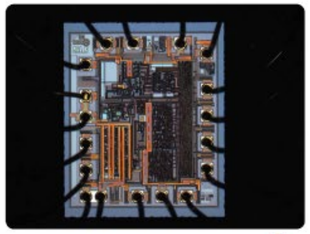


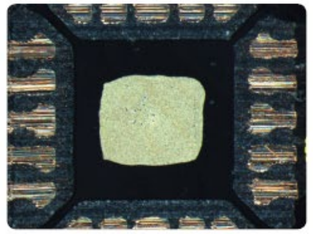
See Air Force SBIR Number AF171-121 for more information



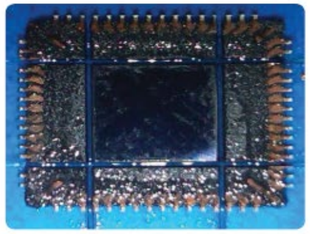


Initial Engineering Investigation / NRE

Back-Side Grind

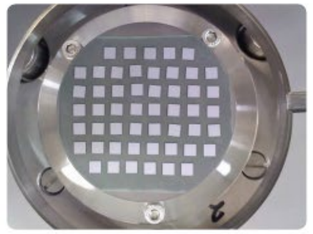


Die Pan Removal

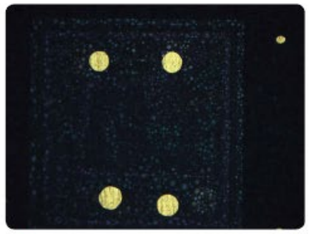


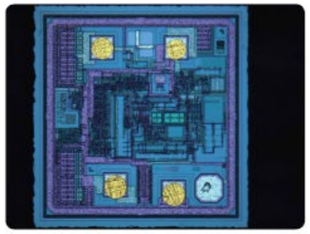
Dice to Precise Dimensions

Front-Side Grind & Diamond Lap



Back-Side Die Thinning





De-Encapsulation Etch Process

HSIP Reliability Baseline

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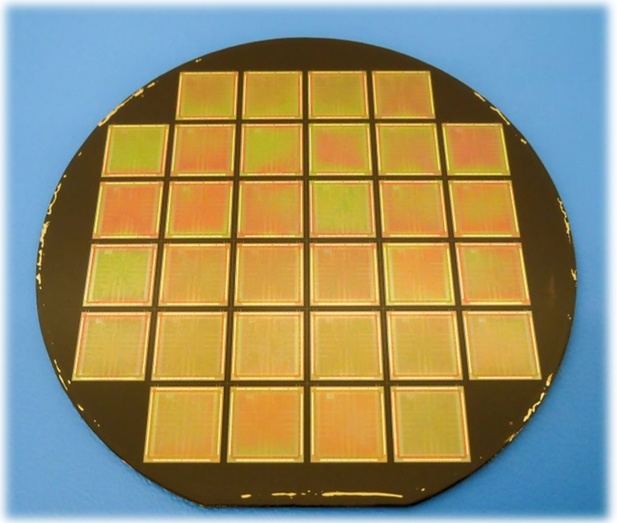
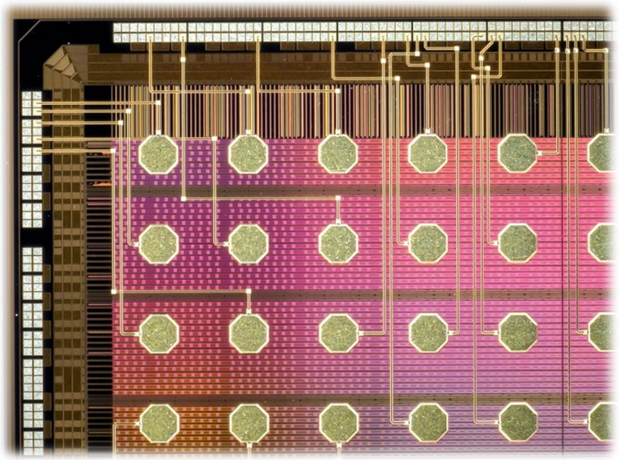
- HSIP Reliability Baseline
  - Over the past 7 years, hundreds of HSIP modules have been shipped on multiple special government projects, with zero field returns for reliability reasons.
  - Testing to-date typically done by our customer partners.
  - HSIP also capable of simpler, single-die, RDL fabrication needs (as shown at right).





Example of Single-Die Redistribution (RDL) using HSIP

HSIP Reliability Baseline

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- HSIP Reliability Baseline

E-Test - Temperature Acceptance Test (ATP)	PASS
Temperature Shock – MIL-STD-810G, Method 503.5, Procedure I-Steady State	PASS
Electrostatic Discharge – EN 61000-4-2, Level 4	PASS
Electromagnetic Compatibility – MIL-STD-461F,RE101,RE102 & Radiated Susceptibility	PASS
Mechanical Shock – JEDEC Standard JESD22-B110A	PASS
Random Vibration – MIL-STD-810G, Method 514.5; system operating during exposure	PASS
High Temperature – MIL-STD-810G, Method 501.5; 2 day steady state +71°C	PASS
Low Temperature – MIL-STD-810G, Method 502.5; 2 day steady state -35°C	PASS
Low Pressure (Altitude) – MIL-STD-810G; system operating during exposure	PASS
Humidity – MIL-STD-810G, Method 507.5’ system operating through test	PASS
Rain – MIL-STD-810G, Method 506.5, device in system format	PASS
1000 hours of HTOL at 125 degrees C	PASS
1000 hours of THB at 85%, 85C	PASS
2000 thermal cycles -29C to +85C	PASS

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TRL / MRL Status of HSIP

CAPABILITY	TRL	MRL	DEPLOYMENT
Single Die RDL, Single Sided Interconnect	TRL-4	MRL-5	Prototyped
Multi Die HSIP, Single Sided Interconnect	TRL-3	MRL-5	D0 Prototype Starting
Multi Die HSIP, Double Sided Interconnect	TRL-7	MRL-7	DX Program POM
Double Sided Die HSIP, Double Sided Interconnect	TRL-2	MRL-3	Concept Vehicle
Two-Slice HSIP Stack	TRL-7	MRL-7	DX Program POM
Three-Slice HSIP Stack	TRL-5	MRL-5	Prototyped
Single-Slice HSIP	TRL-9	MRL-9	7 years deployed system

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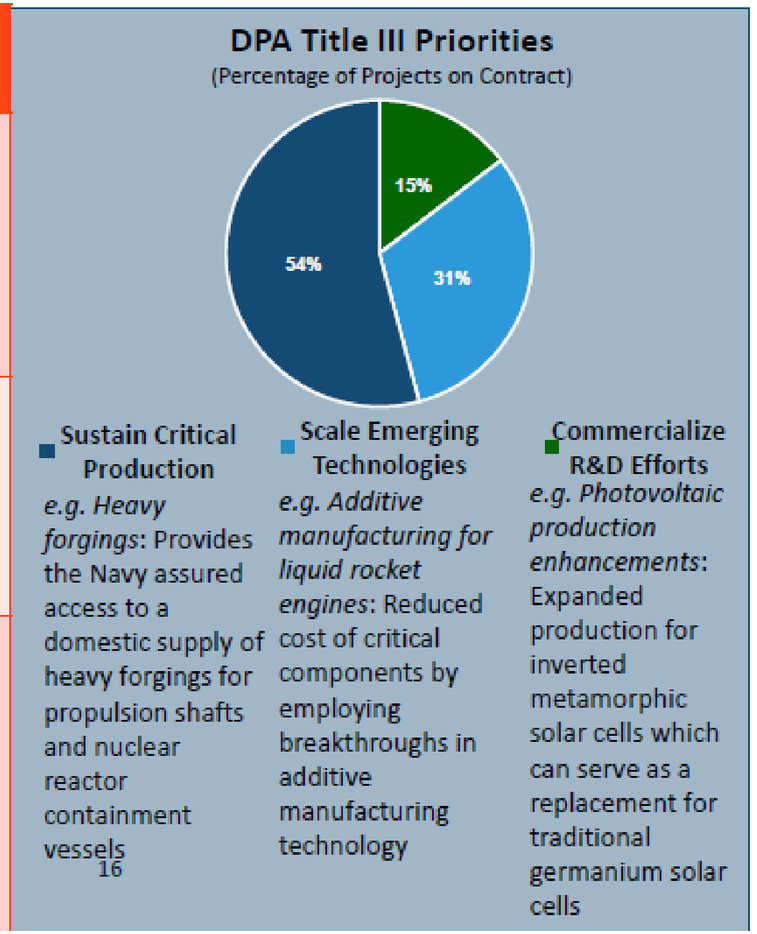
Defense Production Act - Title III Grant

- Title III Grant
  - i3 Microsystems has been selected as the manufacturing subcontractor on a DPA (Defense Production Act) Title III Contract
  - Phase I will cost-down and automate the wafer production technology

DPA Title III Priorities

DPA Title III Priorities (50 U.S.C. Chapter 55 §4533)
Sustain Critical Production "To create, maintain, protect, expand, or restore domestic industrial base capabilities essential for the national defense"
Commercialize R&D Efforts "from Government sponsored research and development to commercial applications;"
Scale Emerging Technologies "for the increased use of emerging technologies in security program applications and the rapid transition of emerging technologies"



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Defense Production Act - Title III Grant

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Source: http://uscode.house.gov/browse/prelim@title50/chapter55/subchapter2&edition=prelim

- Title III Grant – Presidential Determination:

Criteria for DPA Title III Purchases & Commitments (§4533)

The President must determine that…

A. the industrial resource, material, or critical technology item is essential to the national defense;

B. without Presidential action under this section, United States industry cannot reasonably be expected to provide the capability for the needed industrial resource, material, or critical technology item in a timely manner;

C. purchases, purchase commitments, or other action pursuant to this section are the most cost effective, expedient, and practical alternative method for meeting the need.

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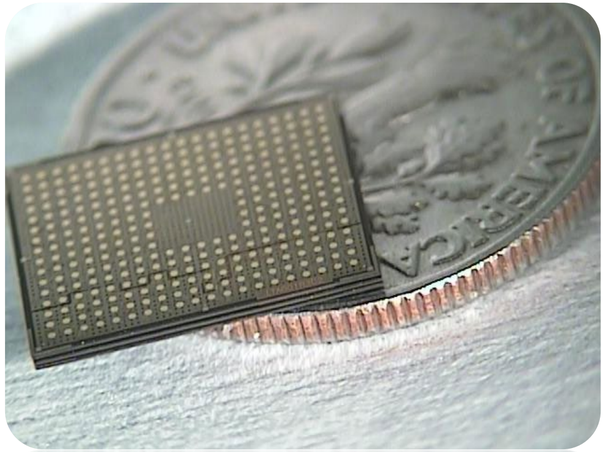
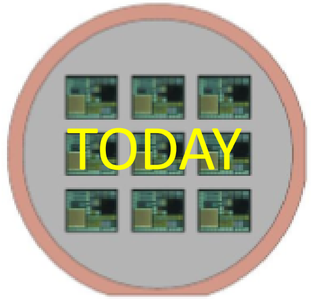
Defense Production Act - Title III Grant



Stacked HSIP Modules
24 Total Metal Layers
BGA Interface

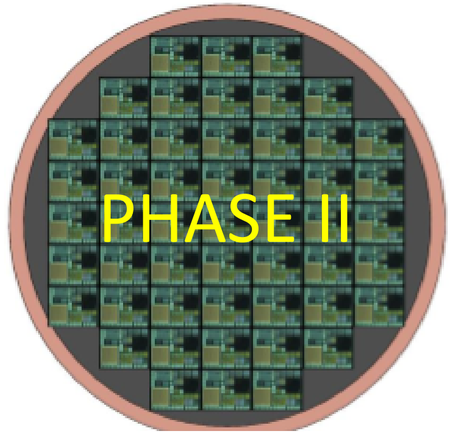
Technology Protection
Current Baseline



100mm Cavity Wafer

100mm Reconstituted Wafer

1.8X more modules per wafer



150mm Reconstituted Wafer

6X more modules per wafer

YIELD IMPROVEMENTS & MOLDED WAFER

PROCESS TOOL AUTOMATIONS

PROCESS TOOL REDUNDANCIES

WAFER-SIZE SCALING FOR VOLUME DEMAND

PHASE I

PHASE II

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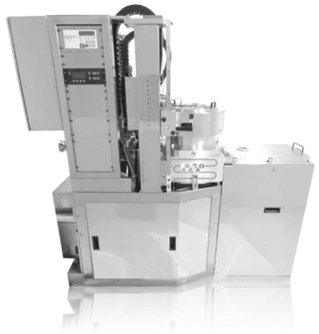
Defense Production Act - Title III Grant

Automated Plating Tool

Coat-Develop Cluster Tool

Automated Optical Inspection



Automated Plasma Etch Tool

Equipment Purchase Line Item	Benefits
Automated Optical Inspection	Automation, Lowers Cost
Copper Plating Bench	Automation, Improves Yield
ENEPIG Bench	Automation, Improves Yield
RIE	Automation, Improves Yield
Laser	Replaces Obsolete Equipment
Wafer Bonder	Automation, Lowers Cost
Wafer De-Bonder	Automation, Lowers Cost
Dielectric Coat - Develop Tool	Automation, Improves Yield
Wafer Cassette Standardization	Improves Yield
Automated Die Handling (P&P)	Lowers Cost
Automated Nikon Loading	Lowers Cost
Automated Stepper Loading	Lowers Cost
Microscope Upgrades (4)	Improves Yield

EVG850TBL
Wafer Bonder

EVG850DB
Wafer De-Bonder

HSIP Fabrication

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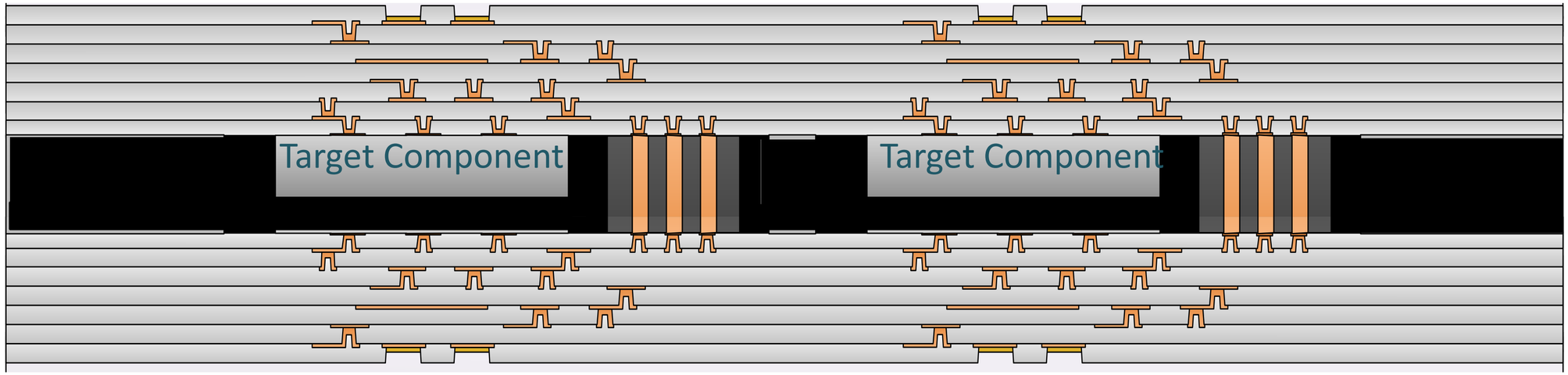
- HSIP Fabrication Discussion



Detail view of HSIP module Layers

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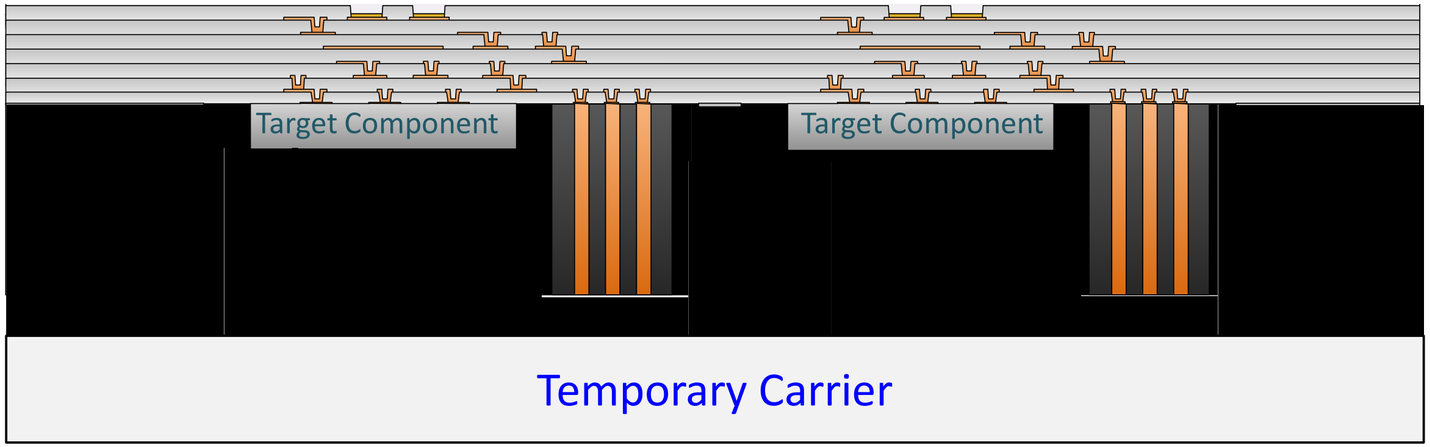
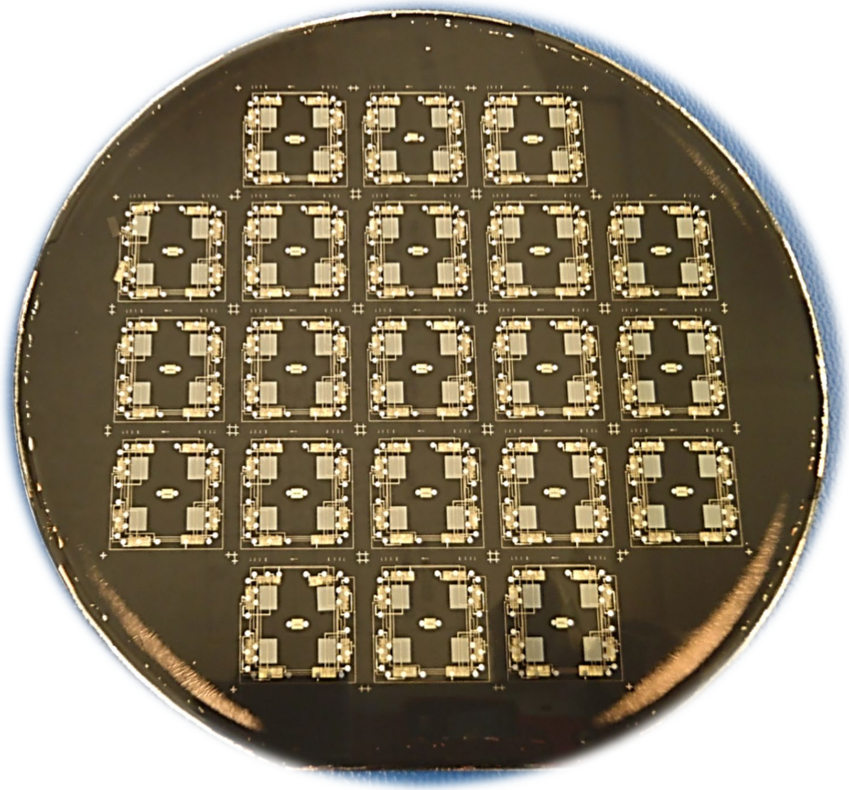
HSIP Fabrication



Molded (Reconstituted) wafer over carrier



actual wafer

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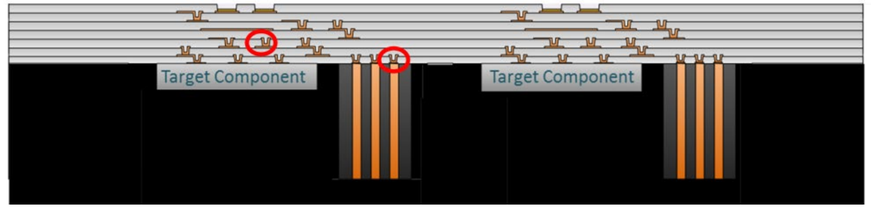
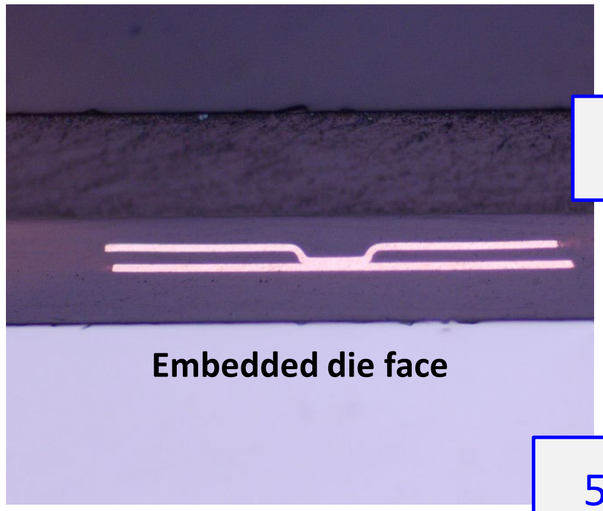
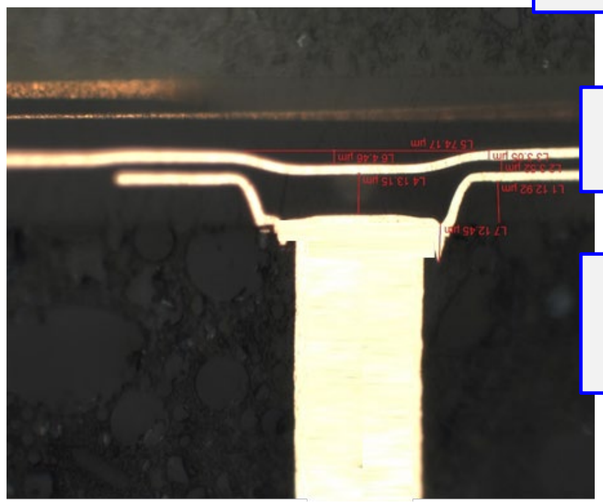
HSIP Fabrication





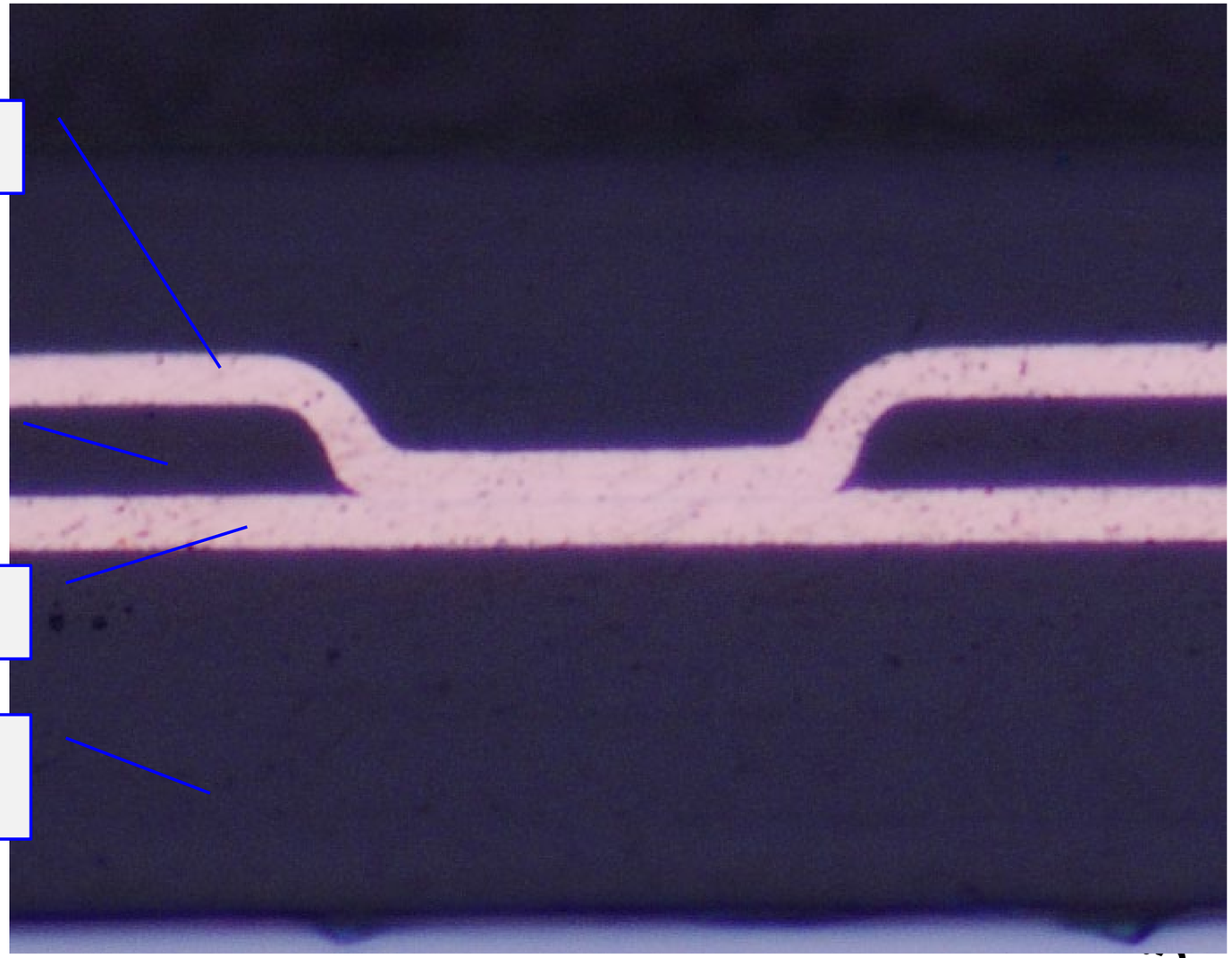


2-micron copper

5-micron dielectric

2-micron copper

15-micron dielectric
(3 Layers)



HSIP Fabrication

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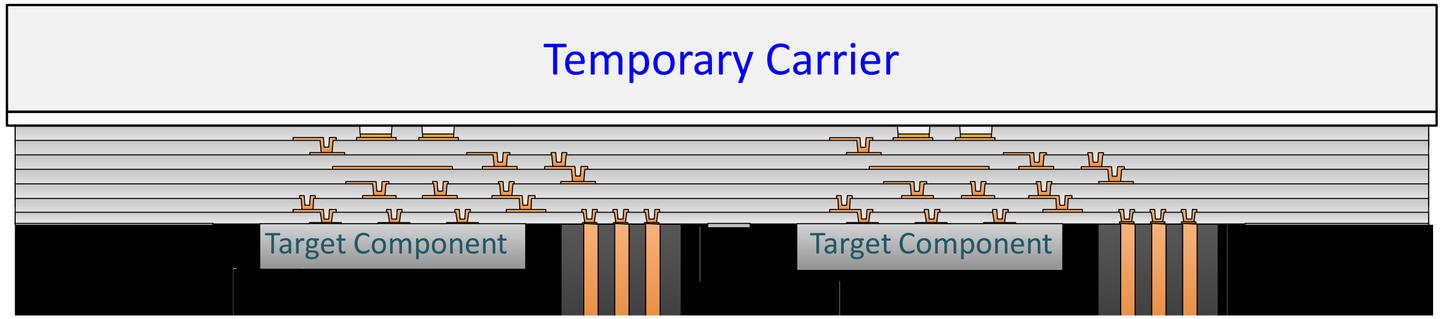
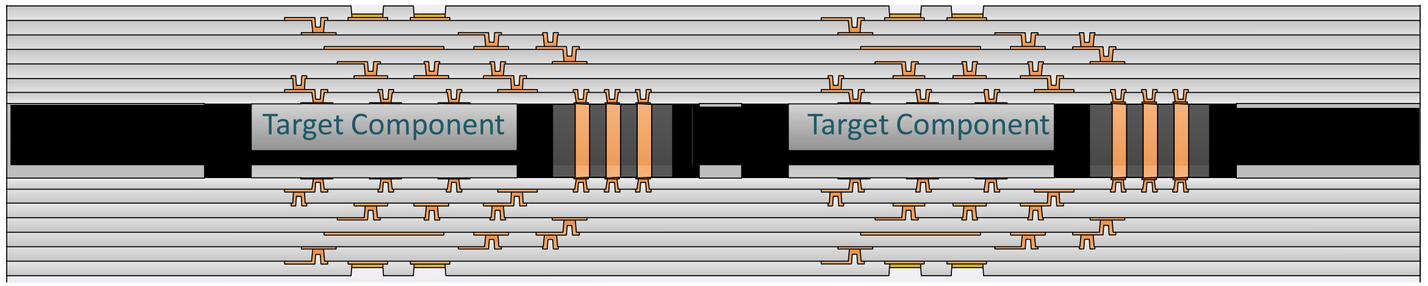
Backside Wafer Thinning

- Opens the Thru-Via contacts
- Brings core of device to target value



Completion of Backside Layers

- Temporary Carrier removed
- Device is singulated in normal dicing fashion



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HSIP Fabrication Example

Date	Wafer	Module	Module Thickness Core (um)	Module Thickness Total (um)	Wafer Bond Thickness (um)	Module Bow (um)	XY Size (um)
6/13/2017	NPT-001					9.7	
6/13/2017	NPT-001					14.4	
6/13/2017	NPT-001					15.6	
6/13/2017	NPT-001						
6/13/2017	NPT-001						
6/13/2017	NPT-002	R5C2	263.4	338.1	42.2	15.9	14606.4
6/13/2017	NPT-002	R4C4	266.0	333.3	45.4	17.8	14597.2
6/13/2017	NPT-002	R1C2	268.7	333.9	46.5	7.4	14604.3
6/13/2017	NPT-002	R2C3	268.2	338.1	45.9	1.6	14601.3
6/13/2017	NPT-002	R3C5	263.4	335.8	46.5	18.3	14591.7
7/24/2017	NPT-003	R1C3	270.7	345.9	41.3	12.6	14625.6
7/24/2017	NPT-003	R1C4	268.5	344.8	43.4	16.3	14608.6
7/24/2017	NPT-003	R3C1	272.8	346.4	38.7	19.7	14621.6
7/24/2017	NPT-003	R4C2	269.6	344.8	45.6	20.0	14593.8
7/24/2017	NPT-003	R4C4	273.2	351.8	48.0	13.2	14598.8
6/13/2017	NPT-004	R2C1	273.8	350.5	41.3	24.9	14557.9
6/13/2017	NPT-004	R2C3	271.2	348.9	46.6	31.4	14568.0
6/13/2017	NPT-004	R3C2	271.7	352.6	56.3	30.4	14576.1
6/13/2017	NPT-004	R4C4	278.1	354.2	42.9	23.2	14575.0
6/13/2017	NPT-004	R5C3	277.6	353.7	38.0	1.0	14572.0

Final Module Bow

Mean 14.5um

Stdev 11.2um

Final Module Thickness

Mean 346.4um

Stdev 7.0um

Final Module Core

Mean 270.5um

Stdev 4.4um

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Conclusion

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HSIP technology can produce robust electronic components that meet next-generation packaging requirements for tightly packed integrations in order to achieve the lowest power, weight, and size while enabling new and exciting system concepts for designers

THANK YOU