IMAPS DPC March 5th, 2020

Collective D2W Hybrid Bonding for 3D SIC and Heterogeneous Integration

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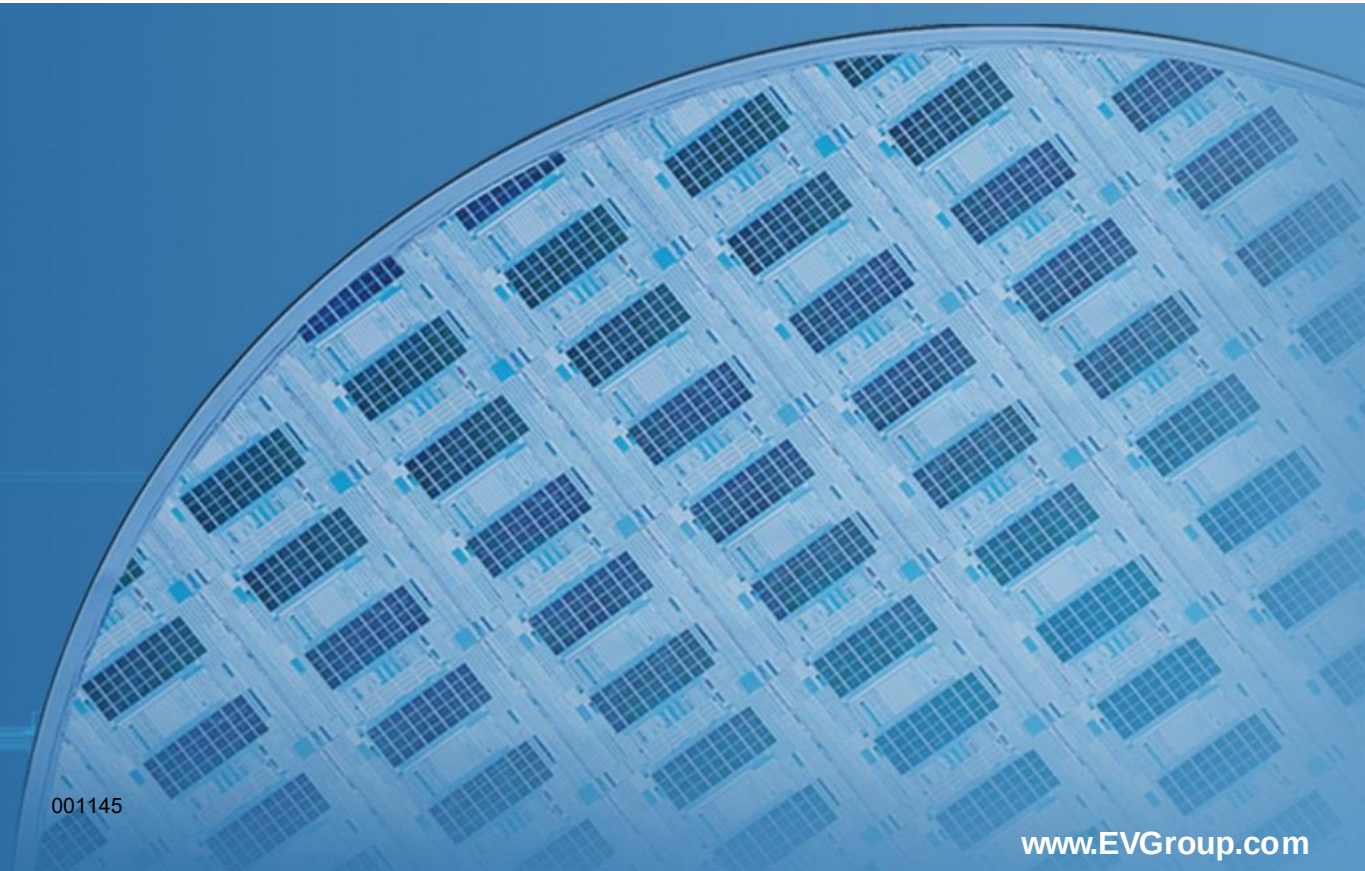

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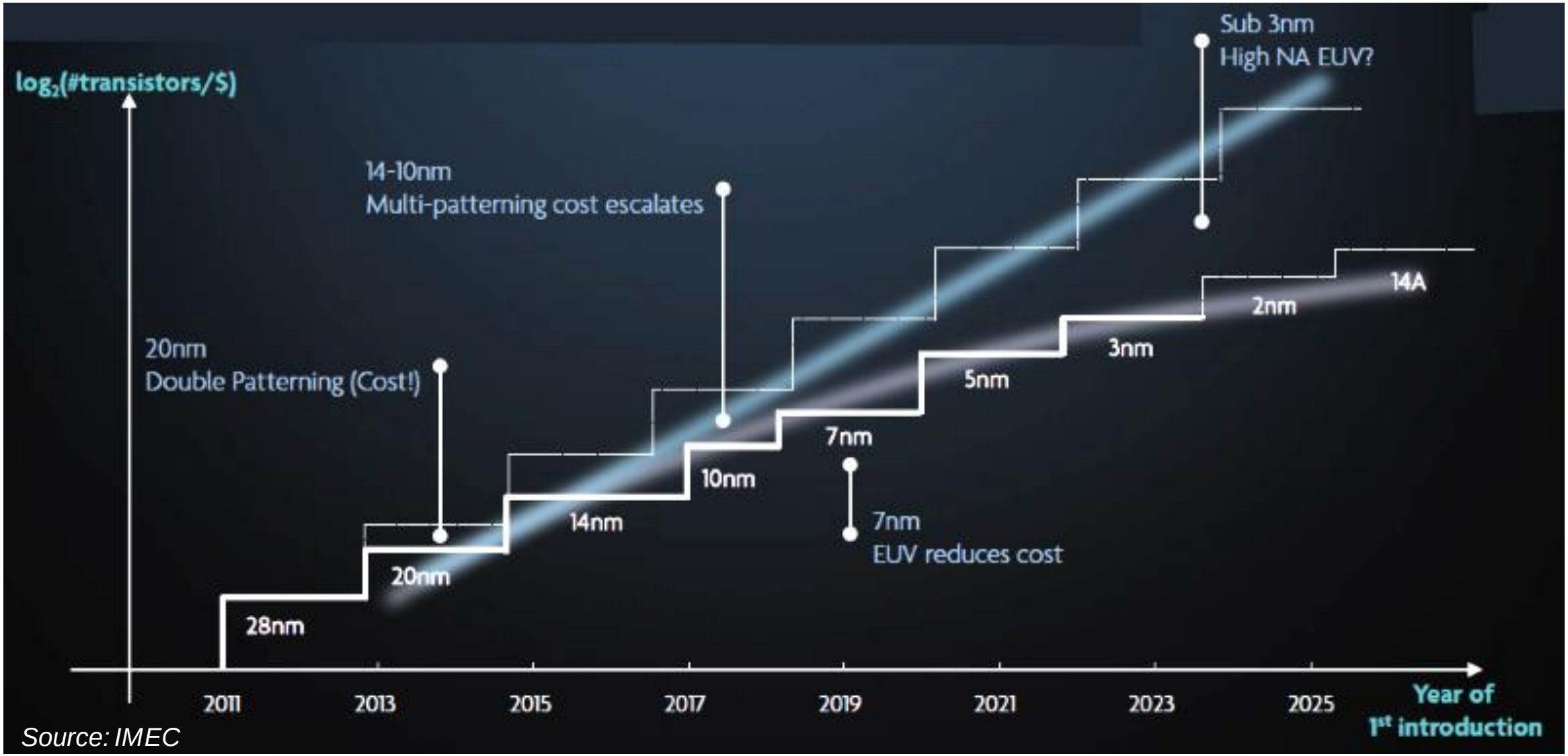
Outline

- Technology Drivers for D2W
- Collective D2W Bonding Motivation
- Process Results
- Outlook and EVG Heterogeneous Integration Competence Center

Market Outlook | Moores Law through Litho Nodes is Challenged



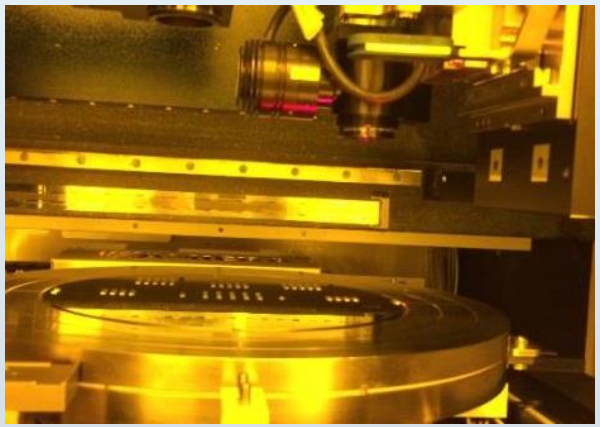
Source: IMEC

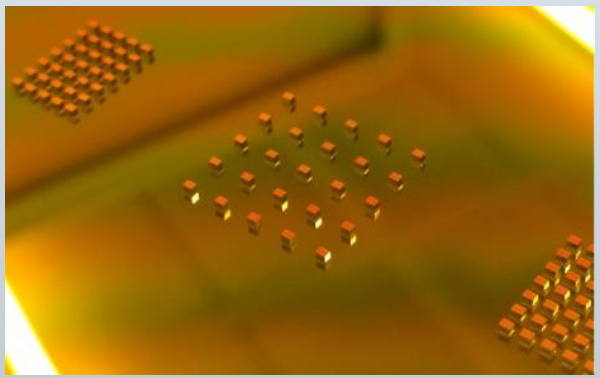
3D and Heterogeneous Integration

3D – SIC | Die Stacking

Hybrid or Fusion Bonding of dies to a receptor wafer

Collective D2W Integration
EVG GEMINI

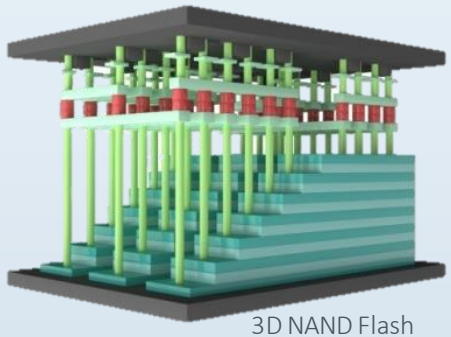




3D – SOC | Parallel W2W

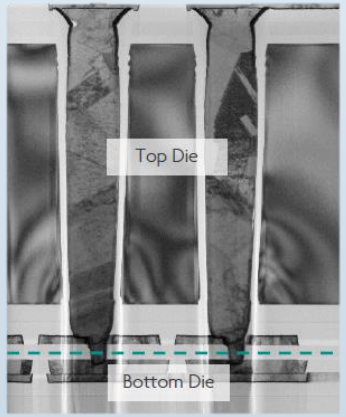
Hybrid Bonding of two FEOL metallization circuits

Hybrid Bonding
EVG GEMINI FB XT



3D NAND Flash
Logic to cell bond

3D SoC
die/ wafer stacking



DRAM on logic
F2F bonding

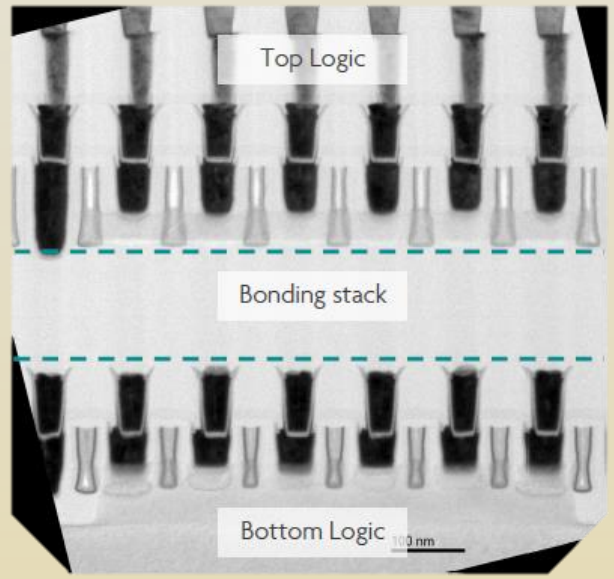
Source: IMEC

3D-SOC/ 3D-IC | Sequential FEOL

Combination of wafer to wafer bonding and deposition

Layer Transfer
EVG BONDSCALE

3D SoC
sequential 3D



Logic block on logic block

Source: IMEC

3D and Heterogeneous Integration

	3D-SIP			3D-SIC	3D-SOC		3D-IC	
3D Technology	"PoP"	"Chip last"	"Chip first"	Die stacking	Parallel W2W		Sequential FEOL	
3D-Wiring level	Package I/O	Chip I/O Interposer I/O	Chip I/O	Global	Semi-global	Intermediate	Local	FEOL
					Chip BEOL Wiring Hierarchy			
Partitioning	Functional unit	subsystem	Embedded die	Die	Blocks of standard cells		Standard cells	Transistors
Technology	Package-to Package reflow	Multi-die SIP 3D/2.5D stack	FO-WLP Embedded die	3D D2D D2W 2.5D Si-interposer	Wafer-to-Wafer bonding		Active layer transfer or deposition	
					Hybrid bonding	Via-last		
2-tier stack Schematic								
Characteristic	Solder ball Stack	• C4, Cu-pillar Si-Organic • Through-	• Bumpless • Si-RDL • Through-	• µbump • Si-to-Si • Through-Silicon-Via	BEOL between 2 FEOL layers		FEOL stack	
					Overlay 2nd tier defined by W2W alignment/bonding		Overlay 2nd tier defined by litho scanner alignment	
				40 ⇒20 ⇒10⇒5µm	5µm ⇒ 1 µm	2 µm ⇒ 0.5 µm	200nm ⇒ 100 nm	< 100 nm
				1 ⇒ 4 ⇒16⇒ 64	64 ⇒ 1600	400 ⇒ 6400	4 10^4 ⇒ 1.6 10^5	> 1.6 10^5

Wafer backside processing

Temporary Bonding with Polymers
EVG 850

Hybrid or Fusion Bonding of dies to a receptor wafer

Collective D2W Bonding
EVG GEMINI

Hybrid Bonding of two FEOL metallization circuits

Hybrid Bonding
EVG GEMINI FB XT

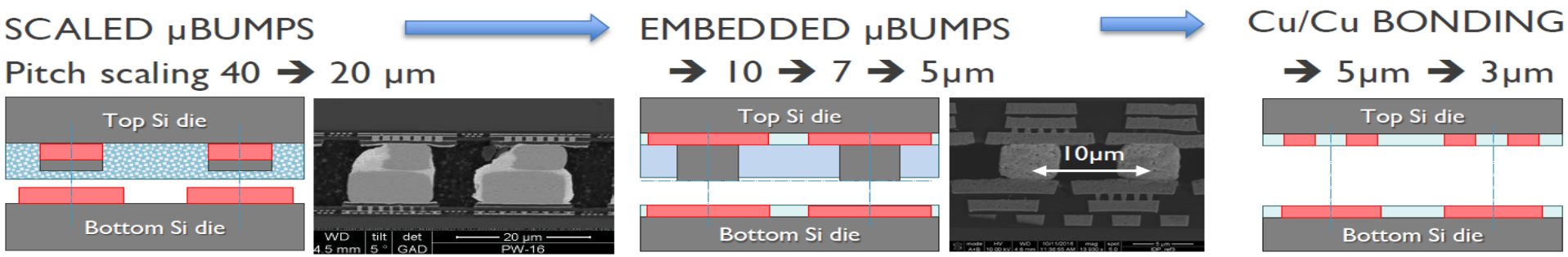
Combination of wafer-to-wafer bonding and deposition

Layer Transfer
EVG BONDSCALE

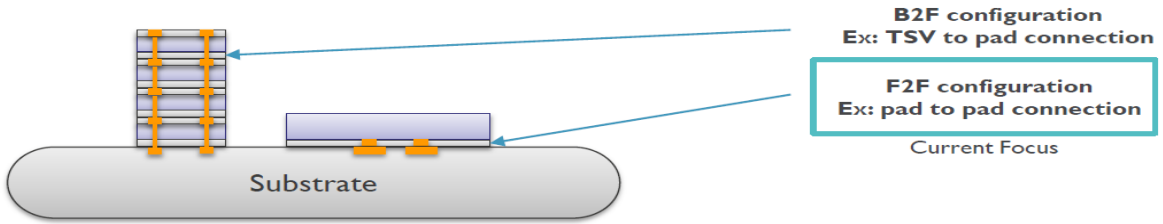
Collective D2W Bonding

D2W Roadmap

- W2W is ideal for image sensors & 3D NAND however heterogeneous integration with multiple wafer sources, different run-out and errors and most importantly die sizes is not working
- KGD is increasingly important with system complexity
- Full advantage of SoCs needs both W2W as well as D2W bonding

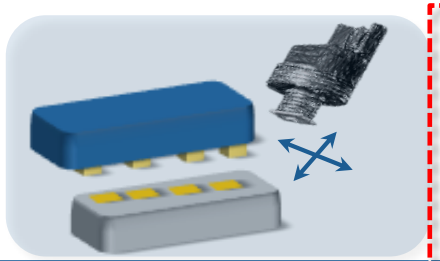
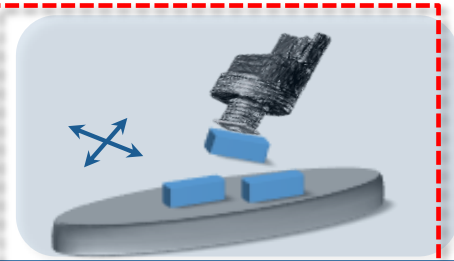
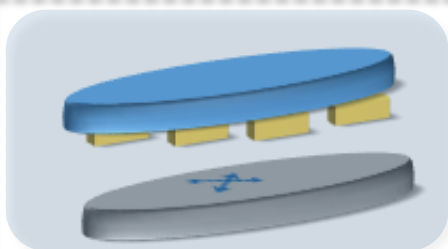
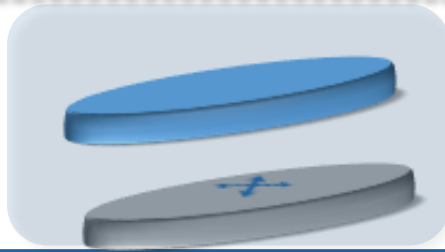


- Multiple layer die to wafer direct / hybrid / fusion bonding



- Target applications :
  - High density memory N>>2
  - Unequal die size assembly with fine pitch <10µm
  - Restricted thermal budget applications (ex: CTE mismatched materials)

Die to Die vs. Wafer to Wafer

Stacking Method	Chip to Chip	Chip to Wafer	Collective Die to Wafer	Wafer to Wafer
Throughput	Low	Mid	High	High
Yield	High*	High*	High*	Mid
Application	Packaging	Processor, Memory, Mems	Image Sensor, Processor, Memory, Mems	Image Sensor, Processor, Memory, Mems
Alignment	1 µm**	1 µm**	> 1 µm**	100 nm
Challenges	Alignment accuracy Cleanliness / Plasma Throughput	Alignment accuracy Cleanliness / Plasma Throughput	Yield	Yield Heterogeneous integration
Compatibility Hybrid Bonding	Mid	Mid	Yes ***	yes

* Known good dies
** Development for 200 nm
*** HVM for III-V Die transfer

Improved yield and throughput management

High yield application

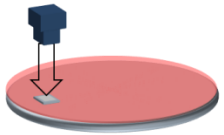
Collective Die Carrier Process Flow

Transfer Carrier Preparation

Glass or Silicon Carrier Wafer (non patterned or with alignment marks)

Carrier Wafer with Adhesive Layer

Carrier Population



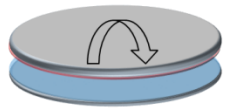
D2W Bonding

Fully populated carrier wafer

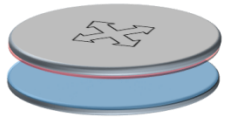
Wafer-to-Wafer Bonding

Collective Carrier

Target Wafer



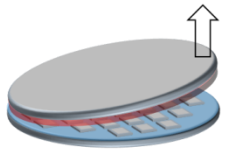
Carrier Flip



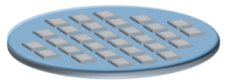
SmartView Alignment

Fusion Bonding

Carrier Separation

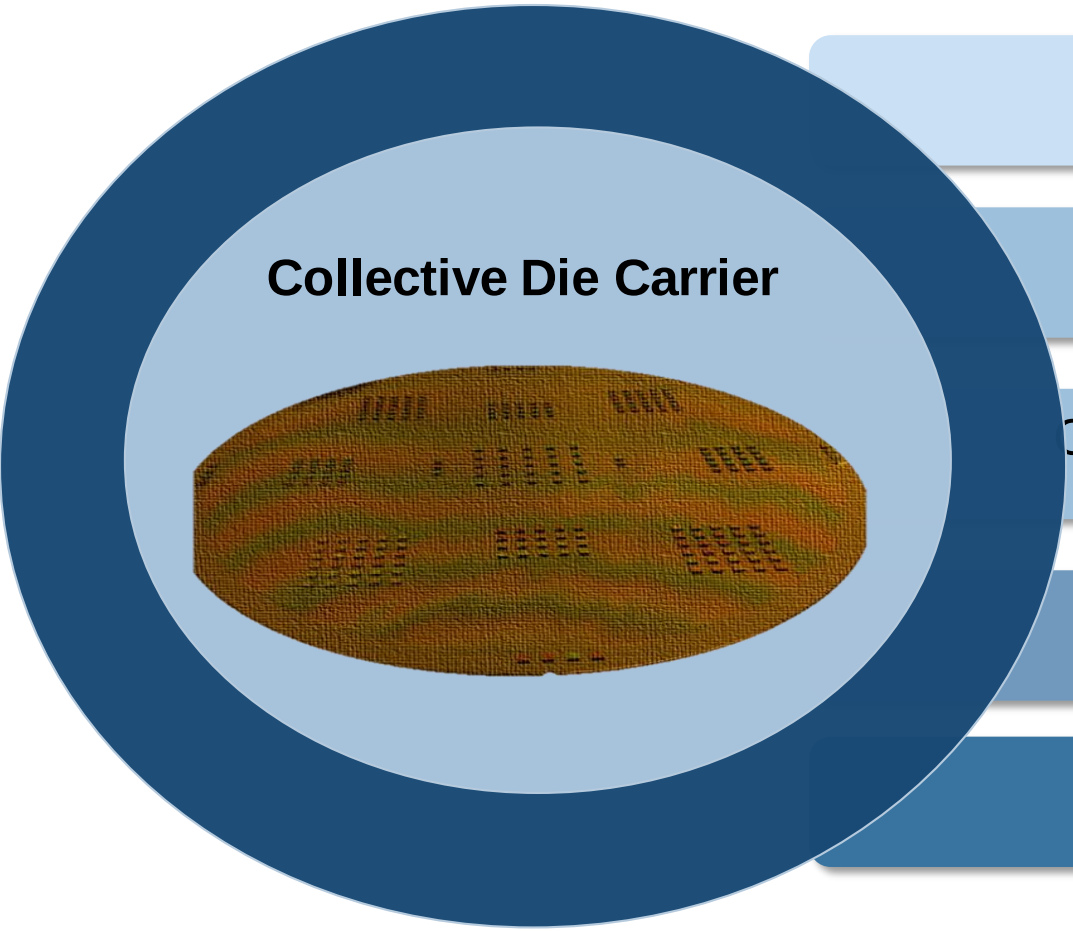


Slide-Off or Laser Debonding

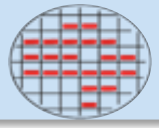


Surface Cleaning

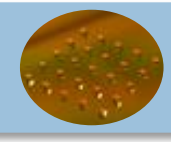
Die to Wafer Hybrid bonding - Status
Collective Die Carrier - Overcome Yield issue



Enables Wafer level processing
minimized risk of contamination



Enhanced oxide management
no Q-time impact, improved oxide management



Compatible with standard wafer processing Equipment
post processing is performed at Wafer level

Die placement accuracy
mainly limited by die placement accuracy of the die bonder

Compatible with multiple bonding technologies
Hybrid Bonding, Thermo compression, eutectic bonding, adhesive bonding

Die Preparation Considerations

Die Properties
- CMP / surface roughness
- Die size
- Edge properties
- Die thickness uniformity

Target Wafer
- CMP / surface roughness
- Protrusion / Dishing of Cu in case of hybrid bonding
- Pad dimensions

Pick and Place
- Placement accuracy (x, y)
- Die rotation
- Die tacking temperature

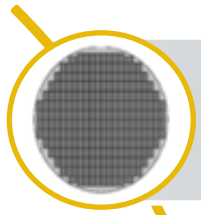
Bond Process
- Die and target wafer surface activation
- Alignment
- Cleaning
- Bond force, temperature and time

Transfer Plate
- Transfer plate materials
- Adhesive thickness and uniformity

Debond and Cleaning
- Debond technology
- Cleaning solvent
- Cleaning time
- Solvent compatibility

Process Results

Collective Die Transfer | EVG in house capabilities



Die Size

800 µm * 800 µm up to 10*10 mm

Materials

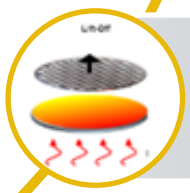
InP, GaAs, Si, GaN, SiC

Carrier Size

200 mm & 300 mm

Bonding Processes

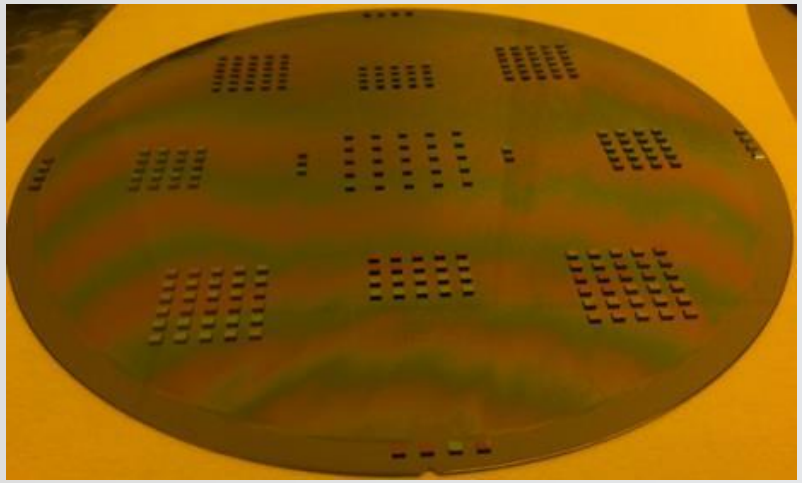
Direct, Metal, Adhesive, Hybrid bonding

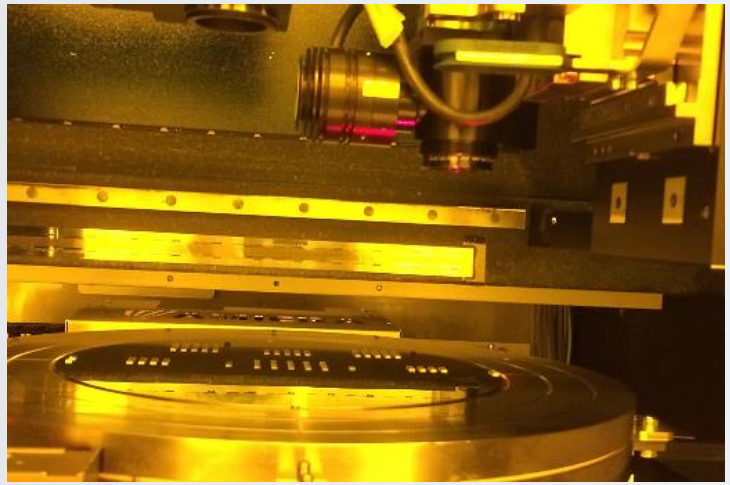


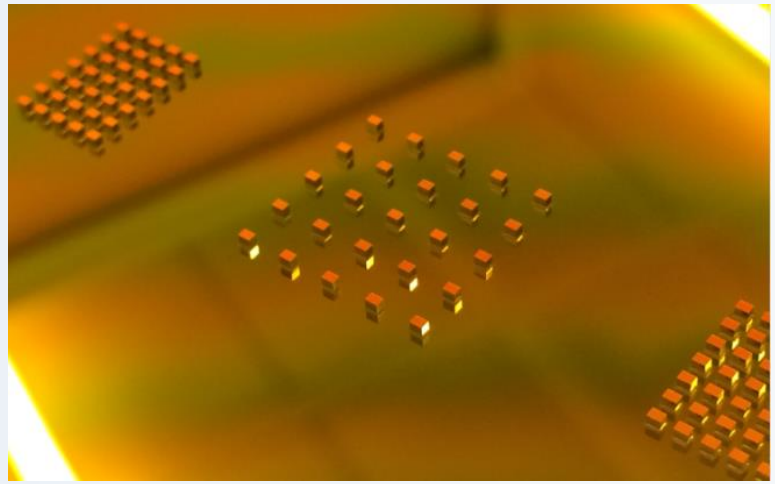
Debonding Technology

Thermal, Laser debonding

Collective Die Transfer | Carrier Preparation

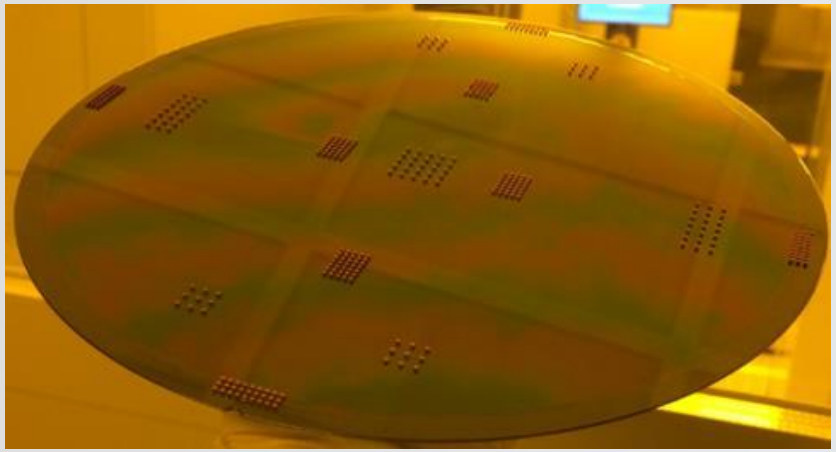


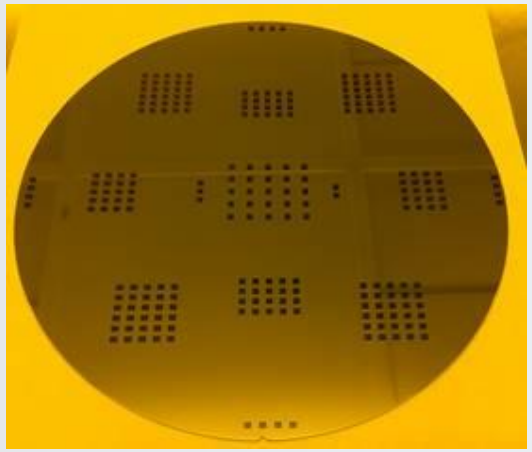


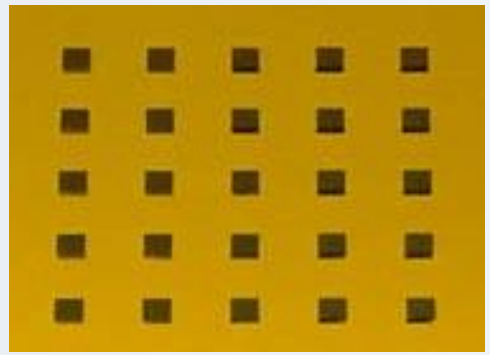


- Individual die placement and pitch
- Carrier placement with or w/o alignment structures
- Moderate die size variation within a wafer

Collective Die Transfer | Bonding Results







GaAs & GaN die transfer using Cu-Cu bonding process

Die size: 800µm * 600µm
Transfer-rate: 100%

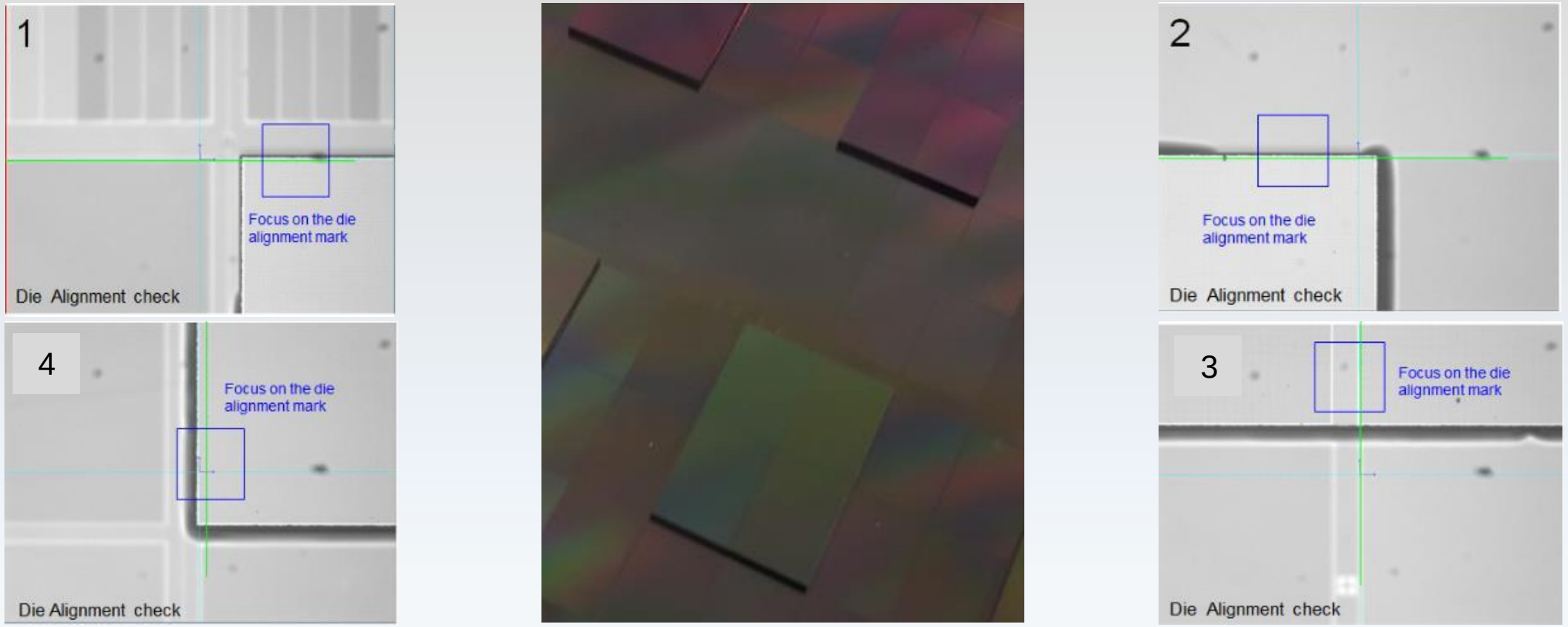
Si die transfer using adhesive (BCB) bonding process

Die size: 800µm * 600µm
Transfer-rate: 100%

SiO_2 die transfer using direct bonding

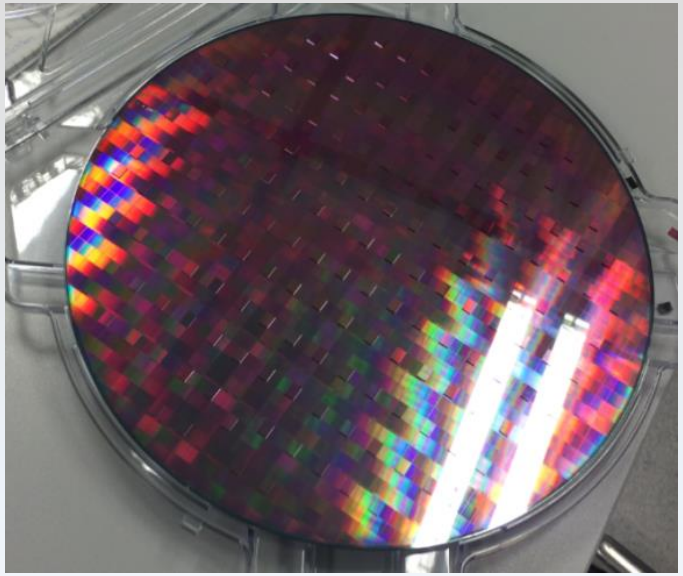
Die size: 1000µm * 1000µm
Transfer-rate: >98%

Collective Die Transfer | Placement Accuracy on Collective Die Carrier

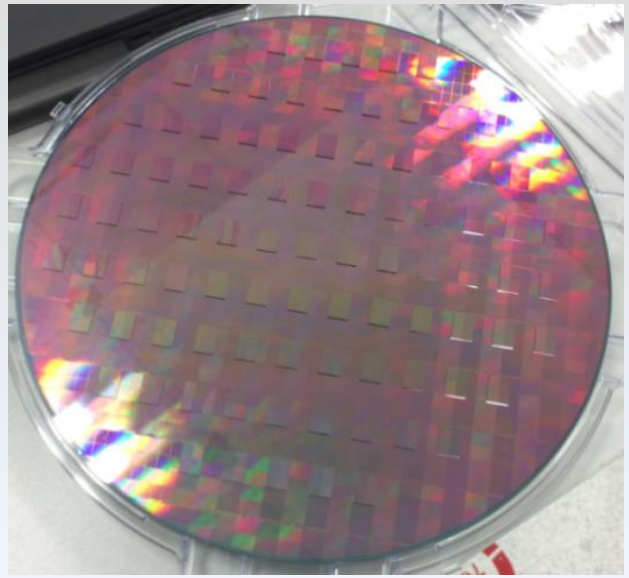


Demonstrator	Die Dimension	Placement accuracy X 3σ	Placement accuracy Y 3σ
A	5mm x 7mm	< 2 µm	< 2 µm
B	10mm x 14mm		

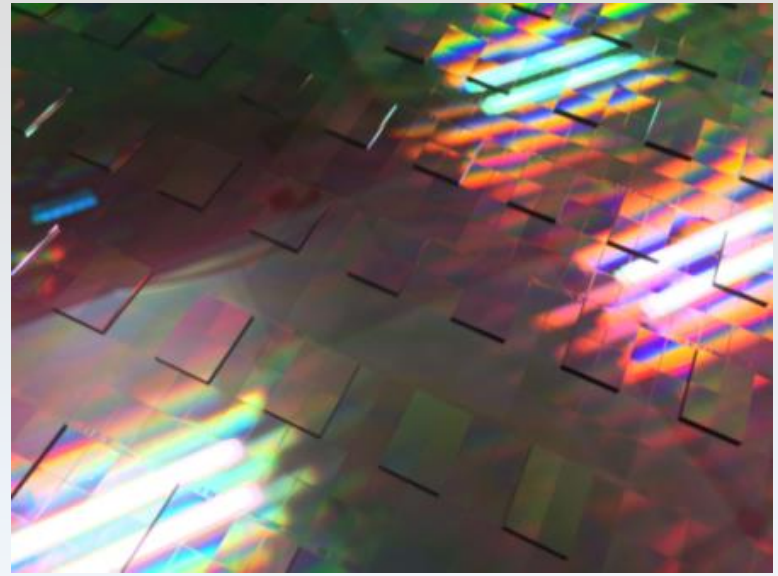
Collective Die Transfer | Recent Bonding Results



Demonstrator A - 300mm
Hybrid Bonding, 5mmx7mm



Demonstrator B - 300mm
Hybrid Bonding,10mmx14mm



→ Pad Size 4 µm – 1µm

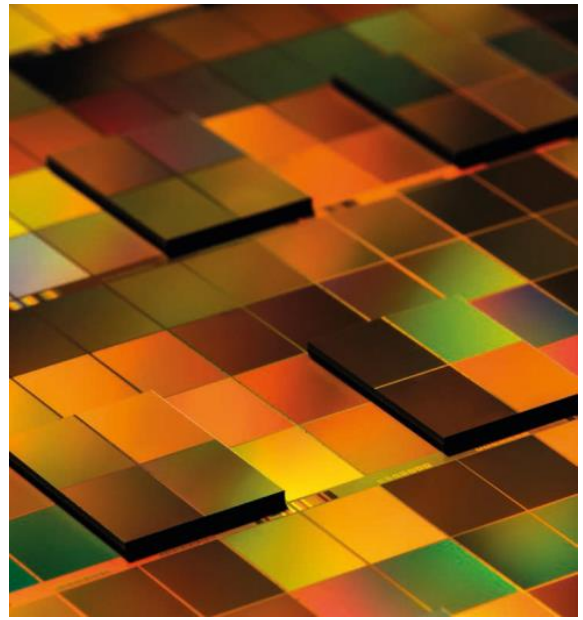
→ Pitch 8,8 µm – 2 µm

Outlook

Heterogeneous Integration Competence Center | Launch 2020

ST. FLORIAN, Austria, March 2, 2020

"Heterogeneous integration fuels new packaging architectures and demands new manufacturing technologies to support greater system and design flexibility, as well as increased performance and lower system design costs," stated Markus Wimplinger, corporate technology development & IP director of EV Group.
"EVG's new HI Competence Center provides an open access innovation incubator for our customers and partners across the microelectronics supply chain to collaborate while pooling our solutions and process technology resources to shorten development cycles and time to market for innovative devices and applications enabled by heterogeneous integration."



Facility-Infrastructure	IT-Infrastructure	Risk Reduction
Process Development	Process Transfer	

Die to Wafer Bonding – Collaboration Framework

Material scouring

Die preparation

(wafer material, Cu dishing management, protection layer, dicing..)

Carrier preparation

(local & global alignment key)

Die Transfer

Carrier coating

(temporary bonding adhesive)

Die placement onto carrier

Collective die Carrier preparation

(protection layer removal, Plasma activation, cleaning)

Die Transfer

(Wafer to wafer alignment, bonding , debonding ,annealing, metrology)

Post Die Transfer Metrology

(die placement accuracy , bonding quality)

Post processing

Target Wafer back side processing

(tbd ..grinding, metal, litho ,etc..)

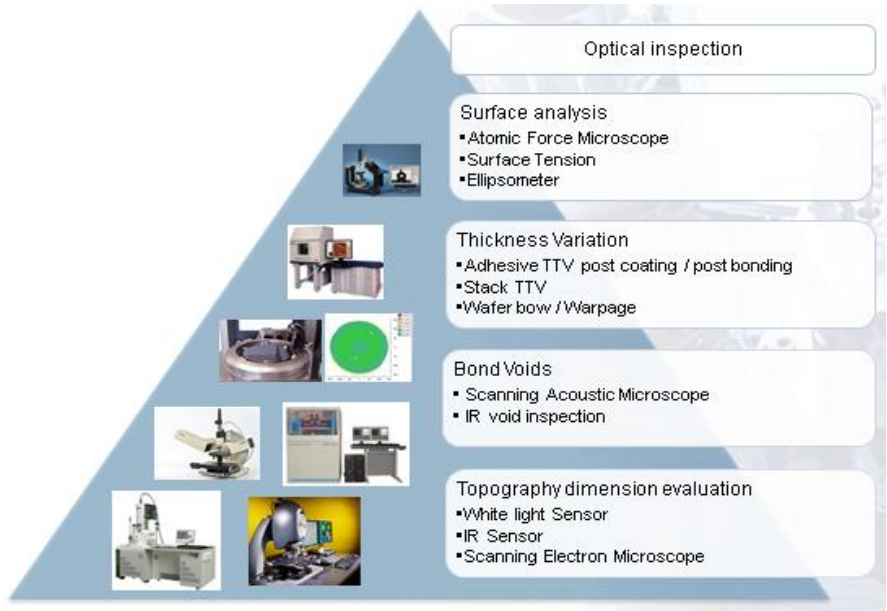
Final Metrology

Summary - Process Development capability

Class 100 Clean room facility

Automated Wafer Bonding systems for development

Metrology equipment capability



Highly competitive wafer processing and metrology capability from 2“ to 300 mm
Fully automated bonding capability for 200 mm & 300 mm

Thank you for your attention.