Copper Wire Ready For Automotive AEC Requirements?

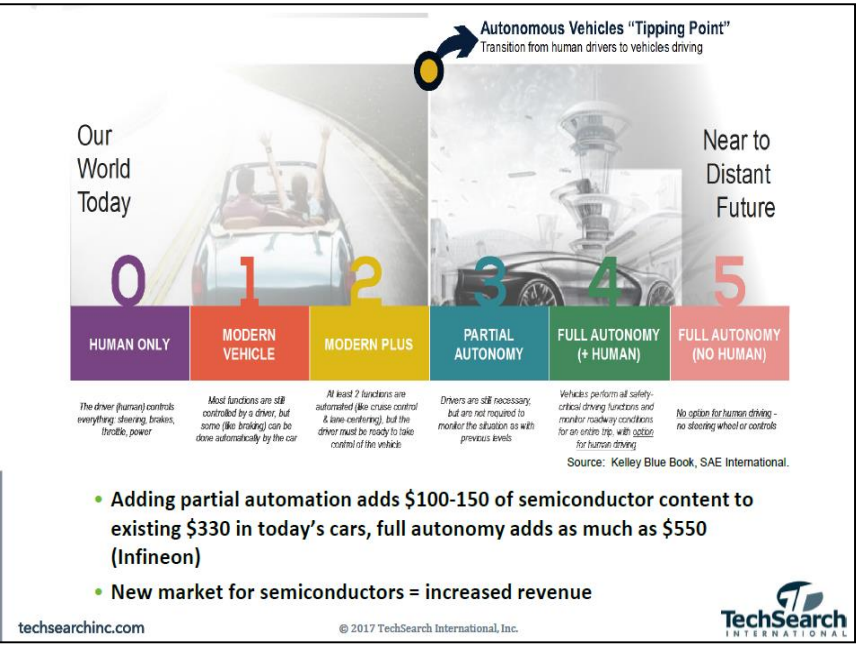
2018:

- **The market of Cu bonding wires has been divided into two types: bare Cu wires (high purity) and palladium coated (PdCu) bonding wires. These wires have yet to satisfy the required characteristics for high reliability products such as industrial and automotive electronics.**

Contents

- Semiconductor Content Increasing
- Overview of Jedec (Commercial Electronics)
- Intro to AEC Q100 (Automotive)
- AEC Q006 for Cu wire (Automotive)
- Various Data Comparisons
  - > Conventional PCC
  - > High Rel PCC (2N Cu core/4N Cu core)
- Intro to AEC Q100 (Automotive)
- Intro to Cu alloy for high Rel

Semiconductor $$ Content per Vehicle



- Adding partial automation adds $100-150 of semiconductor content to existing $330 in today's cars, full autonomy adds as much as $550 (Infineon)
- New market for semiconductors = increased revenue

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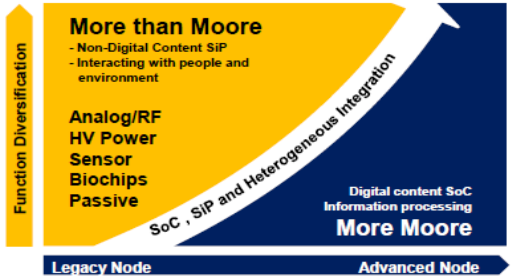
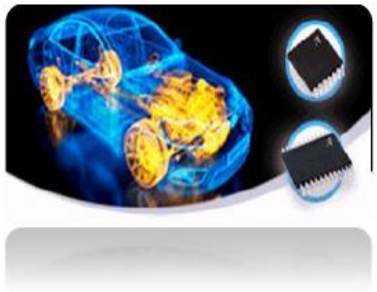
Specialty Technologies will Support the Growth

- **Specialty technologies reflect "More than Moore"**
  - **Focus is not on Advance nodes or Digital Content**
  - **Focus is on Performance and Analog Content**
    - **Higher Voltages, Precision, Interface, Robustness**
- **Products have longer Life Cycles; Longevity of Investment Increased**



Source : "More than Moore White Paper", ITRS

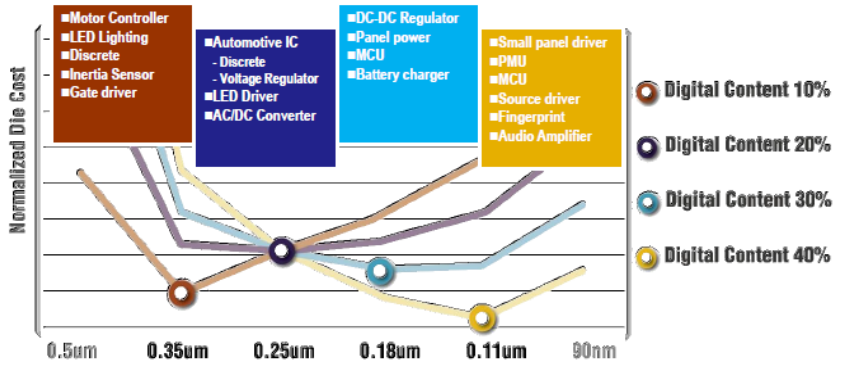
- **Conventional vehicle** semiconductor content per vehicle will grow from $280 in 2015 to $450 in 2020
- **Electric vehicle** semiconductor content is higher than conventional models with $750 per vehicle in 2020



Source: TechSearch

Specialty Technology ICs

- **0.35um to 0.11um are ideal geometries for specialty technology targeting automotive, IoT applications**
- **Focus is on performance and limited digital content**



Source: Internet

JEDEC Standards (Snapshot)

- All figures from www.jedec.org

JEDEC Introduction

- JEDEC was founded in 1960 and stands for the Joint Electron Device Engineering Council.
- JEDEC is the standardization body of the Electronic Industries Alliance, which helps develop standards on electronic components, consumer electronics, electronic information, telecommunications, and internet security.
- JEDEC issues often used standards for device interfaces, such as RAM and DDR SDRAM(double-data-rate synchronous dynamic random access memory), which is a type of memory in integrated circuits used in computers.

Wikipedia,http://en.wikipedia.org/wiki/JEDEC

Source: Internet

Examples of standards

- **JESD 22-A103C HIGH TEMPERATURE STORAGE LIFE:** The test is applicable for evaluation, screening, monitoring, and/or qualification of all solid state devices.
- High Temperature storage test is typically used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms of solid state electronic devices
- During the test elevated temperatures (accelerated test conditions) are used without electrical stress applied.

- **JESD 22-A104C TEMPERATURE CYCLING:** This standard provides a method for determining solid state devices capability to withstand extreme temperature cycling.

- **JESD 22-A106B**
  THERMAL SHOCK: This test is conducted to determine the resistance of a part to sudden exposure to extreme changes in temperature and to the effect of alternate exposures to these extremes.

Source: Internet

Method of Testing

- The samples will be stored at one of the temperature conditions given in Table 1:

Table 1: High Temperature Storage Conditions

Condition A: +125(-0/+10) ºC
Condition B: +150(-0/+10) ºC
Condition C: +175(-0/+10) ºC
Condition D: +200(-0/+10) ºC
Condition E: +250(-0/+10) ºC
Condition F: +300(-0/+10) ºC
Condition G: +85(-0/+10) ºC

Source: Internet

AEC-Q100 is a set of reliability stress tests defined by the Automotive Electronics Council for the purpose of qualifying integrated circuits (ICs) for automotive applications. Linear qualifies products based on AEC-Q100 guidelines and guarantees that all automotive products exceed current AEC-Q100 requirements by conducting additional device and package level stress tests.

Summary of AEC- Q100 Guideline

STRESS	ABV	#	# of LOTS	SS / LOT	ACC	METHOD
Preconditioning	PC	A1	3	77	Ø	JEDEC J-STD-020 JESD A113
Temperature-Humidity-Bias or Biased HAST	THB or HAST	A2	1	45	Ø	JEDEC JESD22 A101 or A110
Autoclave or Unbiased HAST	AC or HAST	A3	3	77	Ø	JEDEC JESD22 A102 or A118
Temperature Cycling	TC	A4	3	77	Ø	JEDEC JESD22 A104 and Appendix 3
Power Temp Cycle	PTC	A5	1	45	Ø	JEDEC JESD22 A105
High Temperature Storage Life	HTSL	A6	3	77	Ø	JEDEC JESD22 A103
High Temperature Operating Life	HTOL	A7	3	77	Ø	JEDEC JESD22 A108
Early Life Failure Rate	ELFR	B2	3	800	Ø	AEC Q100-008
NVM Endurance, Data Retention, and Operational Life	EDR	B3	3	77	Ø	AEC Q00-005
PACKAGE ASSEMBLY INTEGRITY TESTS						
Wire Bond Shear	WBS	C1	Per Shift	30 Bonds	Cpk >1.33 Ppk>1.67	AEC-Q100-001
Wire Bond Pull	WBP	C2	Per Shift	30 Bonds	Cpk >1.33 Ppk>1.67	MIL-STD-883 M2011
Solderability	SD	C3	1	15	Cpk >1.33 Ppk>1.67	JEDEC JESD22 B102
Physical Dimensions	PD	C4	3	10	Cpk >1.33 Ppk>1.67	JEDEC JESD22 B100 & B108
					Cpk >1.33 Ppk>1.67	AEC Q100-010
					Ø	JEDEC JESD22 B105

DIE FABRICATION INTEGRITY TESTS						
Electromigration	EM	D1	-	-	-	JESD 87 and JESD 202
Time Dependant Dielectric Breakdown	TDDB	D2	-	-	-	JESD 92
Hot Carrier Injection / Beta Degradation	HCI	D3	-	-	-	JESD 28
Negative Bias Temp Instability	NBTI	D4	-	-	-	JESD 90
Stress Migration	SM	D5	-	-	-	JESD 202
ELECTRICAL VERIFICATION						
Pre- and Post-Stress Function/Parameter	TEST	E1	ALL	ALL	Ø	ATE
Electrostatic Discharge Human Body Model / Machine Model	HBM / MM	E2	1	3 per Step	N/A	AEC Q100-002 & 003
Electrostatic Discharge Charged Device Model	CDM	E3	1	3 per Step	N/A	AEC Q100-011
Latch-up	LU	E4	1	6	N/A	AEC Q100-004
Electrical Distributions	ED	E5	3	30	Cpk >1.33	AEC Q100-009
Fault Grading	FG	E6	-	-	-	AEC Q100-007
Characterization	CHAR	E7	-	-	-	AEC Q003
Electrothermally Induced Gate Leakage	GL	E8	1	6	Ø	AEC Q100-006
Electromagnetic Compatibility	EMC	E9	1	1	Ø	SAE J1752/3 - Radiated Emission
Short Circuit Characterization	SC	E10	3	10	Ø	AEC Q100-012
Soft Error Rate	SER	E11	1	3	Ø	JESD 89-1/2/3
Process Average Testing	PAT	F1	-	-	-	AEC Q001
Statistical Bin/Yield Analysis	SBA	F2	-	-	-	AEC Q002

*Product Grade Definition

	Operating temperature range	
Grade 0	-40°C	+150°C
Grade 1	-40°C	+125°C
Grade 2	-40°C	+105°C
Grade 3	-40°C	+85°C
Grade 4	0°C	+70°C

Source: AEC-Q100 Specification

Temperature Cycling (TC)

This test highlights the differences in the coefficient of thermal expansion of package materials with Cu along with the increased hardness of Cu with respect to gold (Au).

Perform per the test requirements in AEC-Q100/Q101. The only exception is for Q100 Grade 0 as shown below:

> **Grade 0**: -55°C to +150°C for 1500 cycles or equivalent for step 6 (Stress 1X) of Table 3 and 3000 cycles for step 11 (Stress 2X) of Table 3.

Biased Humidity (HAST/THB/H3TRB)

This test can exacerbate corrosion along the Cu/bond pad intermetallic compound (IMC) interfaces.

Perform per the test requirements in AEC-Q100/Q101.

High Temperature Storage Life (HTSL) / High Temperature Gate Bias (HTGB) / High Temperature Reverse Bias (HTRB)

This test can accelerate IMC growth along the Cu/Aluminum (Al) interface to yield an open bond failure. It can also degrade the mechanical performance of the stitch (wedge/second bond) bond. This is especially important for high temperature applications.

Perform per the test requirements in AEC-Q100/Q101.

Source: AEC-Q100 Specification

Wire Bond Integrity

The tests described below and where they are performed are a good gauge of the bond strength and weld formation of the ball and stitch bonds. They are done to demonstrate adequate process control with acceptable bond integrity. The location of the hook for bond pull should be over the contact of interest (i.e., over the ball and over the stitch/wedge).

- Ball shear – ball bond area versus shear force (pre-packaged)
- Ball and Stitch/Wedge bond wire pull (pre-packaged)
- Perform wire pull/ ball shear on first bond and wire pull for stitch/wedge bond (post packaged)
- Pad cratering test (pre-packaged)

Wire pull / ball shear is performed after stress testing and decapsulation. A recommended process flow is described below:

Cross-Sectioning Inspection

For initial supplier qualification of a new die/package (interaction) family/technology, selecting worst-case components based on CSAM after 2X stress is desirable. The sample sizes and test conditions are specified in the overall process qualification flow shown in Tables 3a/3b.

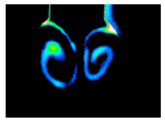
Areas of examination:

- Ball bond area
  - Amount and distribution of intermetallic - an alternative planar analysis method to evaluate ball bond IMC formation is also acceptable.
  - Crack initiation/propagation
  - Corrosion after 1X stress
- Stitch/Wedge bond area
  - Amount of contact
  - Wire angle to stitch/wedge
  - Crack initiation/propagation
  - Corrosion after 1X stress
  - Intermetallics formed in the bond area

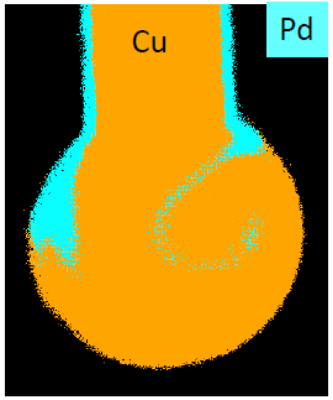
000208

Source: AEC-Q100 Specification

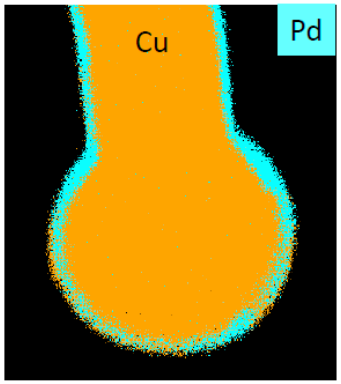
Conventional PCC vs. High Rel PCC

Category	Name	Core Purity (%)	ρ Resistivity*1	Pd distribution
Normal PCC		99.99 (4N)	1.9	
High reliability		99.99 (4N)	1.9	
Ultra High reliability		99 (2N)	2.3	

Conventional PCC



High Reliability PCC



Source: Tanaka

Cu Alloy Wire

Introduction

Benefit of Cu alloy wire

- For customer using **bare Cu** wire

1. Better 2nd Bondability
   - Wider 2nd bond process window.
   - Higher stitch pull strength.
2. Higher reliability
   - Longer HTS life.

- For customer using **Pd coated Cu** wire

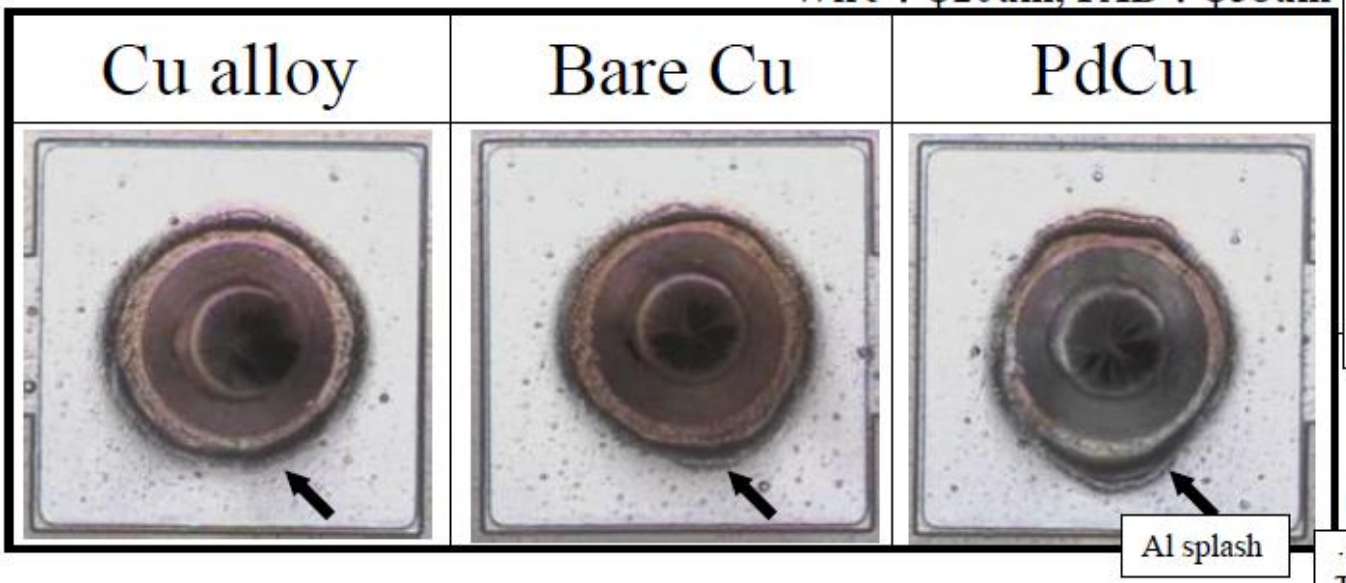
1. Cost
   - Lower cost
2. 1st Bondability
   - Less Al splash

1st Bondability-1

Observation of Squashed Ball

(1st bonding condition of All wires are same bonding parameter)

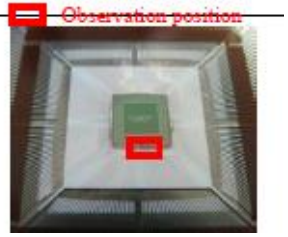
Wire : φ20um, FAB : φ38um



·Bonding condition
Wire Dia : 20um
Bonder:KnS Maxum Plus (Cu kit)
Capillary :SPT SU-25080-385F-ZU34TP
Die: TANAKA TEG Al-0.5%Cu, t=0.8um (Renesas)
Sub:QFP-200(Ag electro plating)
Bonding Temp:220℃
FAB size (Target):38um
Squasehd ball size (Target) :X,Y=48±2um,Z=11±1um
Flow Gas : N2+5%H2, 05L/min

Wire Diameters:0.79mill
FFO Fire Mode:Ball Size
Ball size:1.55(Proto-1,2,CFB-1),1.57(CLR1A)
EFO Current:70mA,EFO Gap:30mils
Tail extension:10mils

·Bond 1 Parameters
Tip:10mils ,C/V:0.3mils/ms, V Mode,USG Mode:Contact Current, USG Current:60mA, USG Bond Time:10ms, USG Pre-Bleed:55mA, USG Profile:Square, Force:20gf, Initial force:30gf,
Initial Force Time:33%, Force Ramp Time:10%, X-Scrub:3um, Y-Scrub:0um, Scrub Cycles:1, Scrub Phase:90deg, 1st Scrub Mode:Pre-USG



**Al splash of Cu alloy is almost same as bare Cu.

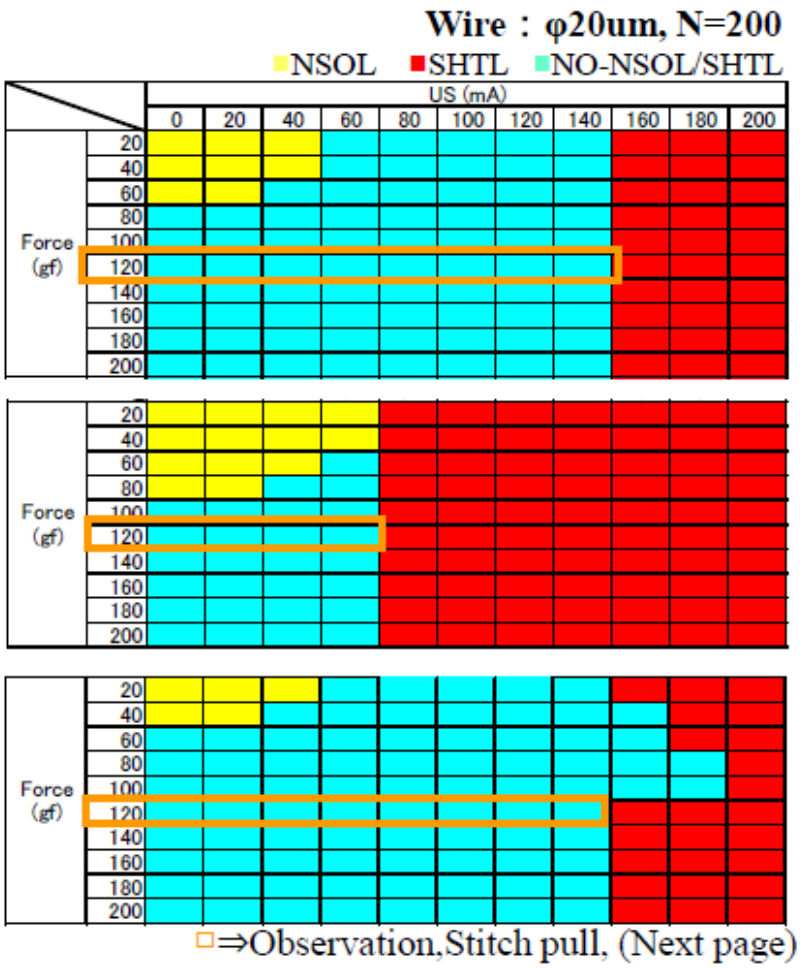
2nd Bondability-1

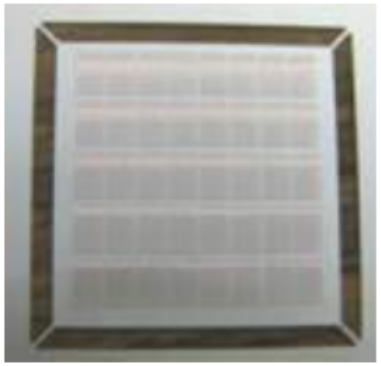
Bonding window (Ag electroplating / QFP Dummy)

Cu alloy

Bare Cu

PdCu





Bond Layout

· Bonding condition
Wire Dia : 20um
Bonder:KnS Maxum Plus (Cu kit)
Capillary :SPT SU-25080-385F-ZU34TP
Sub: Dummy substrate ,Ag electro plating
Bonding Temp:220°C
FAB size Target:38um
Flow Gas : N2+5%H2, 05L/min

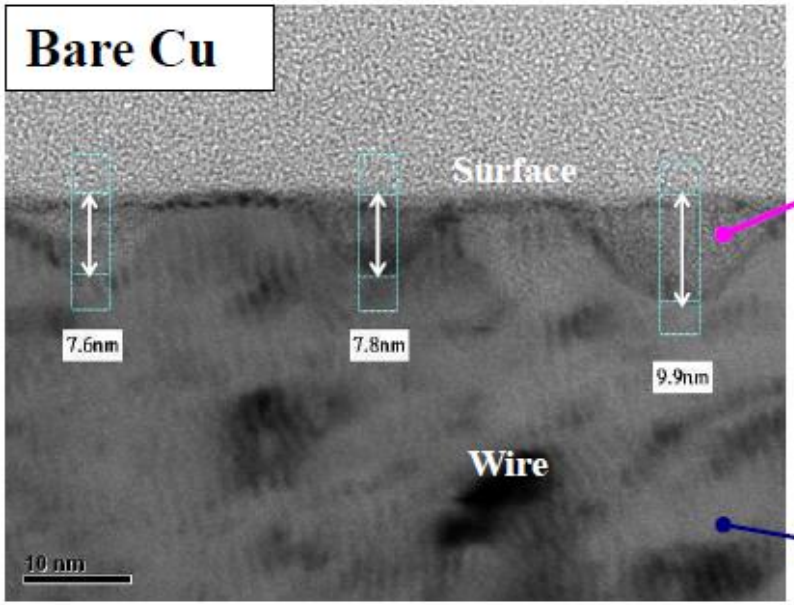
· Bond 2 Parameters
Tip:10mils ,C/V:0.5mils/ms,
Contact Threshold:70%, USG Bond Time:7ms
Power Equ Factor:100%, USG Pre-Bleed:0mA,
Init'l Force:50g,Init'l Force Time:33%
Tail XY Scrub:0um
Z-Tear USG:50mA, Z-Tear Speed:10%
Tail Scrub USG:0mA,

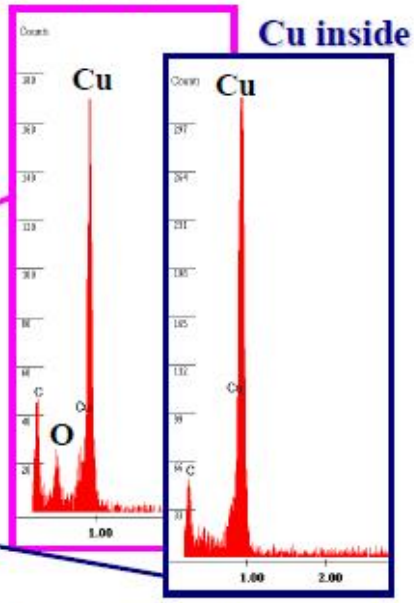
Evaluation condition
· Squashed Ball size
OLYMPUS Measuring Micro Scope STM6
Object Grass:×20
N=200

****2nd Bonding process window of Cu alloy is wider than bare Cu and PdCu.**

Comparison of Oxide film on wire surface

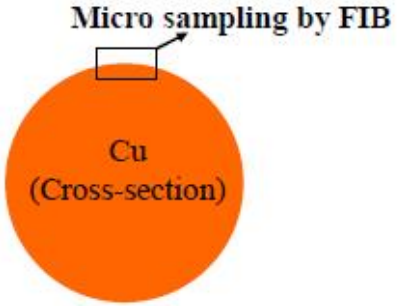
【Cross-sectional View by TEM/EDX】

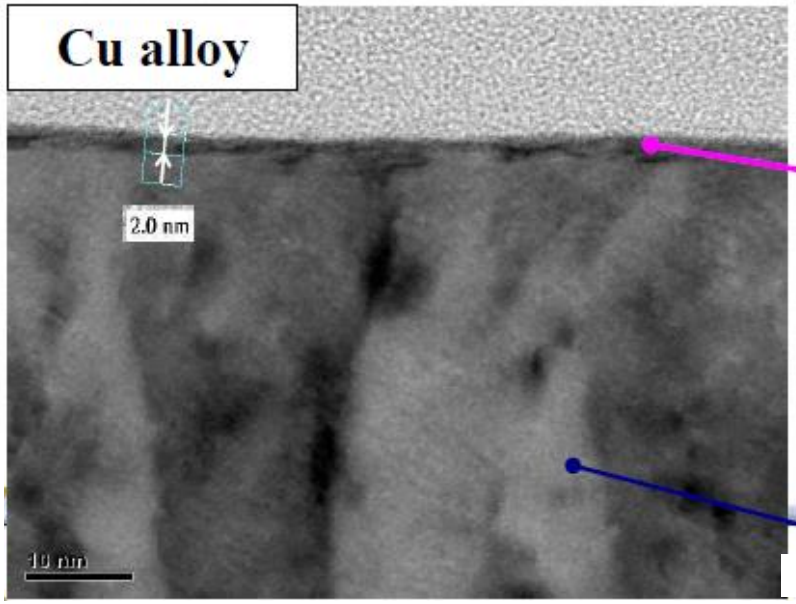


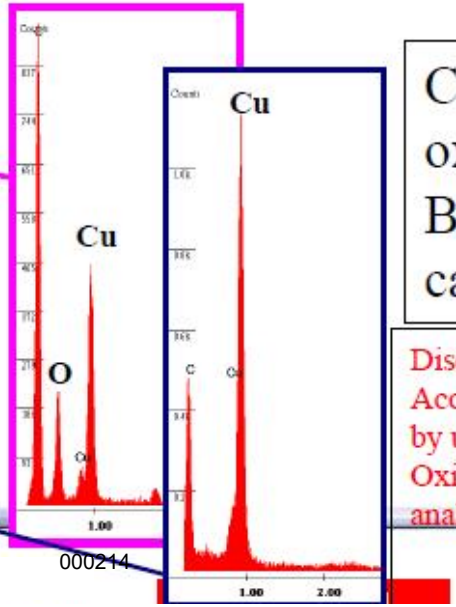


Evaluation wire : Cu alloy, Bare Cu
Wire Dia : 18mm (Cross-section)
Equipment : TEM/EDX
Magnification : ×220k

*
*The sample for observation was adjusted by FIB (Micro sampling).





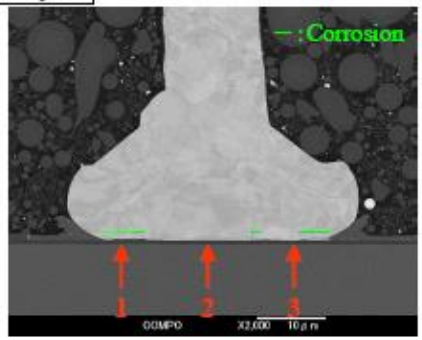


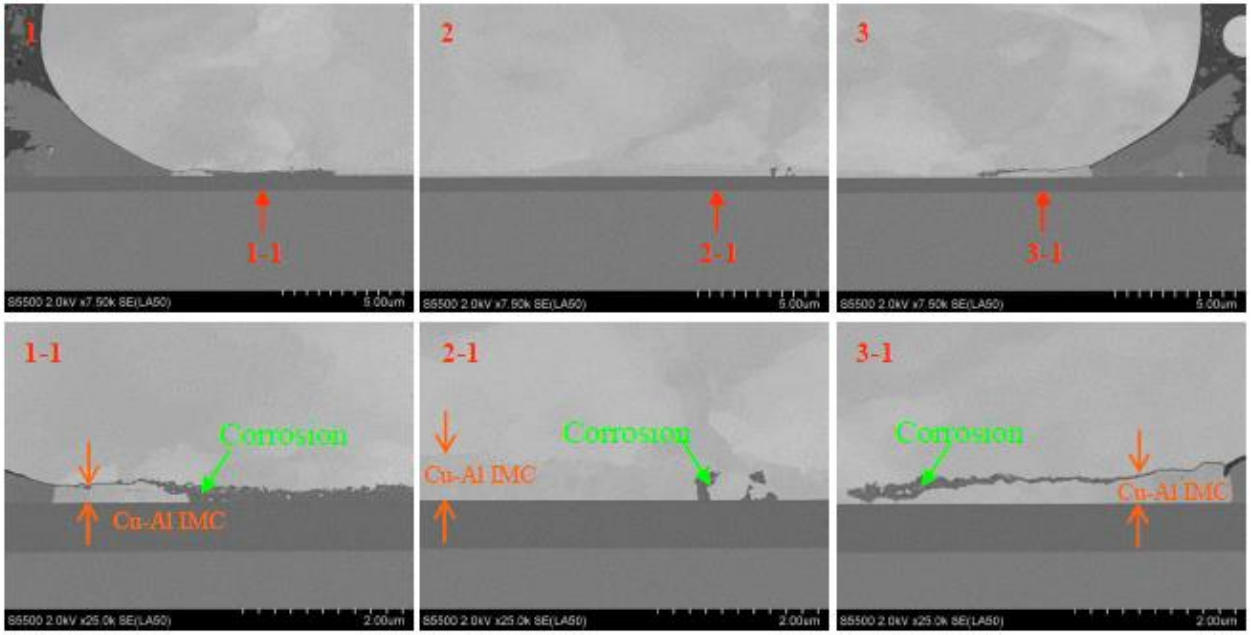
Cu alloy has a uniform oxide film thinner than Bare Cu. Alloy material can prevent oxidization.

Disclaimer:
Accuracy of TEM/EDX may be affected by unevenness of the surface.
Oxide film area is estimated from multiple analyses

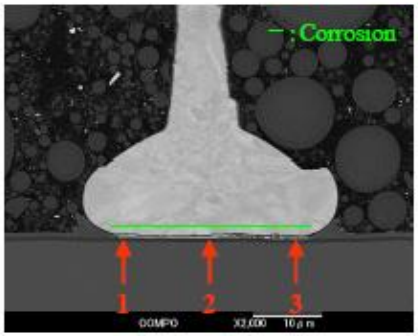
Comparison of Cu-Al inter-metallic @HTS 175℃ 1300hrs

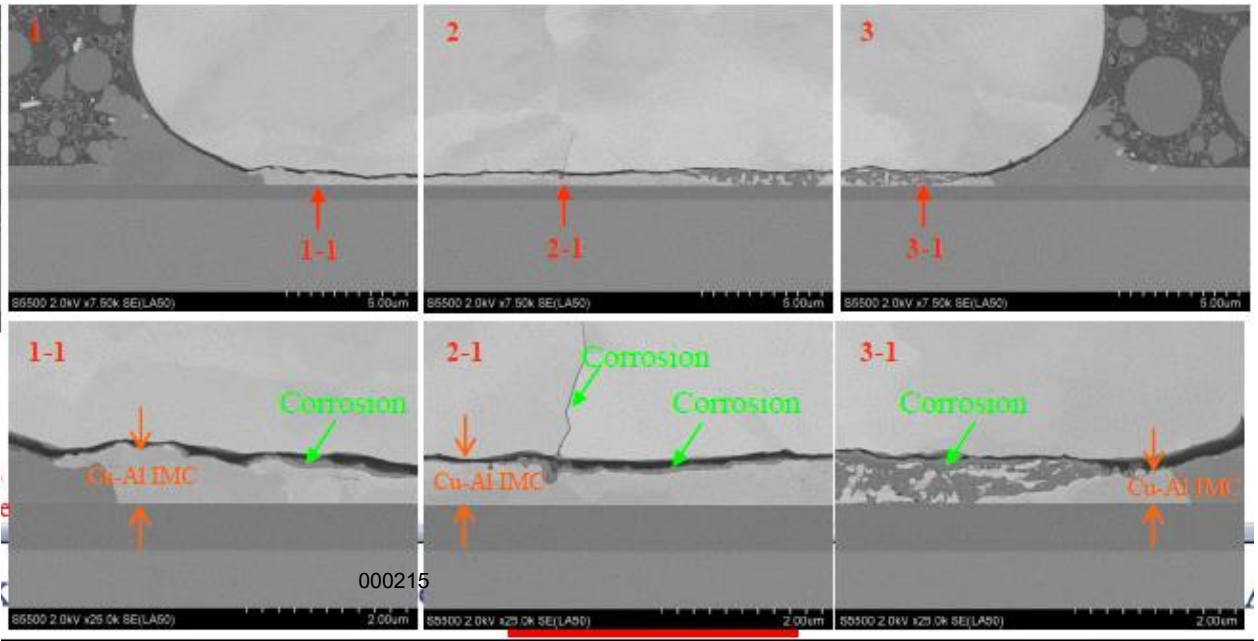
Cu alloy





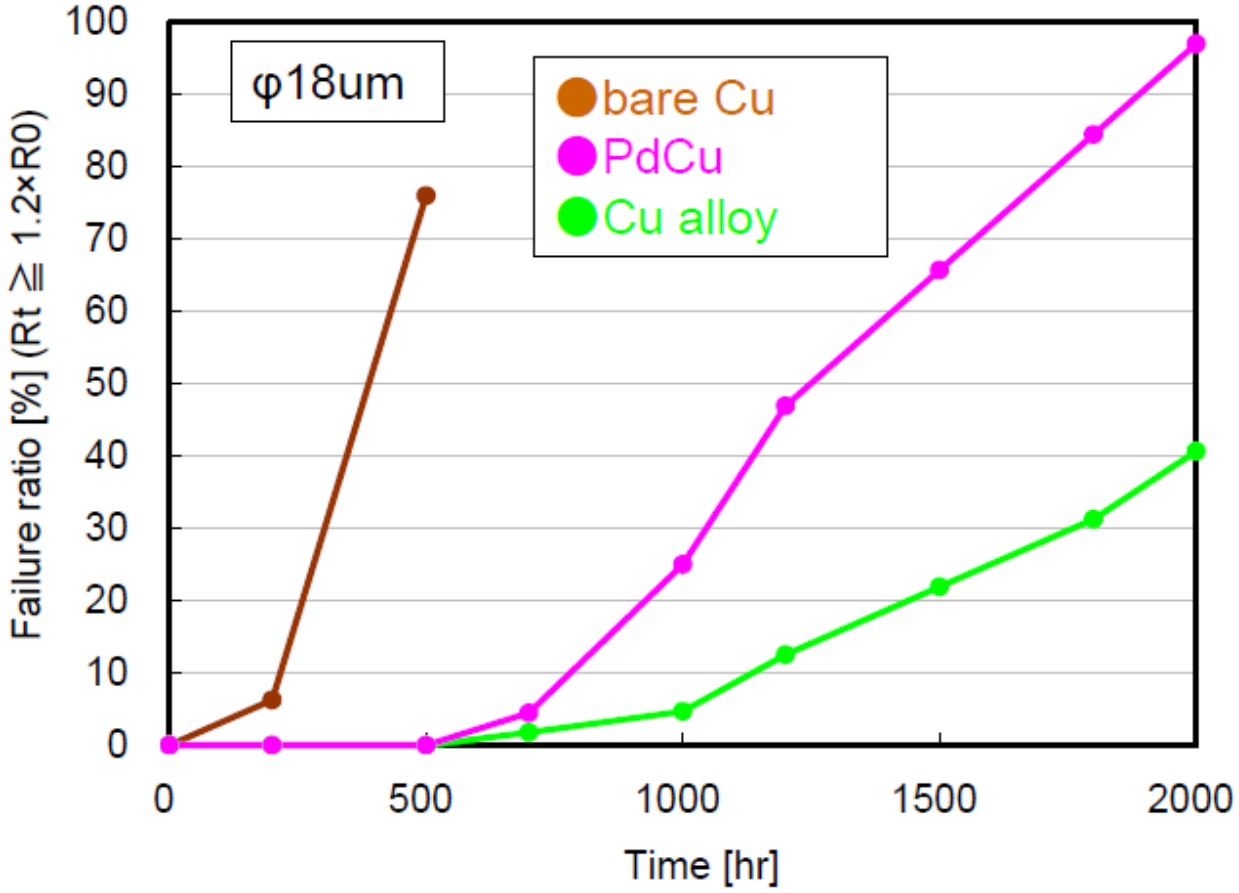
Bare Cu





Reliability Comparisons-HTSL

HTSL - 200℃ (accelerated) , BGA , Green resin



<Bonding conditions>
Bonder: ProCu
Gas flow rate:
Forming, 0.50l/min(EFO)
EFO Current: 65mA
Wire dia.: 18um
Squashed ball dia.: 36um
Squashed ball thickness: 9um
Shear stress: over 12kgf/mm2
SPT SU-23060-283F-ZU34TP

<other conditions>
Die :WALTS MB6020-0102JY,
Pad: Al-0.5%Cu, 0.8umt
substrate:OKI PBGA32pin（HF）
256point, 128circuit
(=16circuit/IC×4IC×2Frame)
Initial resistance:0.8-1.0Ω

**Cu alloy is reliability results are better than Bare Cu & PdCu wires.

Category		Pd coated Cu	Cu alloy	bare Cu
type				
Resistivity		★★★	★★	★★★
Reliability	HTS	★★	★★★	★
	HAST	★★★	★★★	★
FAB formation		★★	★★	★★
1st bondability		★	★★	★★
2nd bondability		★★★	★★	★
Price		★	★★	★★★

Thank you !

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