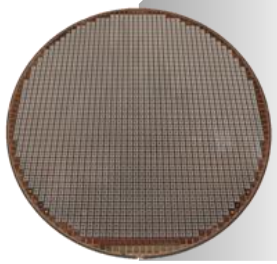
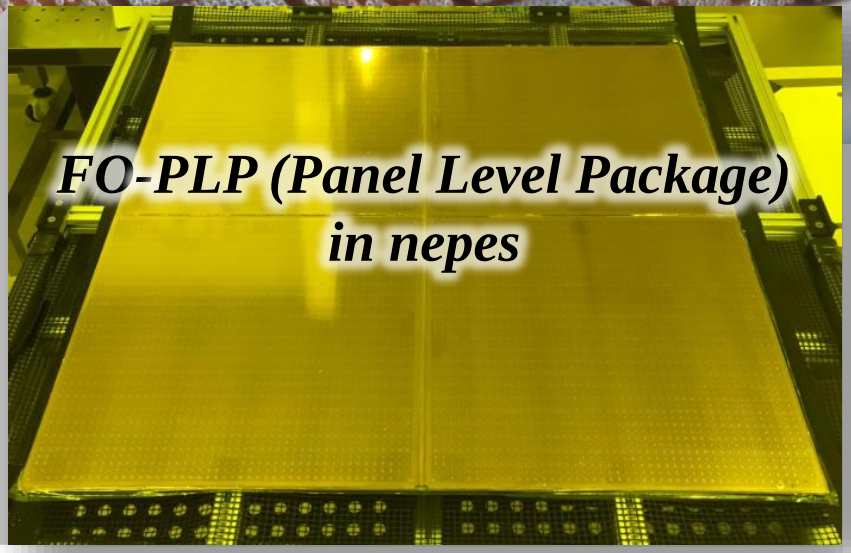
nepes corporation

Trends in FOWLP: 600mm Panel Level for 6-Sided Die Protection with M-Series

FO-WLP
@300mm round

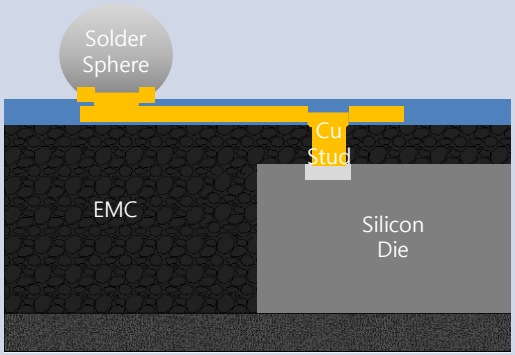
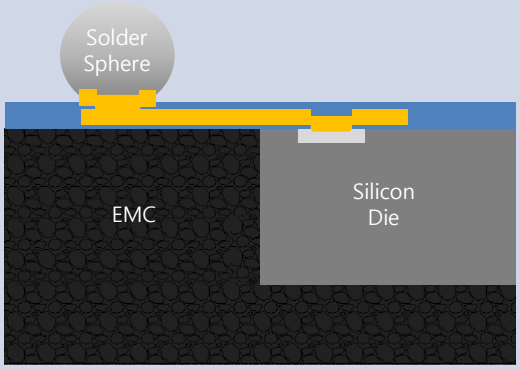
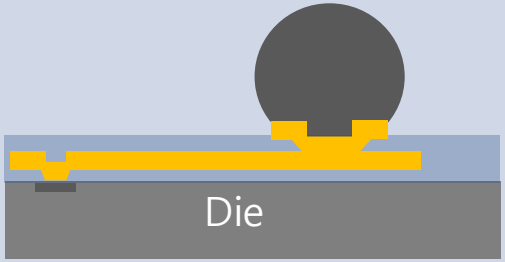


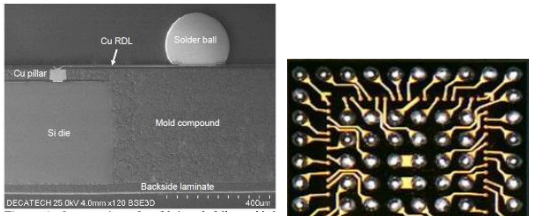


Contents

- **Wafer Level Packaging Attributes**
  - **M-Series (6-sided die protection) vs. eWLB vs. WLCSP**
- **Market Intelligence**
- **FOWLP Applications**
- **6-Sided Die Protection with Panel Level Processing**
- **Key Challenges to Address for 600mm PLP**
- **Reliability**

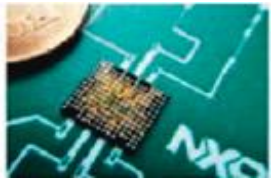
Fan-Out WLP and WLP Structure

	M-Series	eWLB	WLCSP
Package Structure			
Features	• Cu stud + Fully encapsulated PKG • Adaptive Patterning™ → Die Drift • Backside Protection	• 5 sided protection with MC	• Package Size = Die Size • Pitch of interconnect is limited by die s ize • Backside laminate option is available
Process	• Cu stud needed • Create GDS file per panel • Backside Laminate	• Warpage adjust for critical process step	• Standard thin film processing
Die Drift Control	• Low Accuracy Chip Attach Process & Ad aptive Patterning™ • Pitch Compensation	• High Accuracy Pick and Place Process • Pitch Compensation	• None
Warpage Control	• Use of Backside Laminate	• Warpage Adjust for critical process steps	• None



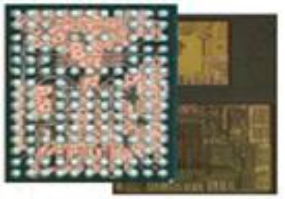
Source: Deca Technologies

Radar Module



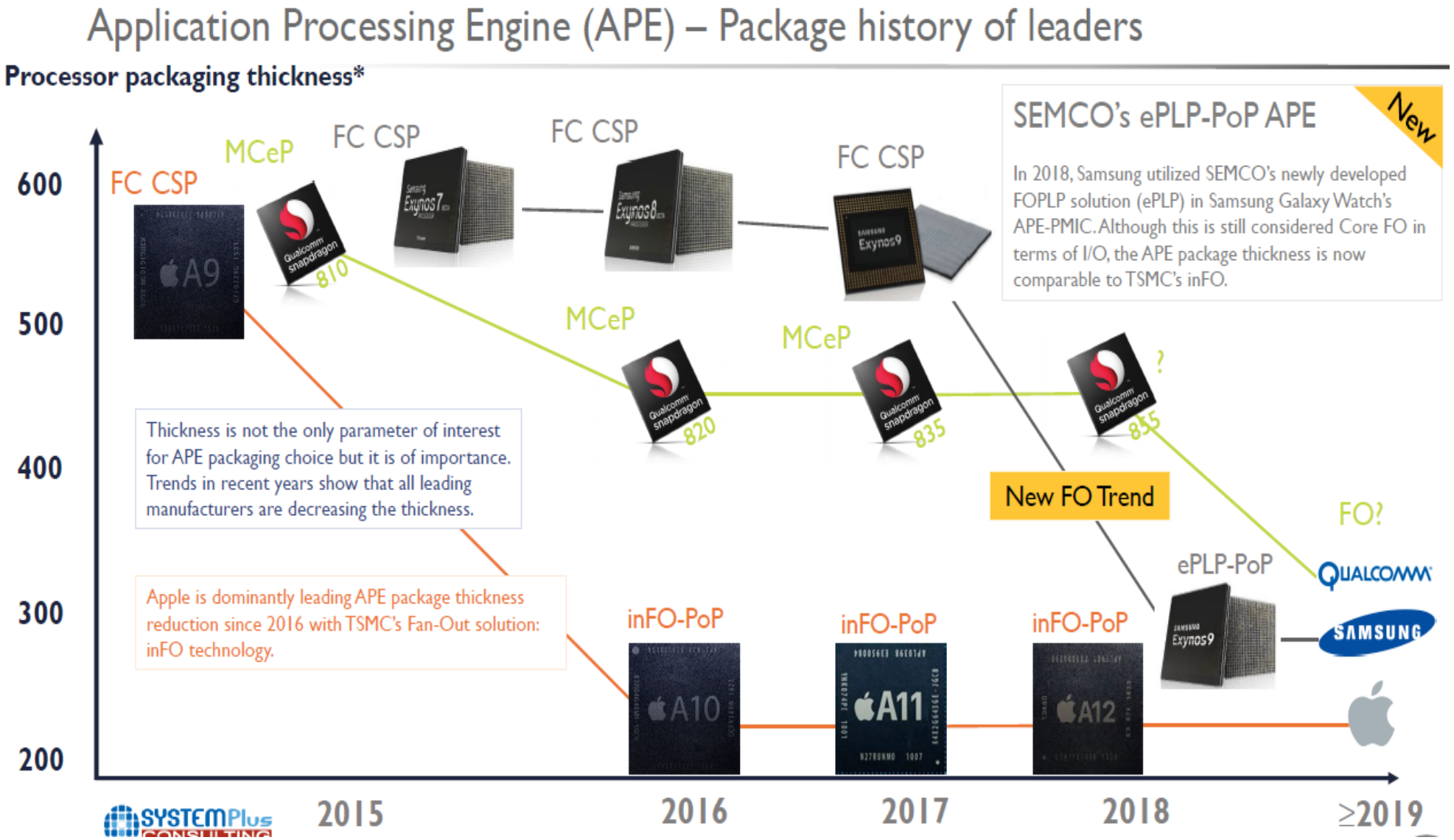
Source: NXP

Marvell PMIC & Audio CODEC



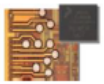
Source: Nanium/Marvell

Fan-Out End Applications – Application Processing Engine



Source: Yole 2019

Fan-Out Potential for Volume Products

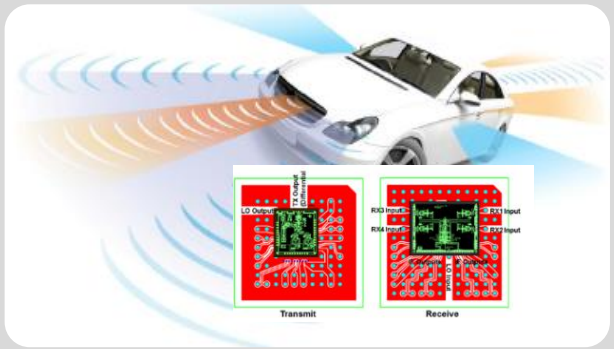

Products	Wireless Basebands SoC	PMU/PMIC	RF Connectivity (Transceivers/Receivers)	Audio & Video codecs	APE
Motivations/drivers for Fan-Out	• Lower cost when shrinking to smaller nodes • Supply chain simplification • Electrical performance	• Thermal performance (>20% increase vs BGA) • Package thickness	• Electrical performance/ speed • Miniaturization	• Lower cost • Low thickness	• Lower cost if high yield is achieved • Lower thickness • High electrical performance
Limitations & challenges for Fan-Out	• Changing from mature package platform • Package IC co-design environment • MCP/SiP platform required in the future	• Changing from mature package platform • Thickness of RDL to carry high current • MCP/SiP platform required in the future	• Changing from mature package platform • Integration of thin-film passives • MCP/SiP platform required in the future	• MCP/SiP platform required in the future	• Changing from mature package platform • Price (PoP capability at high yield vs FC BGA is still questionable)
Type of SoC integration	BB + GPS + FM + others	PMU + Audio + video + USB + others	• Multiband transceivers • Combos of BT, WLAN, FM, GPS, NFC, MCU…	SoC → Two-chip module	APE + Memories
I/O numbers	200–300	100–300	36–200	60	>1500
Package body size	5x5mm² → 8x8mm²	5x5mm² → 8x8mm²	4x4mm² → 8x8mm²	3x3mm², 4x4mm²	15x15mm²
Fan-Out configuration	Single Die FO → FO-PoP	Single Die FO → FO-SiP/MCP	Single Die FO → FO-SiP	Single Die FO -> FO-SiP/MCP	FO-PoP → FO-SiP
Packaging competition	Flip-Chip, WB-BGA	WB-BGA, Flip-Chip, WLCSP	Flip-Chip	WLCSP	Flip-Chip, MCeP
Commercialization/ time to market	Commercialized	Commercialized	Commercialized	Commercialized	Commercialized
Key potential customers	Qualcomm, Marvell, Broadcom, Spreadtrum, STMicroelectronics, Mediatek	Qualcomm, TI, Maxim IC, Dialog Semi, NXP, STMicroelectronics, Cirrus Logic	Broadcom, TI, Qualcomm, Marvell, STMicroelectronics, Qualcomm, NXP	NSC, Cirrus Logic, Dialog Semi, Maxim IC, NXP, TI, Rohm	Apple, Qualcomm, Samsung, Mediatek

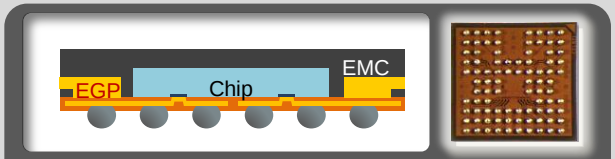
Source: Yole 2019

FOWLP/ FOPLP : Other Market Applications

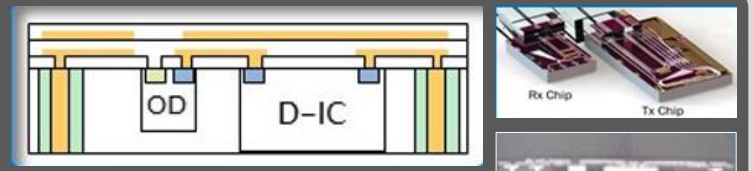
Automotive

Advanced Driver Assistance System





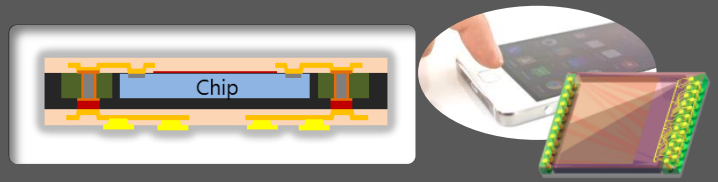
- **ADAS Radar Sensor**
  - RF Performance (77GHz)
  - Thermal Dissipation
  - High Reliability



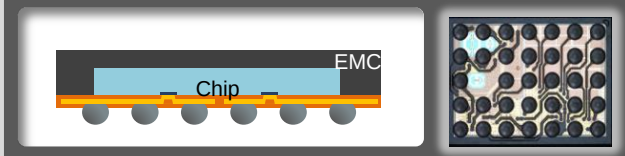
- **Photonics**
  - Low cost & Easy Optical Alignment

Consumer

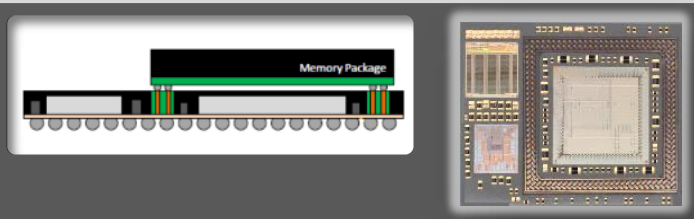
Smartphone, IoT, Wearables



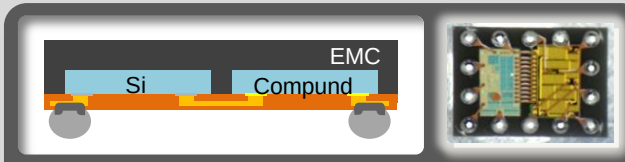
- **FPS, Bio & Medical Sensor**
  - Face-up, Via-frame, Open Cavity



- **RF, Power, Audio, etc.**
  - Performance, Form factor

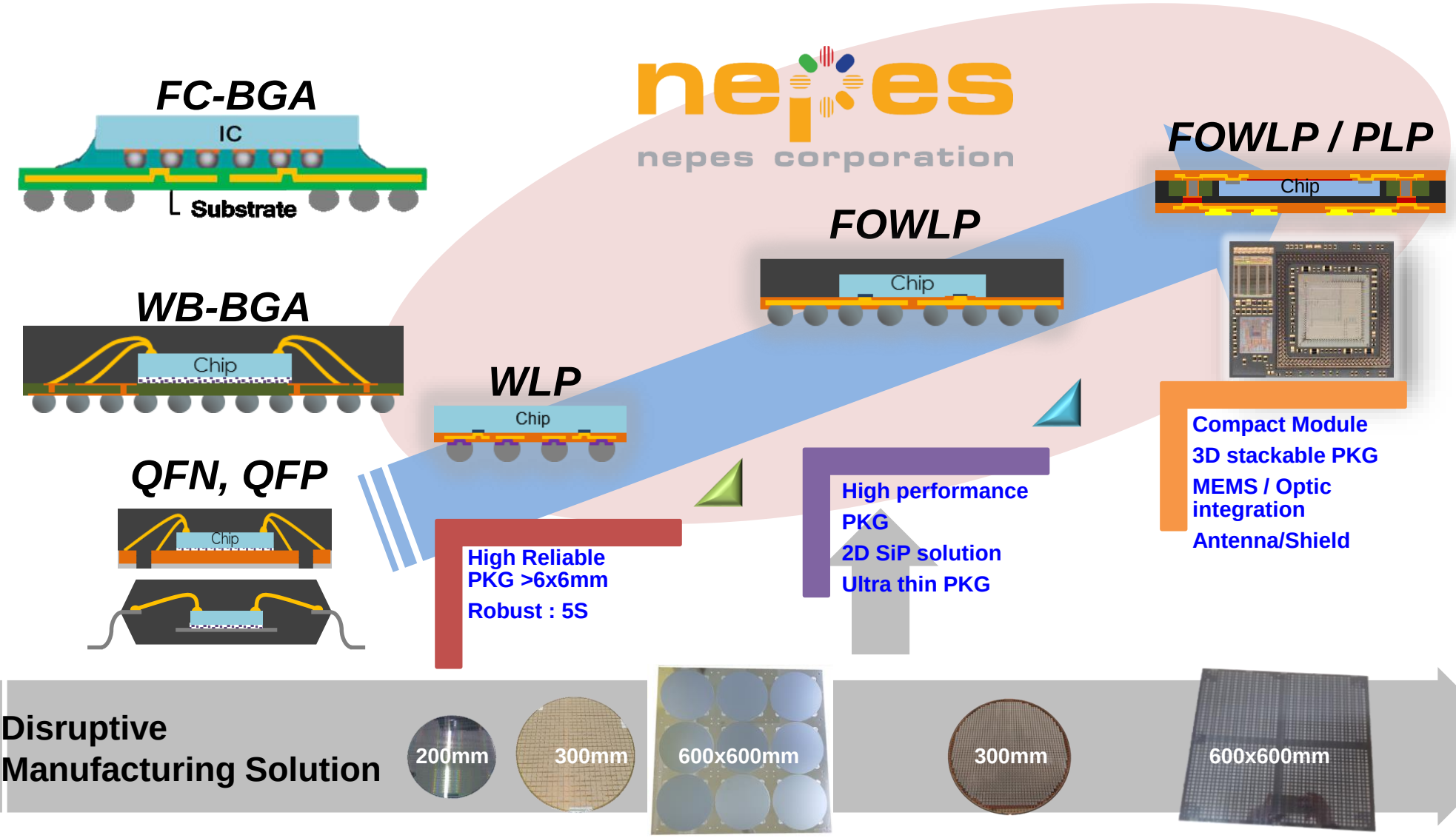


- **System in Package**
  - Multi-Die, Passives, 4 RDL Layers



- **Antenna Switch**
  - Multi-chip Integration
- **Bluetooth Low Energy**

Package Technology Trend



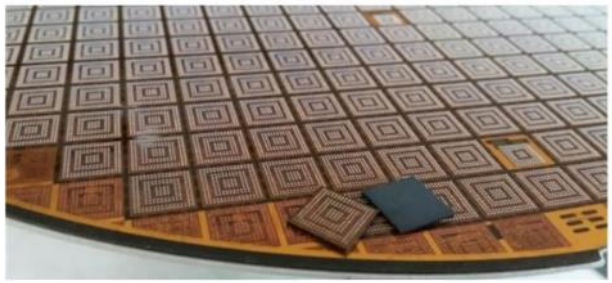
Panel Level Package : Overview

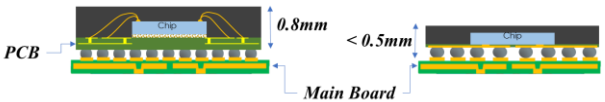
Process innovation

- **Hybrid Process Technology (Fan Out + LCD line@nepes factory)**

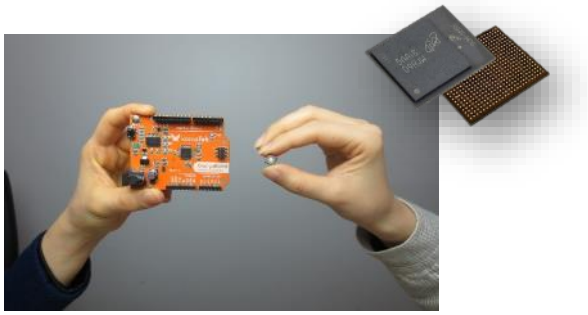
  Scale up **Fan-out WLP** to Panel Level Package

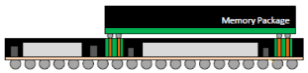
Slim & Performance



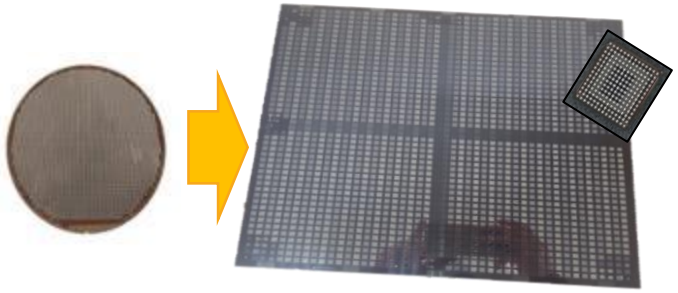


Integration

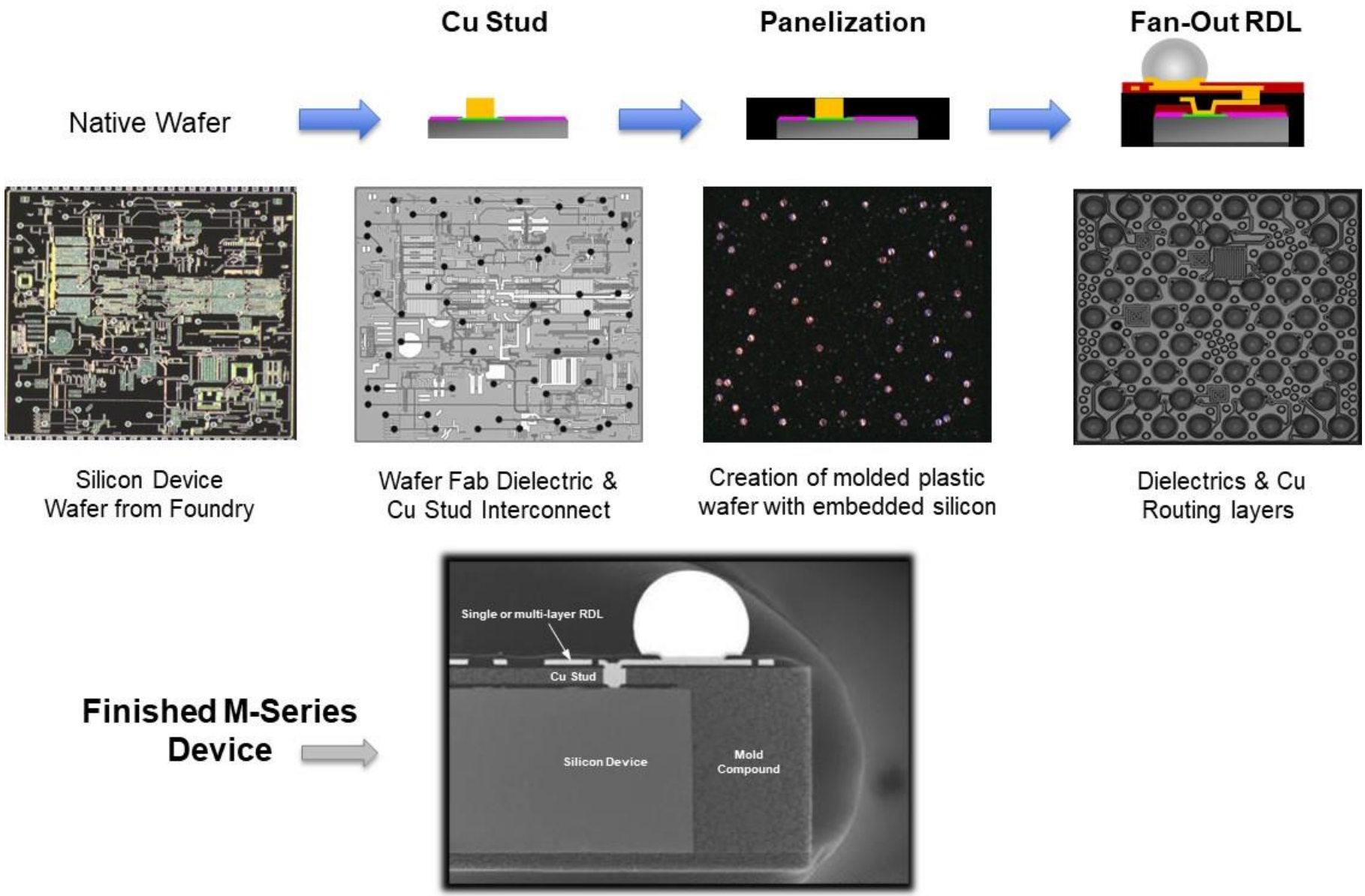




Scale up

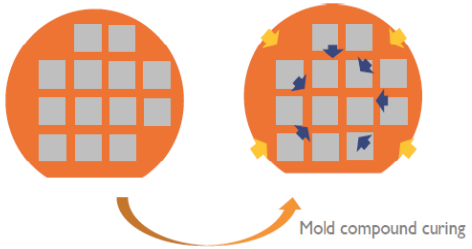


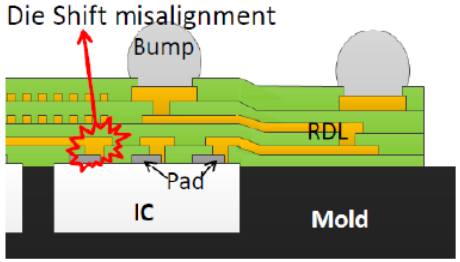
M-Series: Key Process Flows with 600mm PLP



FOWLP Key Challenge #1: Die Drift

Die Drift





Mold compound shrinks when curing

Known Good Dies shift as a result

Pick & Place
- Die position error

Molding
- Shrinkage
- CTE mismatch

Quality
- Yield
- Fine Al pad
- MCP/SiP

Table I: Magnitude of the worst-case die shift caused by 0.3° rotation for several package sizes, assuming the die is centered in the package.

Package Size (mm)	Shift from Rotation (μm)
3.3 x 3.3	10.4
3.5 x 3.5	11.1
6.2 x 5.4	19.6
8.0 x 8.0	27.8
9.9 x 9.9	34.8

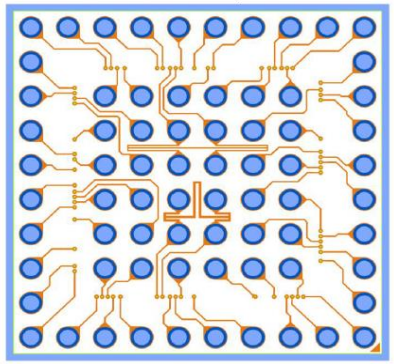
M-Series Solution:

- Bond Pitch Compensation
- Adaptive Patterning ™

→ automatically corrects for perfect connection to each device

Adaptive Routing

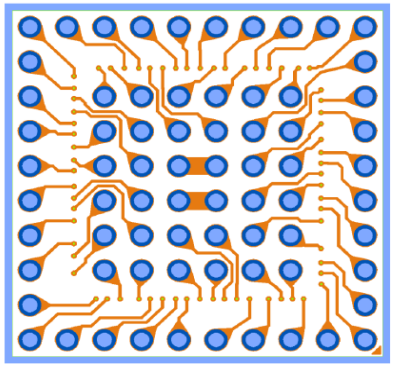
Dynamically adapt RDL routing to the measured die position



BGA array fixed to package outline
Enables multi-die fan-out

Adaptive Alignment

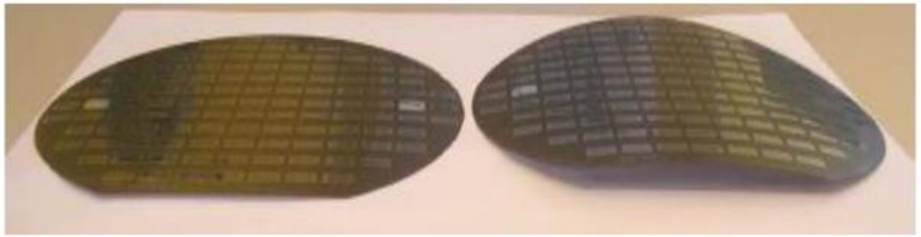
Align the entire RDL pattern to the measured die position

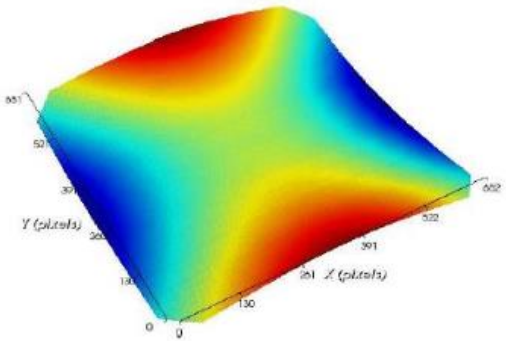


BGA array fixed to package outline
Precisely aligns inductors to the die

FOWLP Key Challenge #2: Warpage

Panel/Package Warpage





Source: Akrometrix

Molding
- •CTE mismatch
- •Die to EMC ratio

Warp
- •Magnitude
- •shape

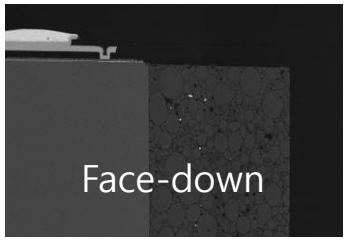
Quality
- •Yield
- •Fine Al pad
- •Die stress

M-Series Solution:

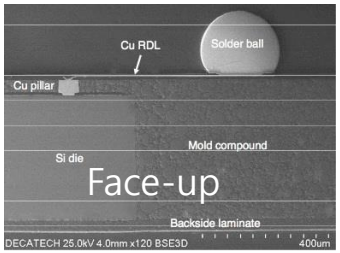
- Use of Backside Protection
- Optimize Warpage Control for Panel Processing with 600mm PLP leverage LCD Best Known Practices

FOWLP Key Challenge #3: Fine Line/Space

Fine Geometry L/S



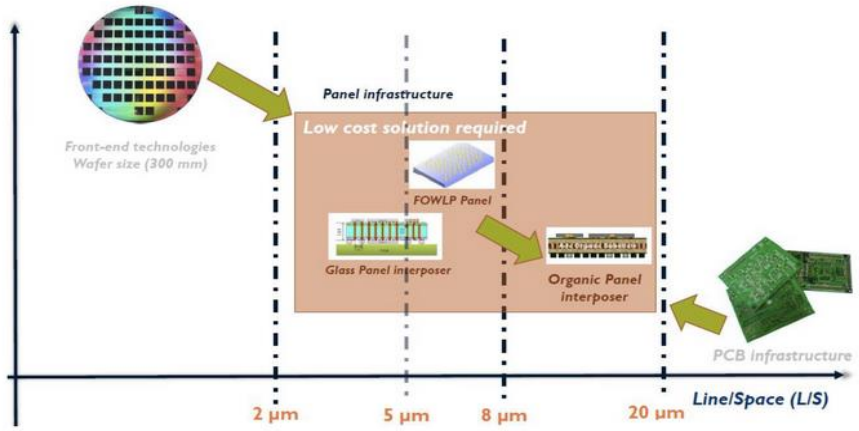
VS



Warp
- Magnitude
- shape

Topography
- Die to EMC transitions

Quality
- Yield
- Fine L/S
- Multi layers

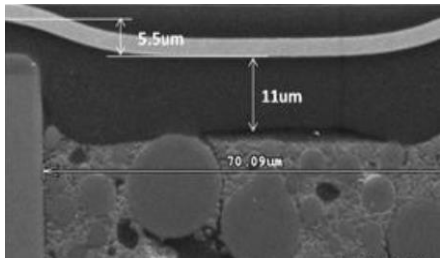


M-Series Solution:

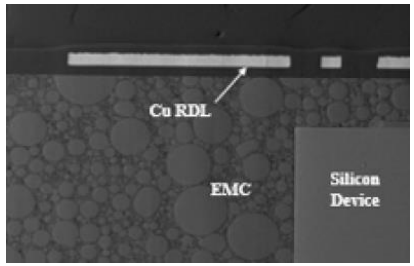
- Chip-first & Face-up
- L/S: 8/8um (HVM); 5/5um (pending release); 2/2um (roadmap)
- Planarized structure

→ Eliminates the discontinuity from the active device surface to the EMC surface resulting in non-planarity of the first dielectric layer

eWLB – Chip Face-Down



M-Series – Chip Face-Up



FOWLP Key Challenge #4: Reliability Performance

Reliability performance

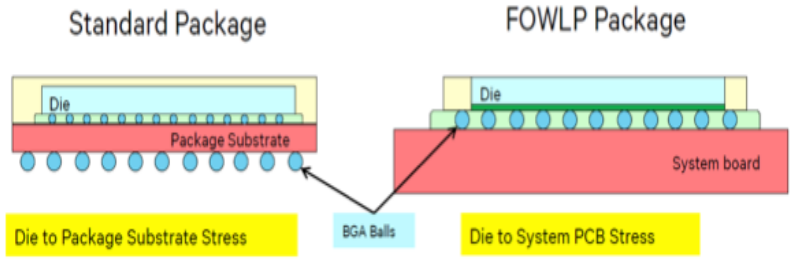
FAB
- ULK <28nm
- CBI : chip stress, electrically

Chip-PKG-Board
- Co-design
- Right material selection (UF)

Quality
- Reliability
- Electrical performance

Chip Package Interaction Stress is dominant on Standard Package
- Package Substrate, C4 Bumps, Underfill and Mold Compound
- Package substrate isolates die from System Board

Chip Board Interaction Stress is dominant on FOWLP Package
- Thin package, no substrate, soft materials
- Stress driven primarily by System Board and Board Level Underfill
- No package substrate to shield the die

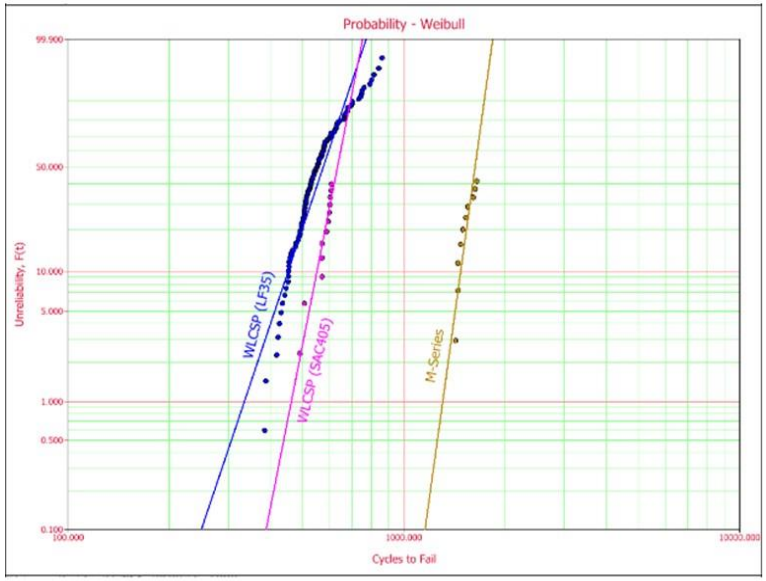


M-Series Solution:

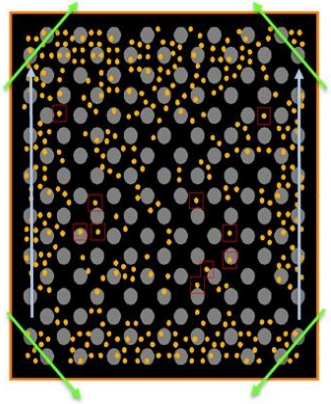
- Package information: 6.25x6.25mm, 0.5mm, non-UBM
- BLR: TC no failure up to 1000 cycles

Exceptional BLR

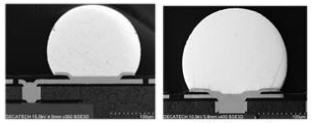
>200% improvement over WLCSP



Same 6x6 mm test chip in WLCSP and in 6.25 x 6.25mm package, All 0.5mm thick
Board level temperature cycle on JEDEC 1mm board, SAC 405



Zero dummy bumps & zero exclusion zones allows greatest miniaturization

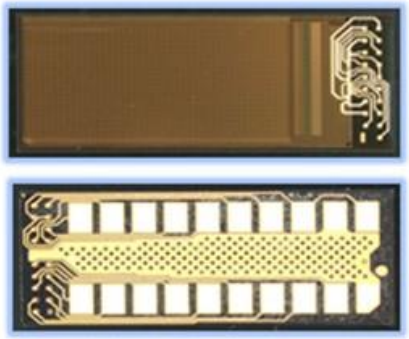


Shadow ball | Via in pad

PLP 600mm Reliability Summary Continued – Larger Body

Package Information

nPLP(FOPLP : double-sided RDL)				
PKG Size		9.37x3.98x0.2mmt	I/O	Ball array : 2 x 10
Build-up (Front/Back)	RCF	6um	LGA	10um, Cu/Ni/Au
	RDL	4um, Cu	Pitch	Pitch : 1.0mm
	PSV	5um		Size : 0.80x0.50mm

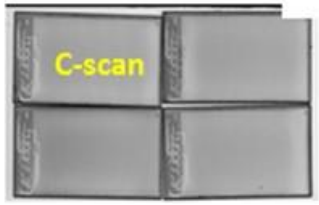


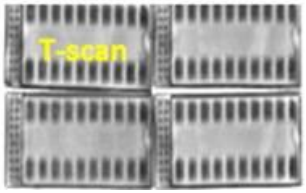
Reliability condition for Package level

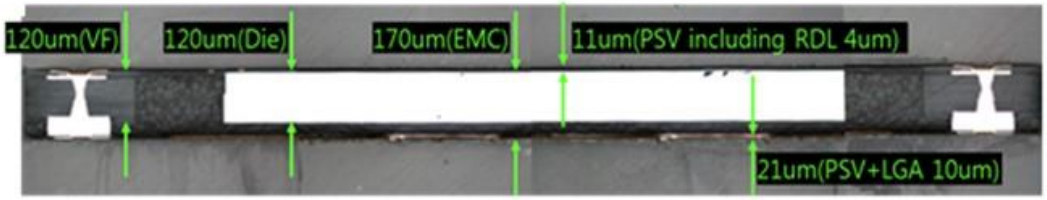
Test	Specification	Condition	Duration	Sample Q'ty	Result*
Pre-condition	J-STD-020E	MSL2	-	90	Passed
Long Term TC (after pre-con)	JESD22-A104E	Condition B (-55℃~125℃)	1000 cycles	45	Passed
Long Term u-HAST (after pre-con)	JESD22-A118B	Condition B (110℃/85% RH)	264 hrs	45	Passed
Long Term HTS (without pre-con)	JESD22-A103E	Condition B (150℃)	1000 hrs	45	Passed

✓ * : Pass/Fail Before & After test confirmed through VI, SAT and Section & SEM analysis.

Post TC1000cycles







Panel Level Package : Solution

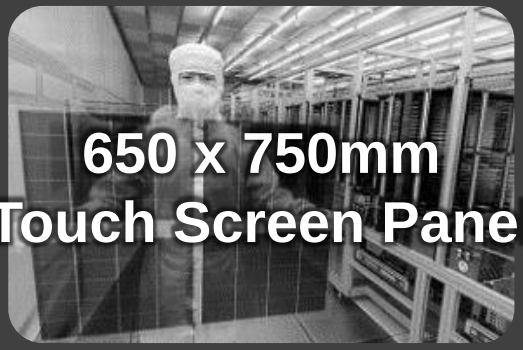
- **Hybrid Process Technology between FOWLP & LCD**
- **Advanced packaging platform with cost competitiveness**

FO-WLP since 2009

- **Core technology know-how**
  - Die drift or Warpage Control
- **Wafer-level experience since 2001**
  - 150mm, 200mm, 300mm
  - Process know-how (Bumping, RDL)
- **Fan-Out Package R&D records**
  - SiP, 4 metal layers, 2 sides RDLs

FO-PLP

LCD Panel since 2011



- **4th Gen. Process infrastructure**
  - 650x750mm
- **LCD process know-how**
  - Panel Handling, Vacuum control, etc.
- **Proven film process technology**
  - Dry film PR, Thin-film tech.

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Thank you

To Him who alone does great wonders, His love endures forever. Psalm 136:4
* A dandelion means ‘Gratitude’ in the language of flowers.

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