Fan Out Wafer Level Package With Enhanced Product Reliability and Advanced Node Silicon Chip Package Integration

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Processors Package Solutions – Packaging Innovation

SECURE CONNECTIONS FOR A SMARTER WORLD

Outline

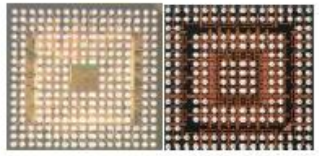
- ❑ FOWLP Introduction
- ❑ Reliability Challenges
- ❑ Developed FOWLP
- ❑ Design of Experiments
- ❑ Experimental Results
- ❑ Summary & Conclusions
- ❑ Q & A

FOWLP History and Evolution

Chip-First Face-Down Fan-Out

Early Fan-Out Activities
(long history, high volume)

Chip-First Face-Up Fan-Out



RCP creation

eWLB creation

First volume eWLB

First volume RCP

M-Series creation

RDL-First R&D

Chip-Last Fan-Out

InFO creation

HD FOWLP made possible

InFO first volume

FOPLP Milestone Achieved

ePLP first volume

2007 2008 2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019

NXP freescale

Infineon

Intel

JCET

ASE

NEPES

Amkor-Nanium

Deca Technologies

TSMC

ASE

Amkor

SPIL

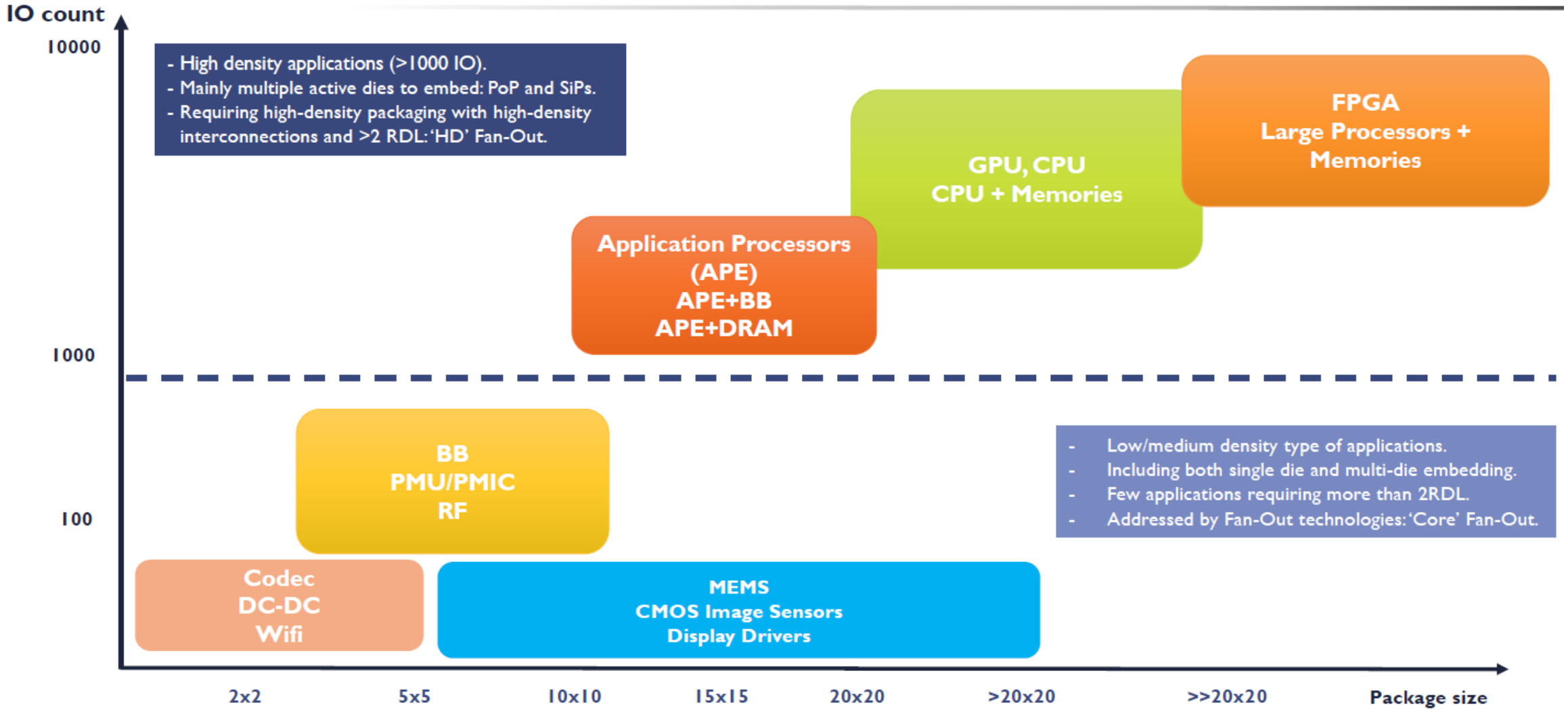
SEMCO

Powertech

NEPES

Redrawn from: Fan Out Packaging 2019 – Technologies and Market Trends report, Yole Development, 2019

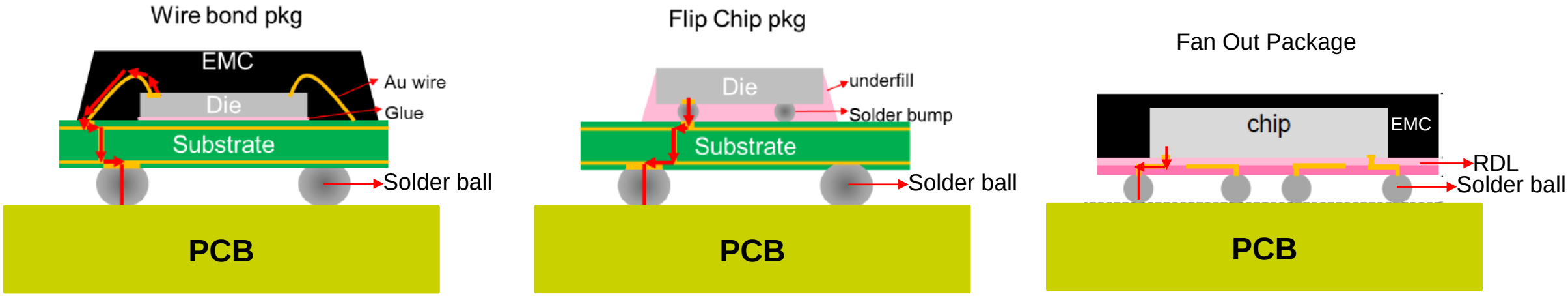
Potential FOWLP Product Applications



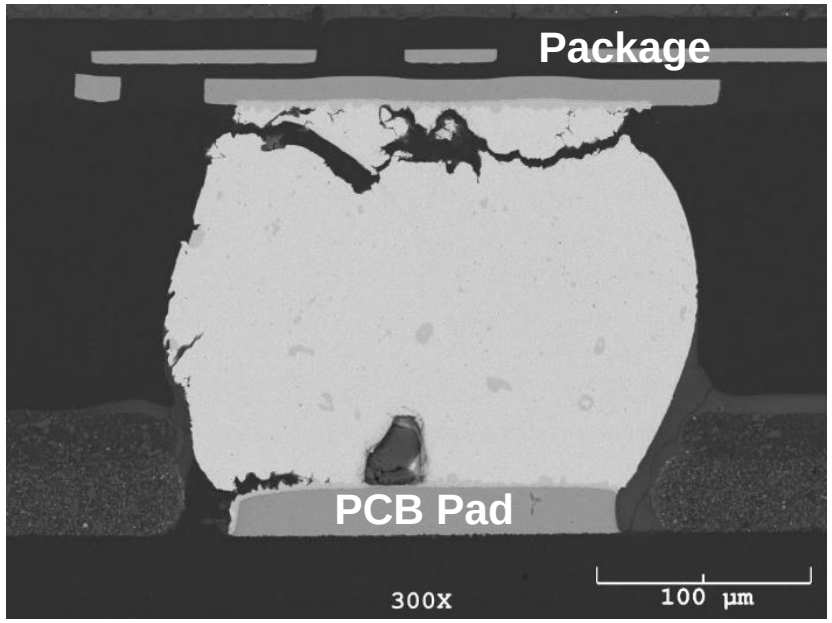
Source: Fan Out Packaging 2019 – Technologies and Market Trends report, Yole Development, 2019

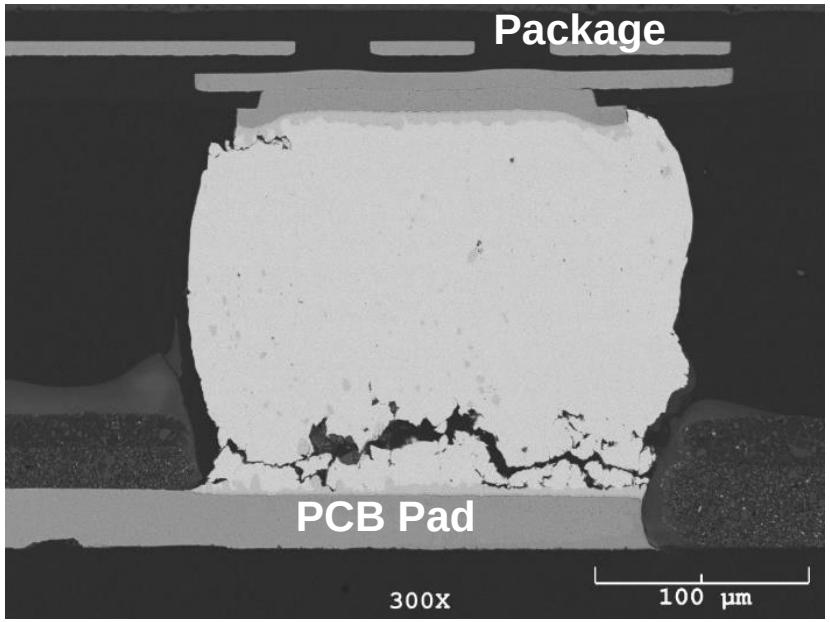
FOWLP BLR-TC Reliability Challenges – 1/3

- Unlike wire bond and flip chip packages, FOWLP have no substrate and are directly assembled on PCB
- During BLR-TC there is significant solder ball joint stress between package/PCB due to their CTE mismatch

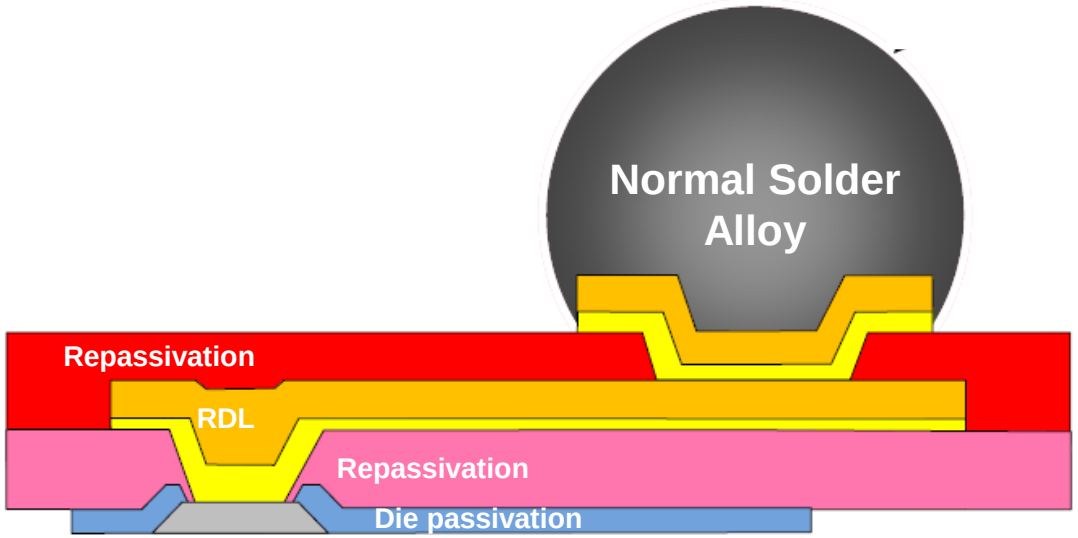


FOWLP BLR-TC Reliability Challenges – 2/3





- Primary failure modes are bulk solder joint cracking at package, PCB interface



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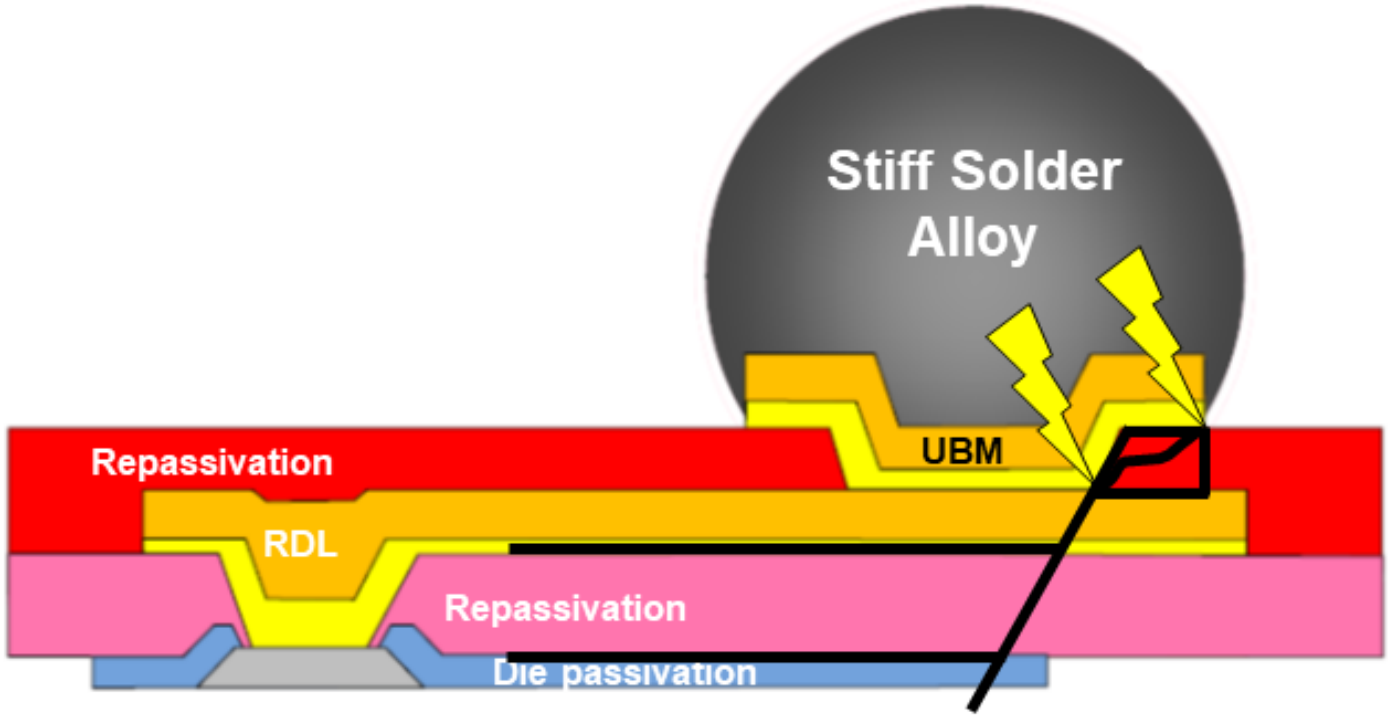
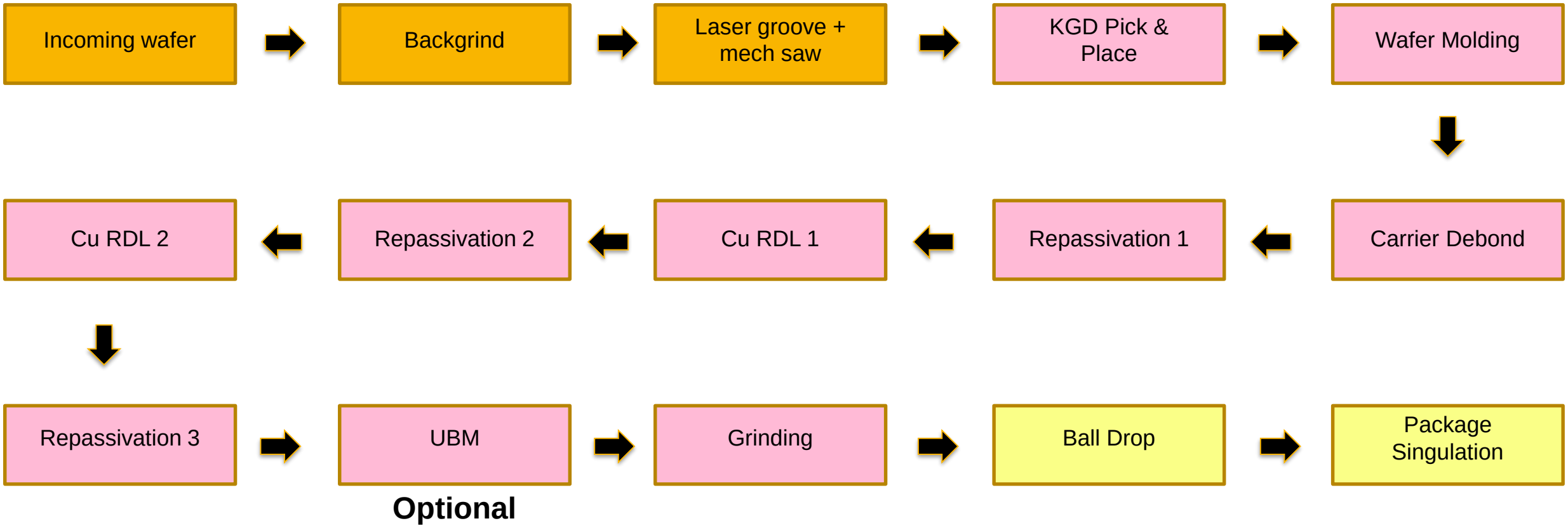
FOWLP BLR-TC Reliability Challenges – 3/3



Potential Failure Modes

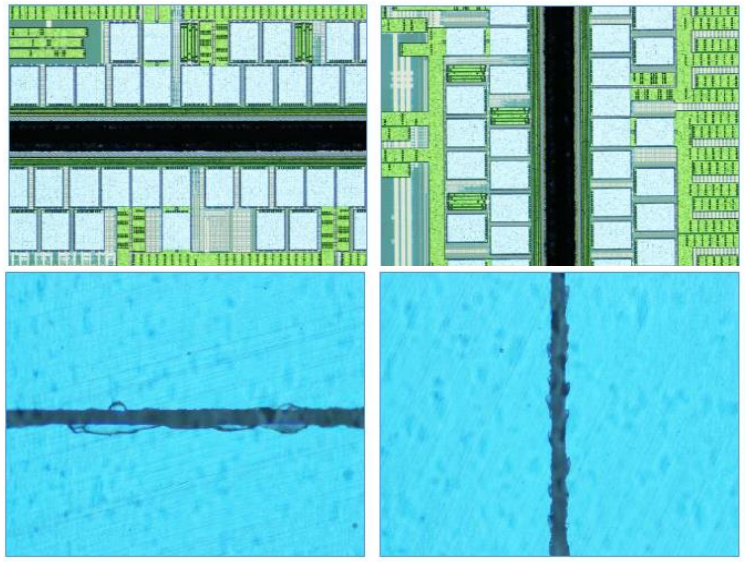
- Delamination between UBM and repassivation
- Repassivation crack => RDL crack
- Delamination between repassivation and RDL layer
- Repassivation crack => delamination between repassivation and die passivation
- Repassivation crack => die passivation crack => BEOL crack

FOWLP Process Flow

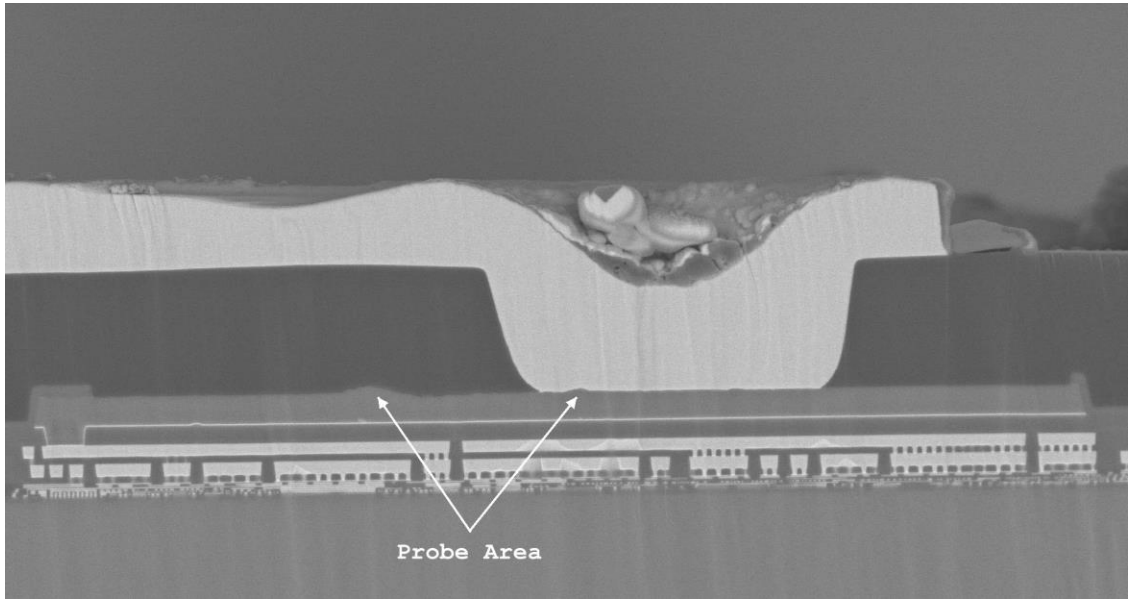


FOWLP Process Optimization

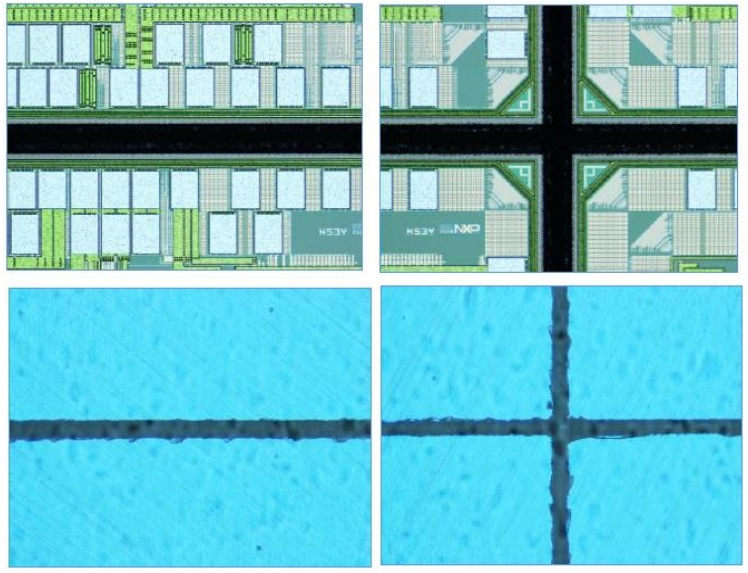
LG + saw at high metal density location



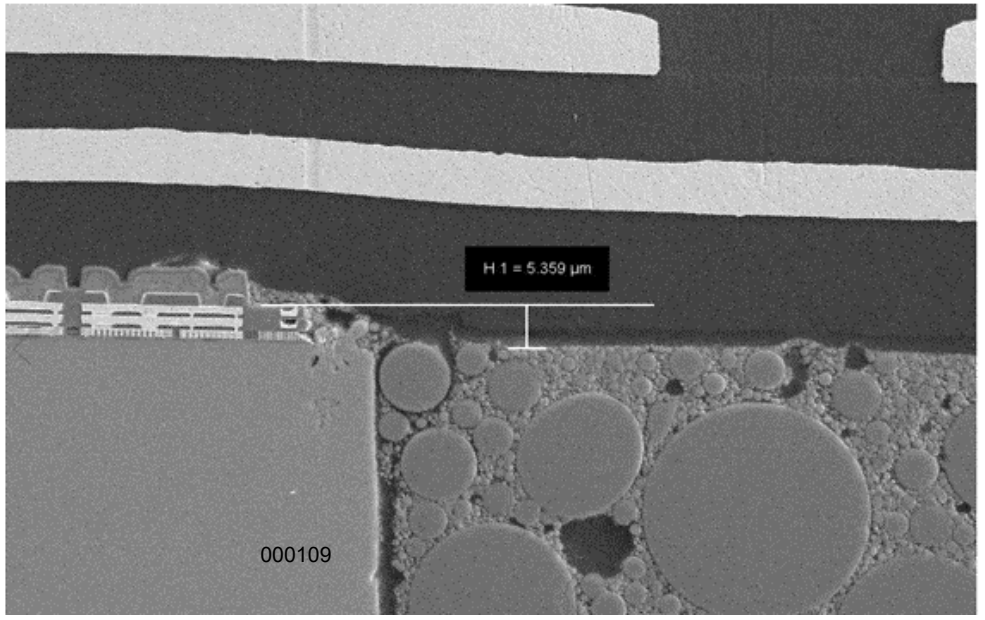
RDL over probe interface (9x tri temp probe)



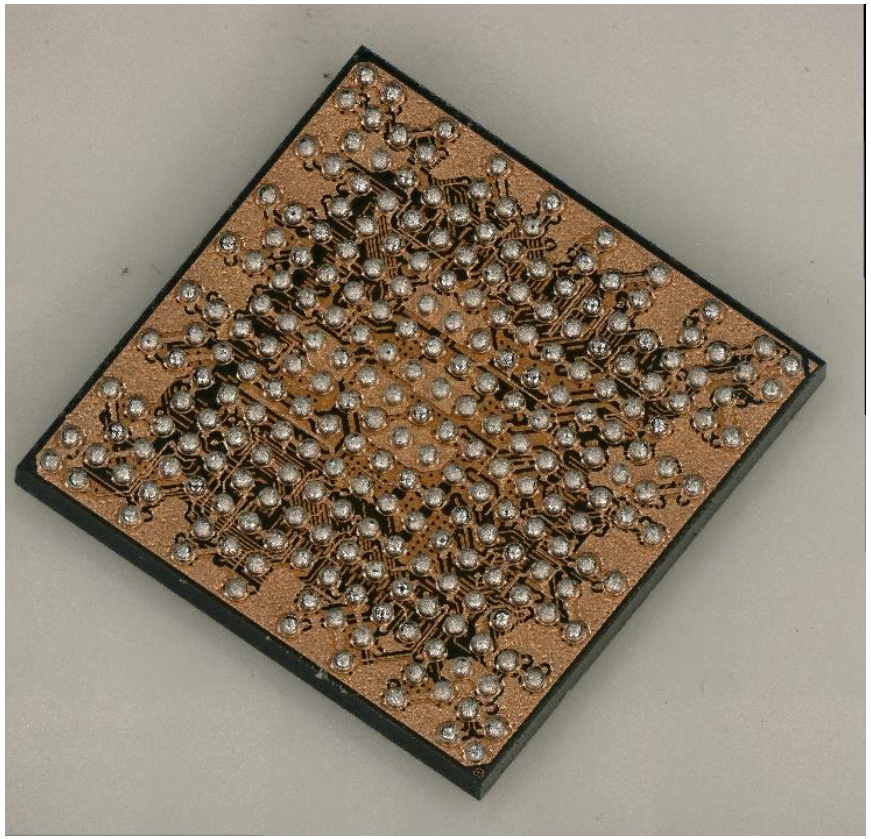
LG + saw at low metal density location



Silicon/EMC/Multi Layer RDL Integration



Developed FOWLP



- Die size = 4.5x4.5mm
- Package size = 7x7mm
- # of solder ball = 249
- Solder ball pitch = 0.4mm
- Package RDL stack up
  - Dielectric/Cu/Dielectric/Cu/Dielectric
  - Dielectric/Cu/Dielectric/Cu/Dielectric/UBM

FOWLP DOE

Solder	REP1	RDL 1	REP2	RDL2	REP3	UBM	Underfill
SACA	Diel 1	Copper	Diel 1	Copper	Diel 2	No	No
SACA	Diel 1	Copper	Diel 1	Copper	Diel 2	Yes	No
SACB	Diel 2	Copper	Diel 2	Copper	Diel 2	No	No
SACB	Diel 2	Copper	Diel 2	Copper	Diel 2	Yes	No

- SACA and SACB are different lead free solder alloys
- Diel 1 and Diel 2 are different dielectric materials
- REP - Repassivation, RDL - Redistribution Layer

Solder Alloy	Relative Tensile Strength	Relative Elongation
SACA	X	1.6Y
SACB	1.9X	Y

Reliability Qualification Summary

- Developed FOWLP passed all reliability qualification test

Test	Condition	Zero fail criteria	Result
Moisture Sensitivity Level 3 (MSL3)	30 °C/60% RH	168 h	Pass
Highly Accelerated Stress Test (HAST)	110°C / 85%RH/3.3V	528 h	Pass
Application-Level Temperature Cycling (AL-TC)	Ta = -40°C to 125°C	600 cycles	Pass
High Temperature Storage Life (HTSL)	Ta = 150°C	2000 h	Pass
Board Level Temperature Cycling (BL-TC)	Ta = -40°C to 125°C	500 cycles	Pass
Drop Impact Test	1500 g / 0.5 ms	30 drops	Pass

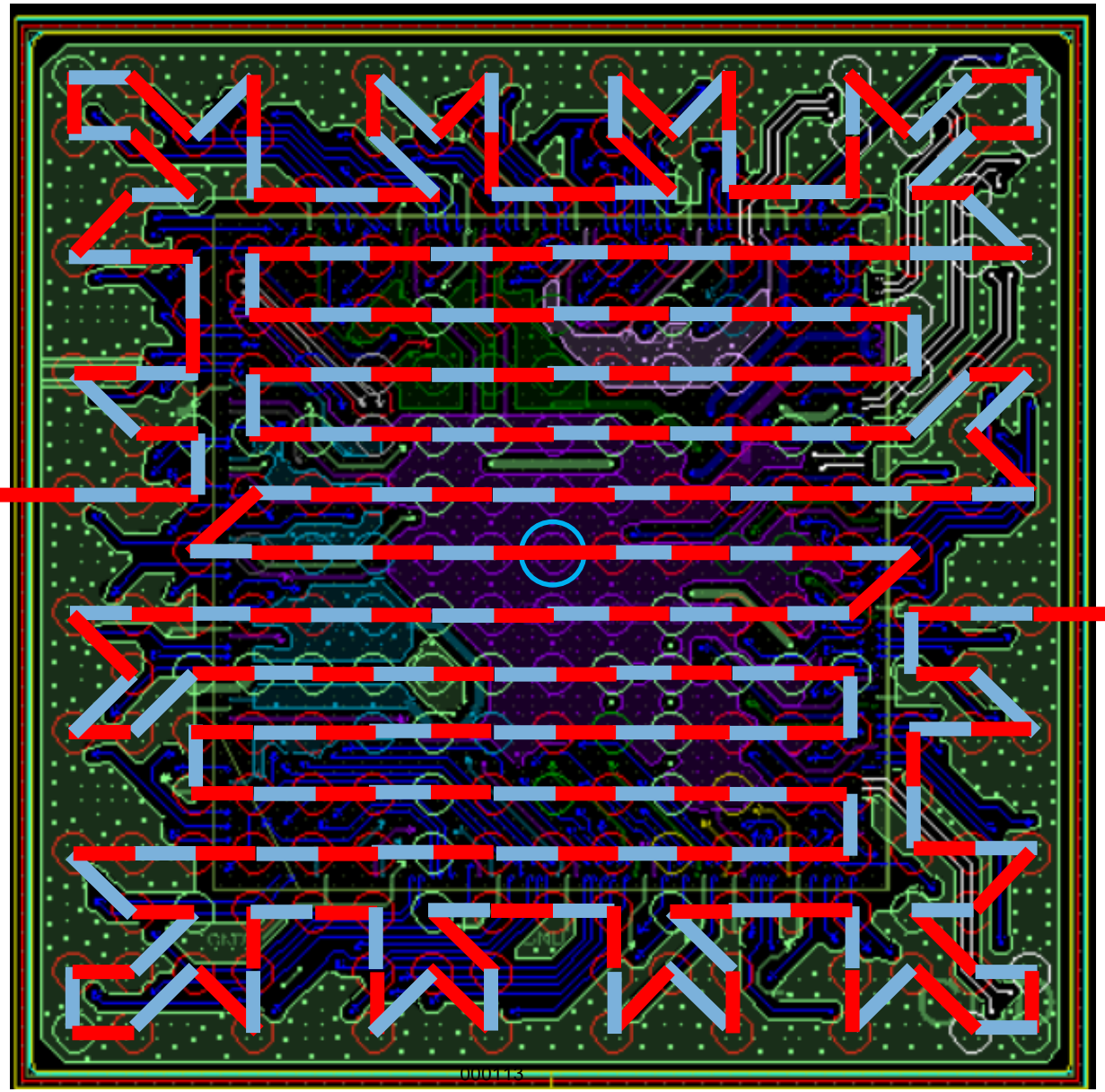
FOWLP Daisy Chain Interconnection

Key

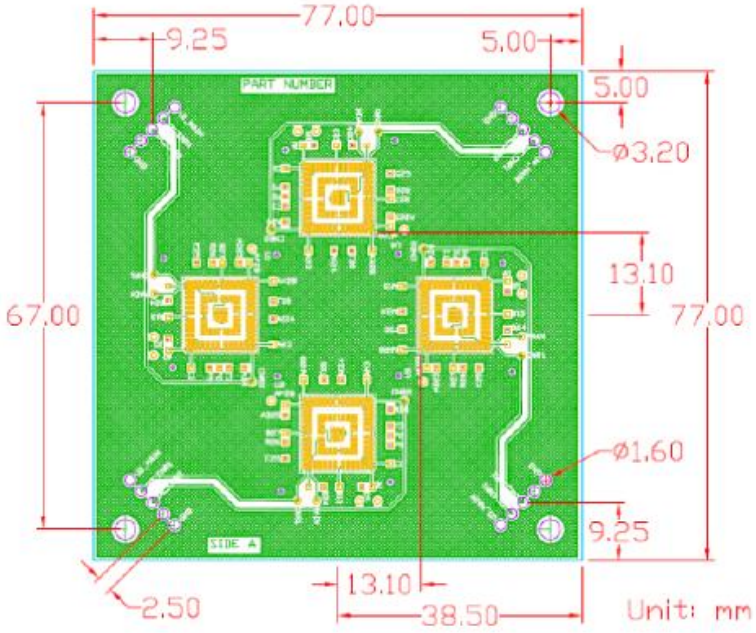
= Pkg

= PCB

= No connect
(odd number I/O)



FOWLP Board Layout for Reliability



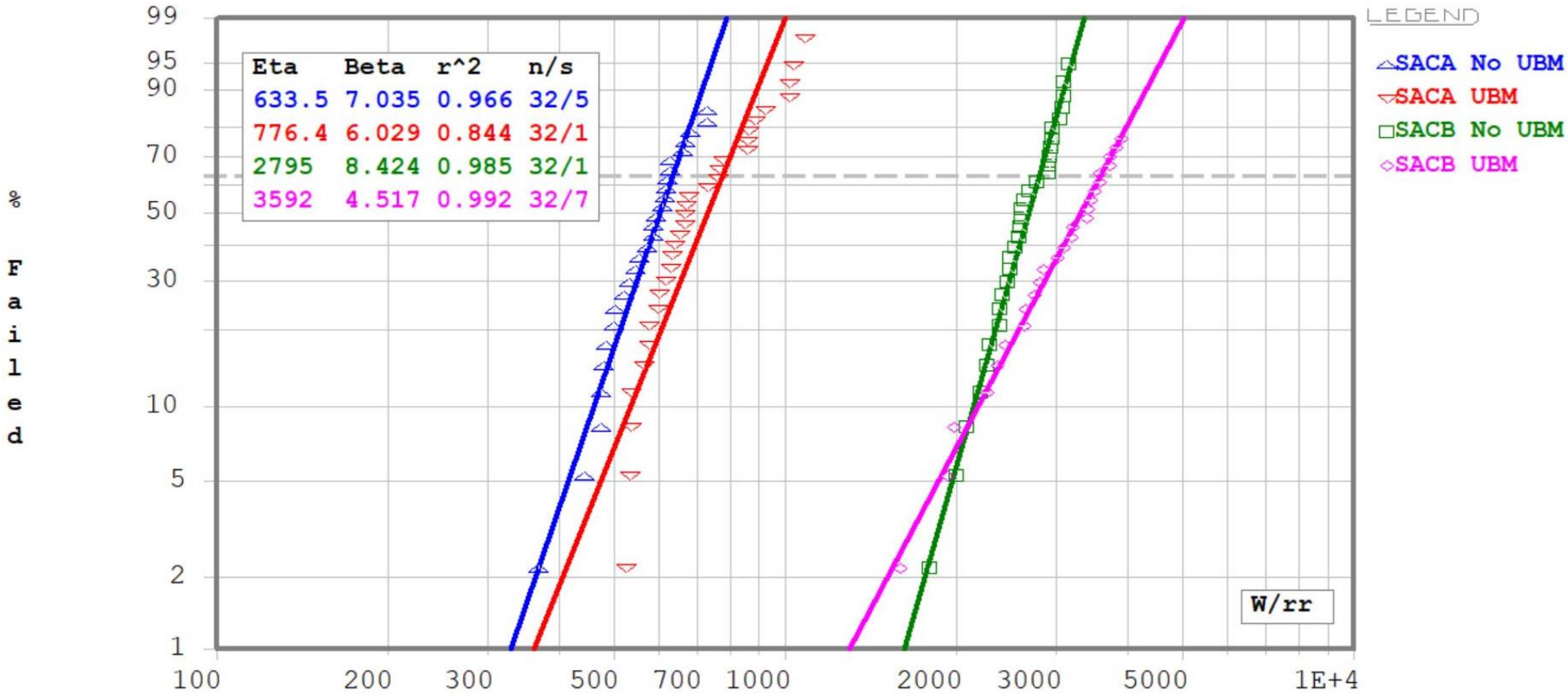
Board Layer	Thickness (um)	Copper Coverage (%)	Material
Solder Mask	20		LPI
Layer 1	25	Pads + traces (Via in Pad)	Copper
Dielectric 1-2	60		FR4*/**
Layer 2	25	40% 70%including daisy chain links	Copper
Dielectric 2-3	60		FR4**
Layer 3	18	70 %	Copper
Dielectric 3-4	100		FR4**
Layer 4	18	70 %	Copper
Dielectric 4-5	100		FR4**
Layer 5	18	70 %	Copper
Dielectric 5-6	130		FR4**
Layer 6	18	70 %	Copper
Dielectric 6-7	100		FR4**
Layer 7	18	70 %	Copper
Dielectric 7-8	100		FR4**
Layer 8	18	70 %	Copper
Dielectric 8-9	60		FR4**
Layer 9	25	70%	Copper
Dielectric 9-10	60		FR4*/**
Layer 10	25	Pads + Traces + daisy chain links (No Via in Pad)	Copper
Solder Mask	20		LPI

* If RCC used instead of FR4, it shall be reported.
** Suggested FR4 Material: NELCO N-4000-6, Panasonic R1551W or equivalent (shall be reported)

Board design was based on JESD22-B111A

FOWLP BLR-TC Reliability Results

- SACB alloy, which is selected as product POR significantly outperforms product reliability requirement of 500 cycle no fail



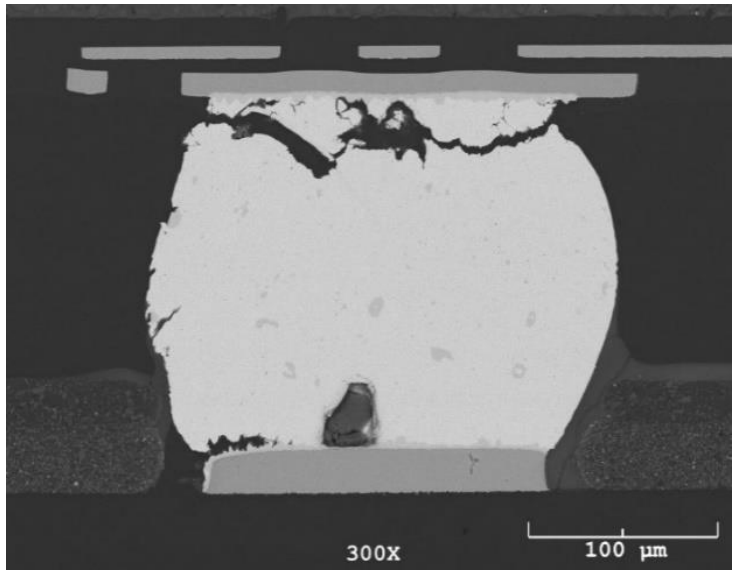
Relative BLR-TC Performance

- BLR-TC condition is Ta = -40° C to 125° C
- Product reliability requirement is no fail @ 500 cycles
- SACB alloy, which is selected as product POR significantly outperforms product reliability requirement

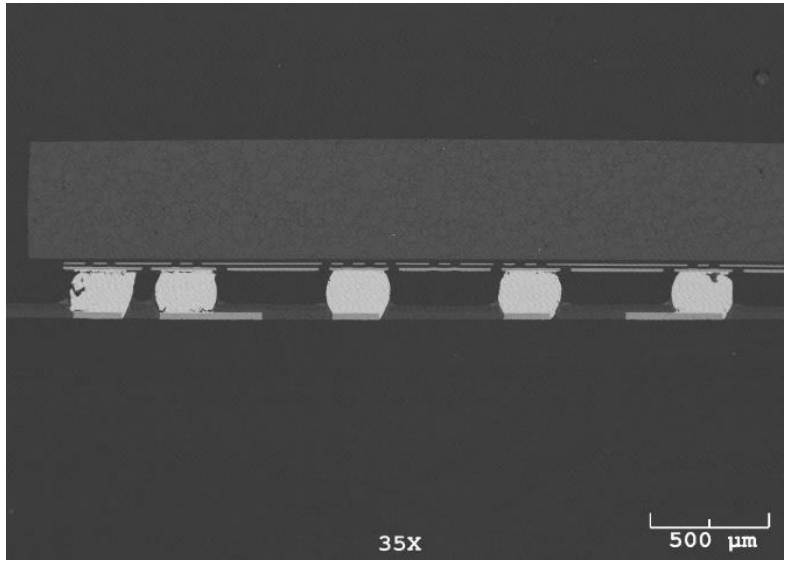
DOE Leg	First Fail (cycles)	63% Fail (cycles)
SACA - no UBM	369	633 (x)
SACA - UBM	525	776 (1.2x)
SACB - no UBM	1795	2795 (4.4x)
SACB - UBM	1598	3592 (5.7x)

BLR-TC Failure Analysis

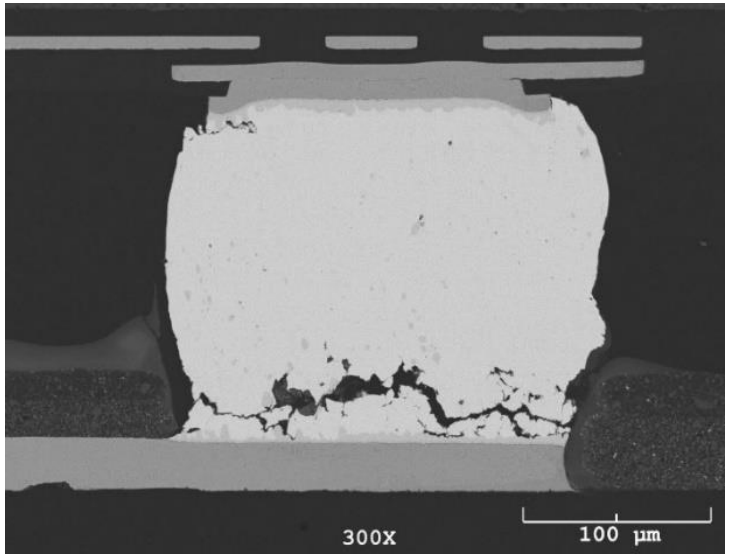
SACA no UBM, 475 cycles

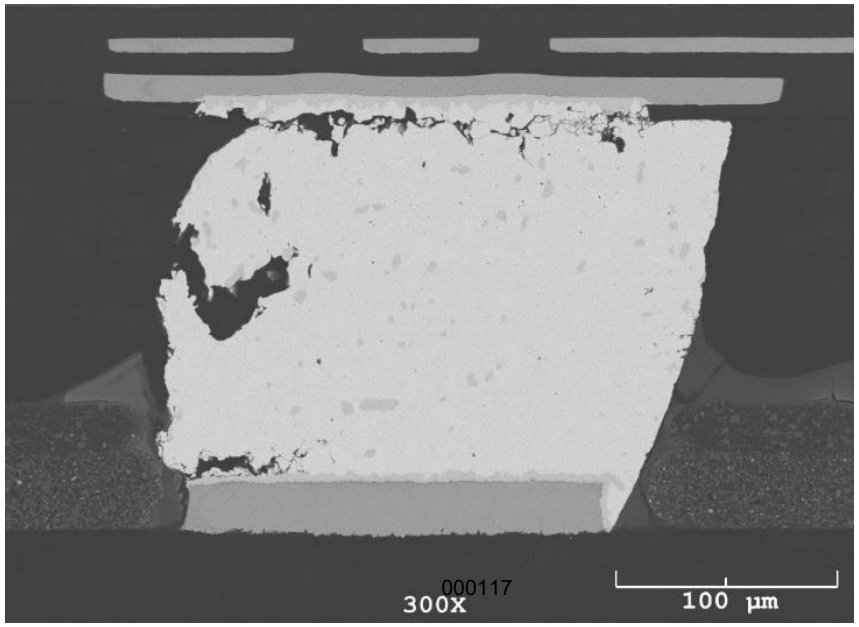


SACB no UBM, 3164 cycles



SACA UBM, 525 cycles



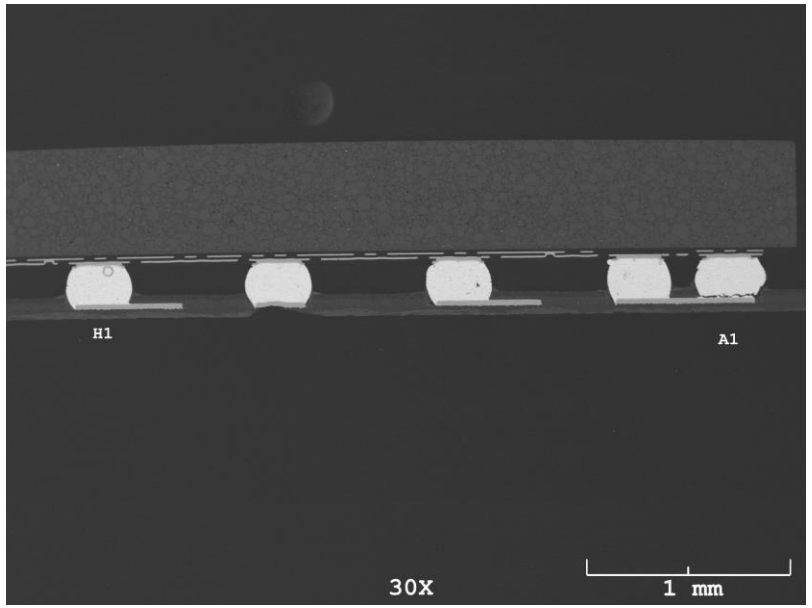


SACB alloy, no UBM which is selected as product POR significantly outperforms product reliability requirement of no fail at 500 cycle

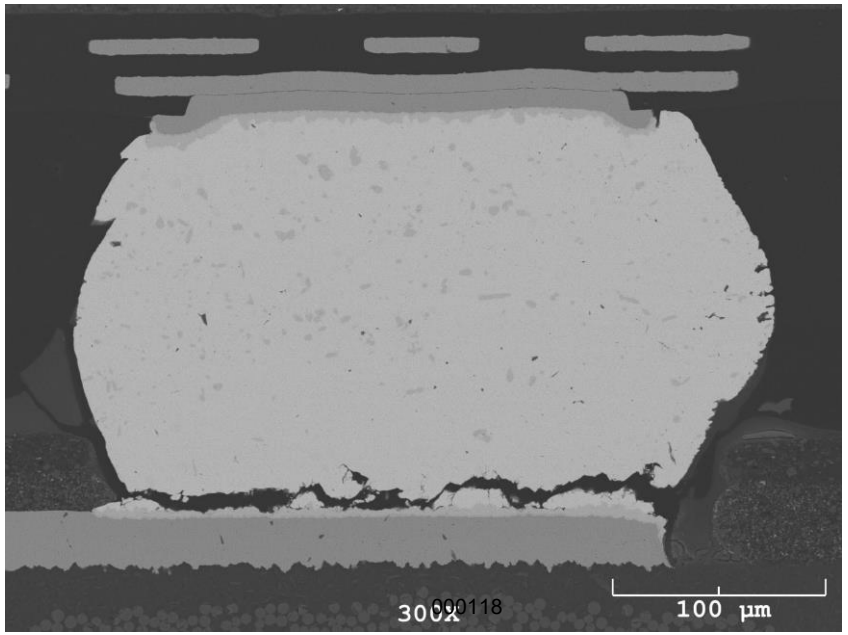
BLR-TC Failure Analysis

- Failure analysis after 3985 cycles
- SACB alloy with UBM significantly outperforms product reliability requirement of no fail @ 500 cycle
- RDL crack initiation is seen after 3985 cycles, but yet no crack propagation

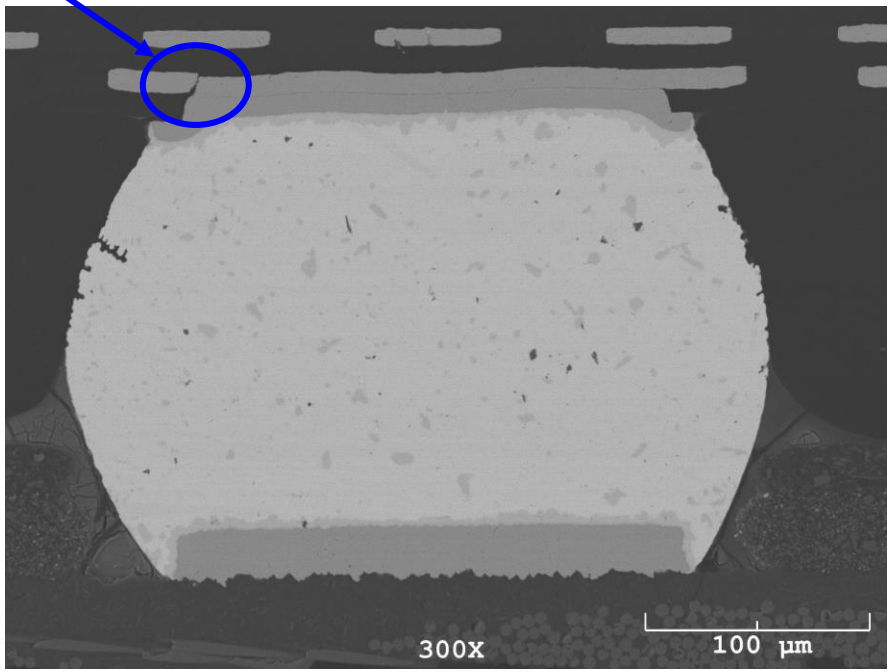
SACB UBM



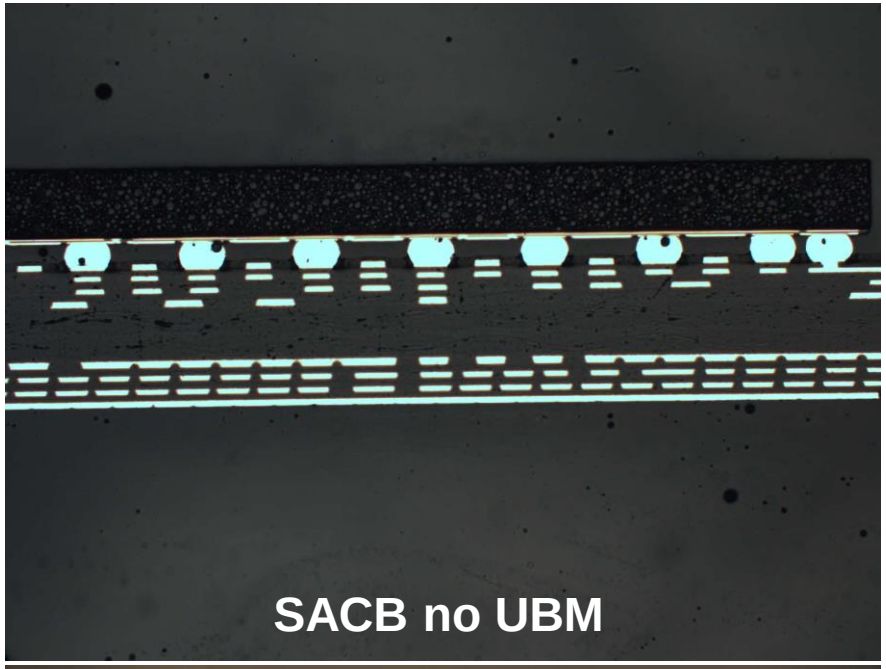
SACB UBM, Corner Ball

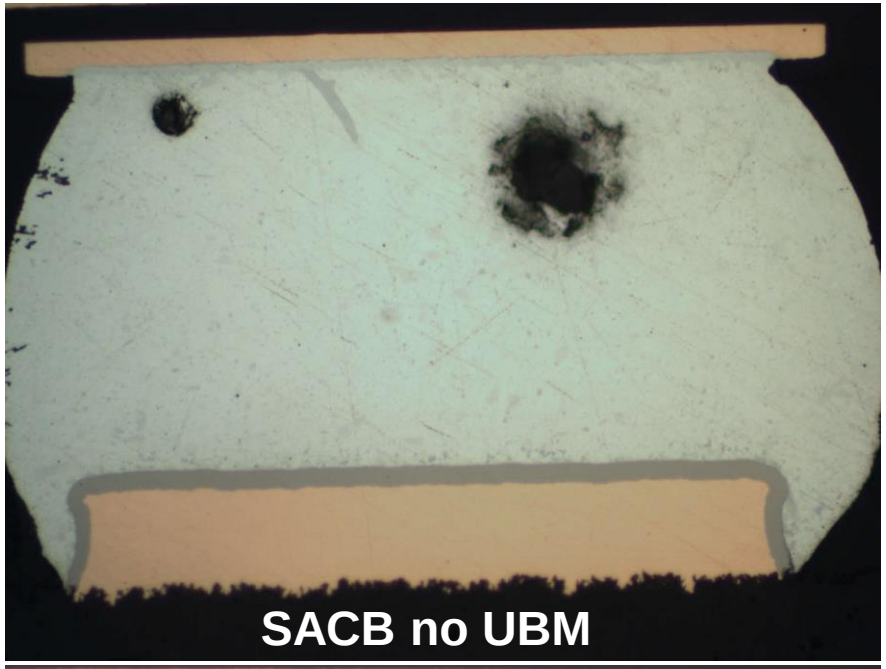


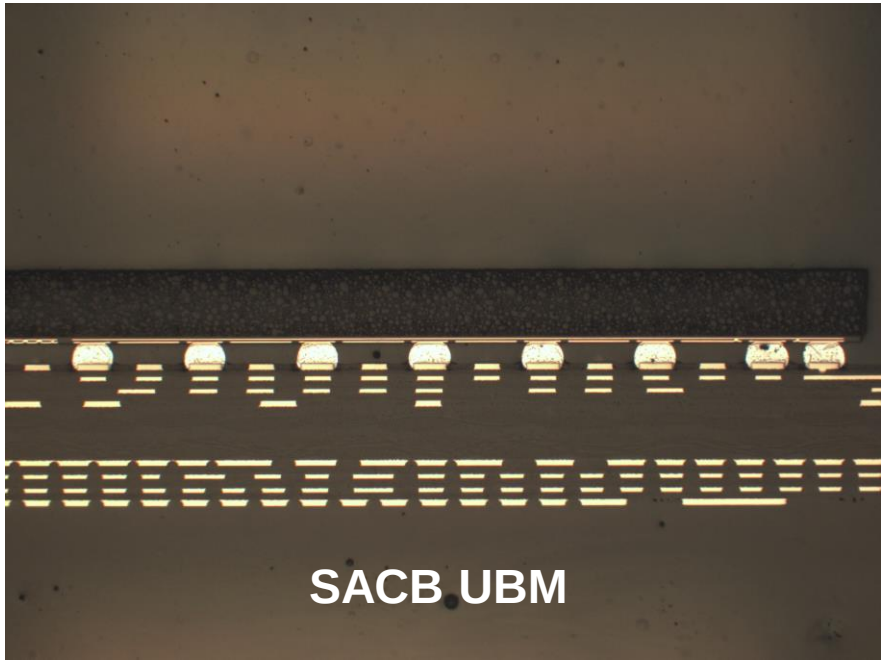
SACB UBM, Non Corner Ball

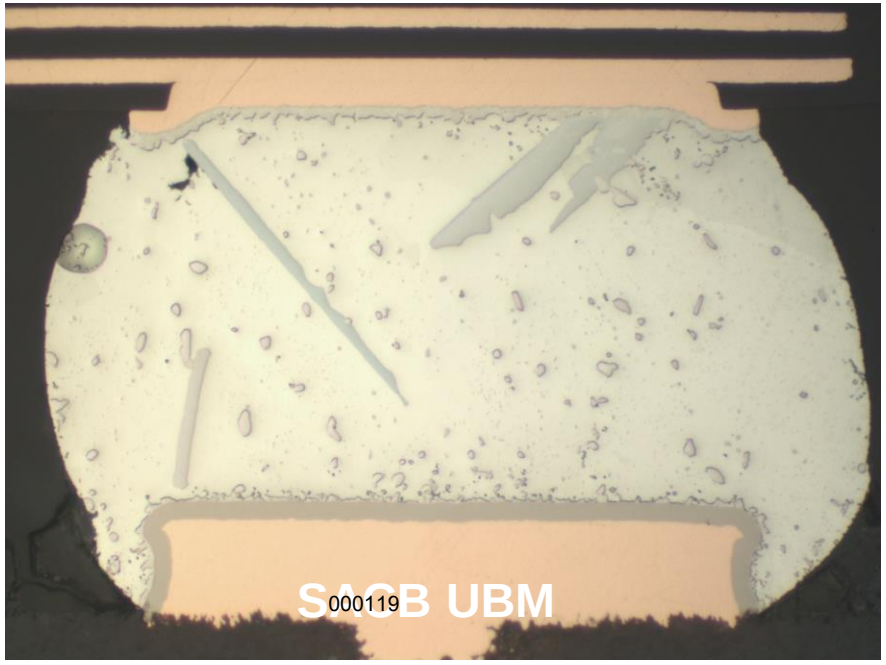


Product on Board - Application Level Temperature Cycle



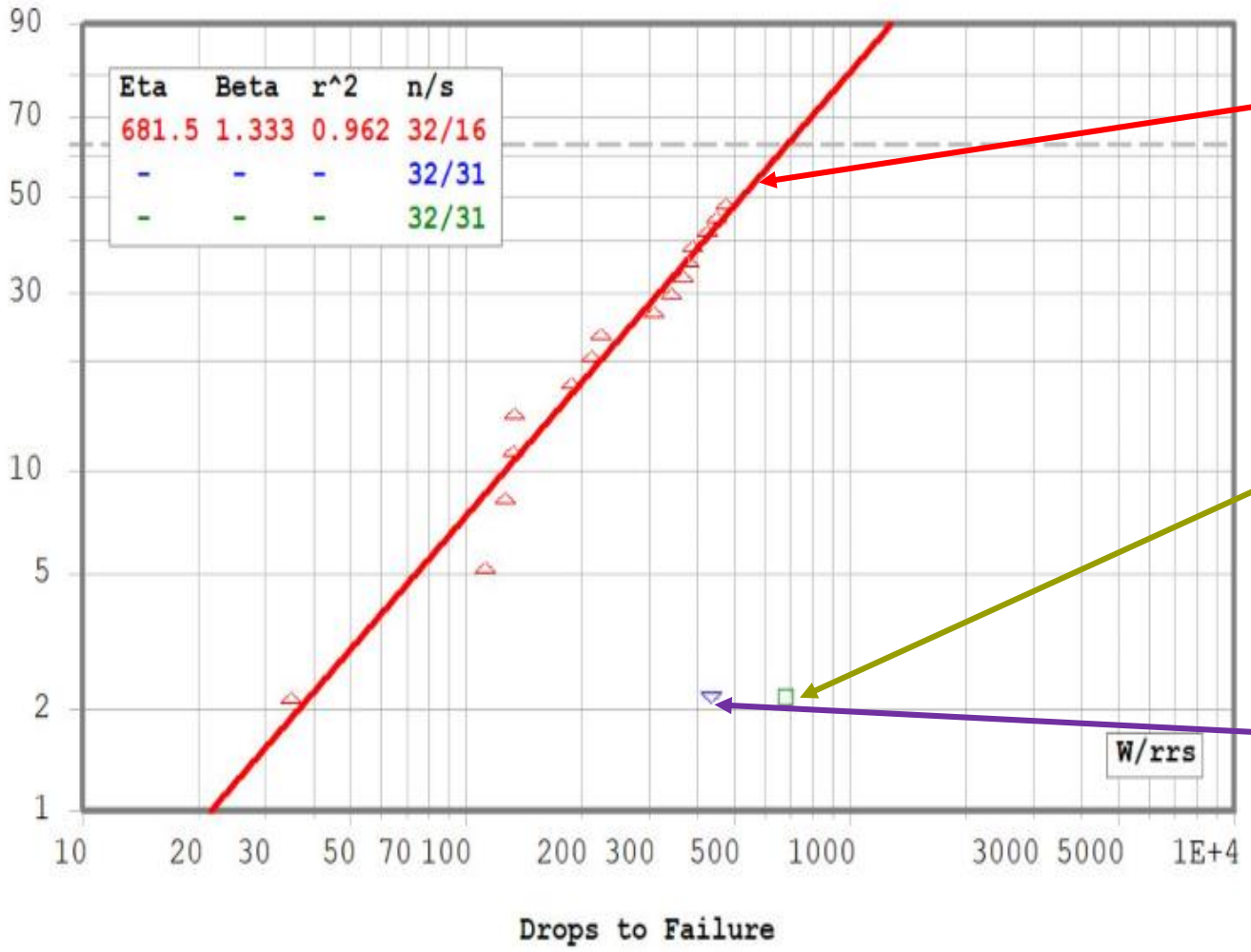






- Both SACB no UBM and SACB UBM have zero product FT fail after 1500 cycles
- SACB alloy significantly outperforms product reliability requirements of 600 cycle no fail

Relative BLR-Drop Performance



SACA – no UBM
- First fail – 35 drops
- 50% fail – 500 drops

SACB – UBM
- Only one fail @ 679 drops
- Testing stopped at 1000 drops

SACB – no UBM
- Only one fail @ 432 drops
- Testing stopped at 1000 drops

- **SACB alloy significantly outperforms product reliability requirements of 30 drops no fail**

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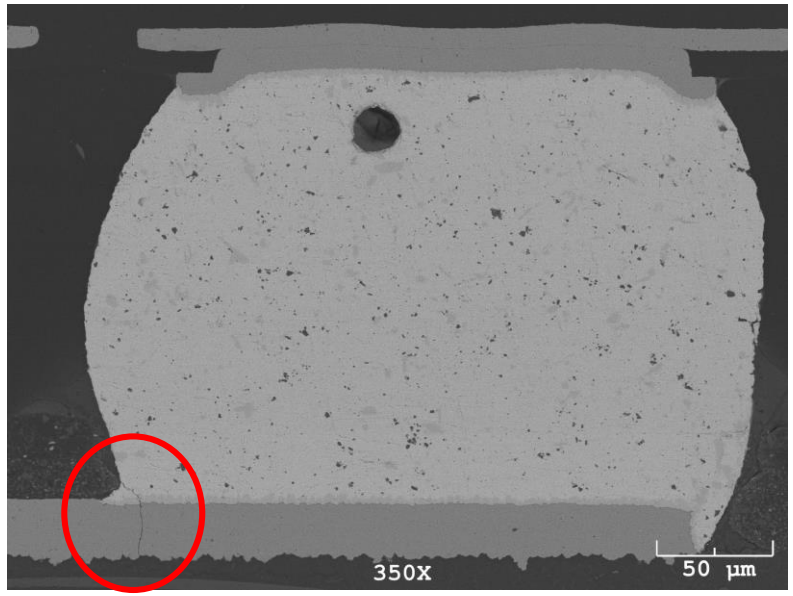
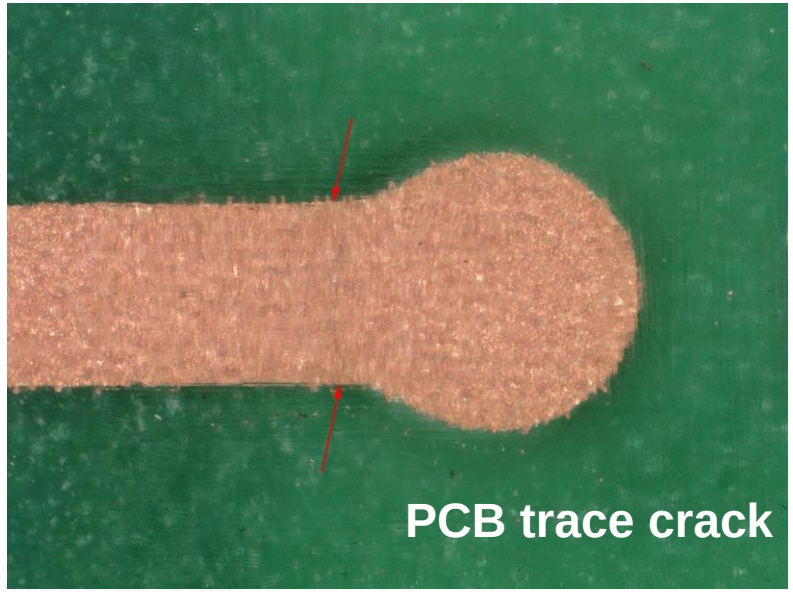
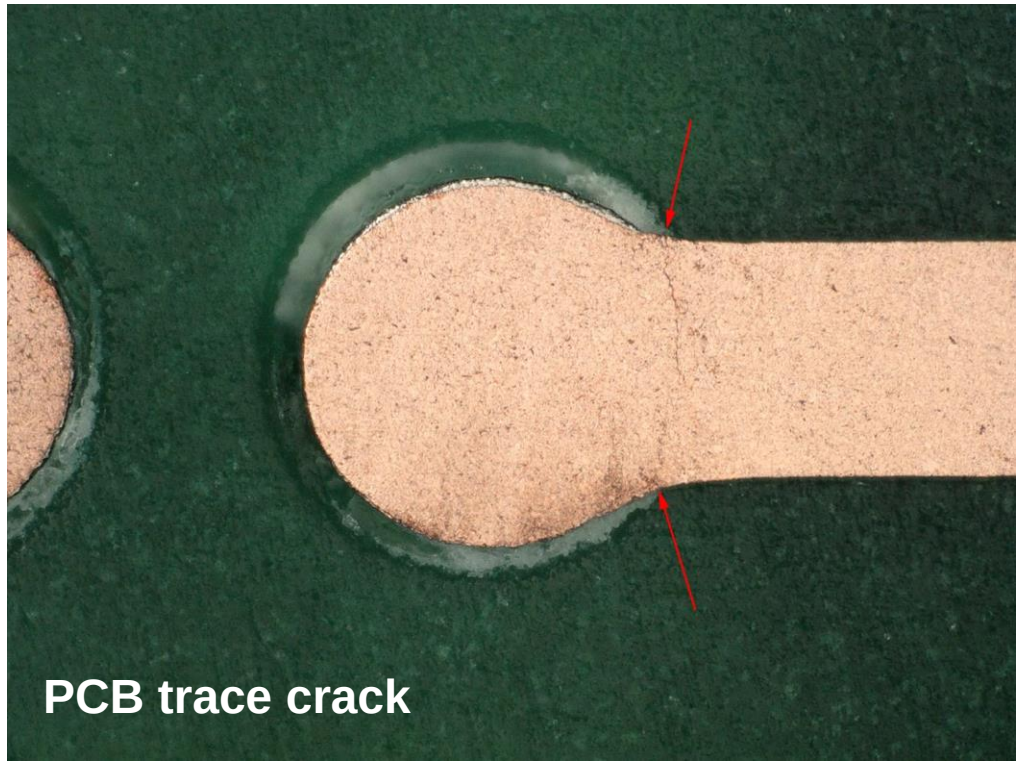
BLR – Drop Test FA

SACB UBM – 679 drops





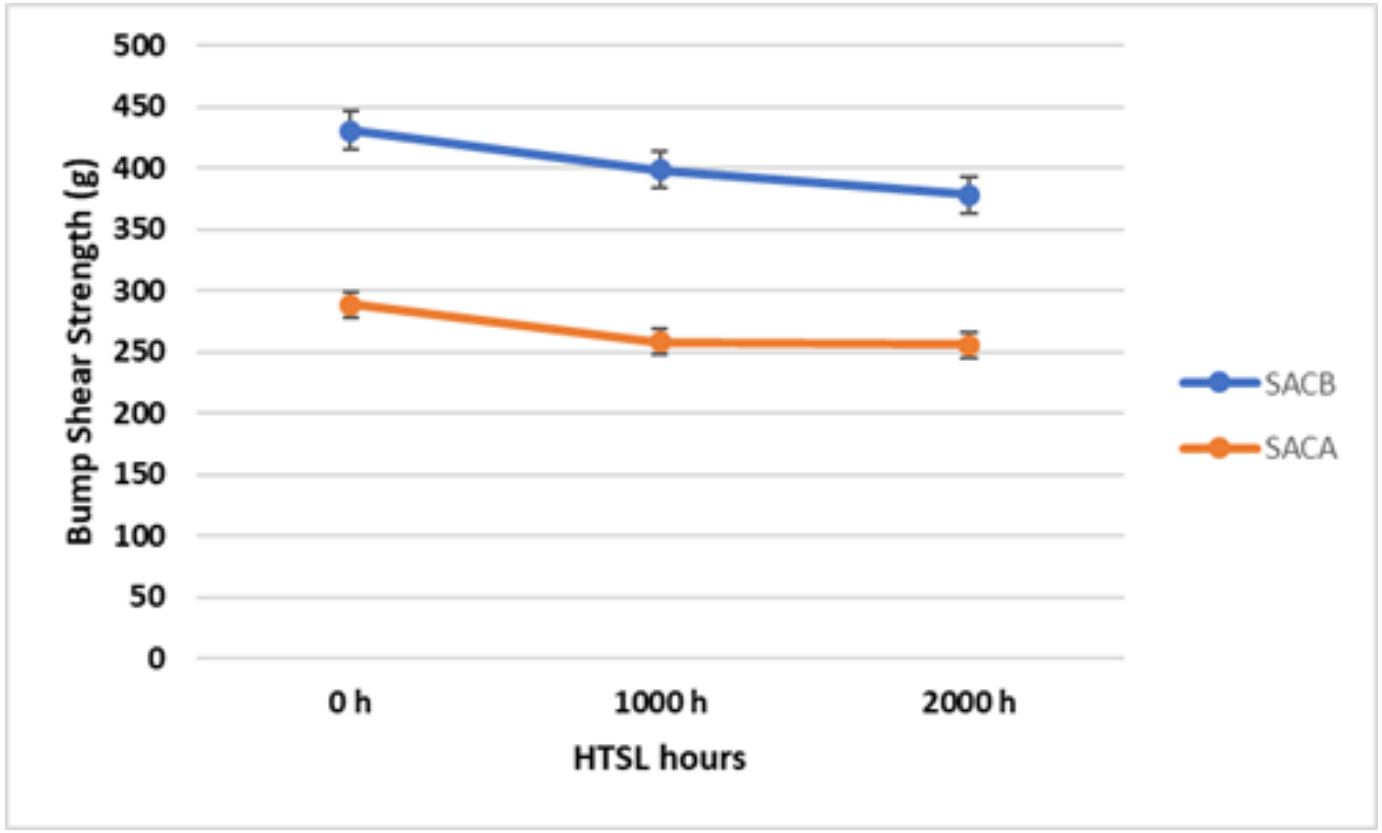
SACB No UBM – 432 drops



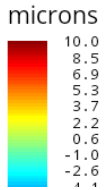
- No package related fails found till 1000 drops testing for both UBM and no UBM legs
- SACB alloy significantly outperforms product reliability requirements of 30 drops no fail

Bump Shear Comparison (SACA vs SACB)

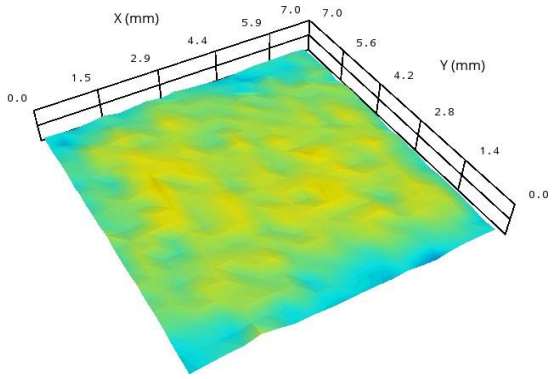
- **SACB alloy has >50% bump shear strength than SACA alloy, even after 150°C 2000 h aging**



FOWLP SACB No UBM – TherMoir Warpage

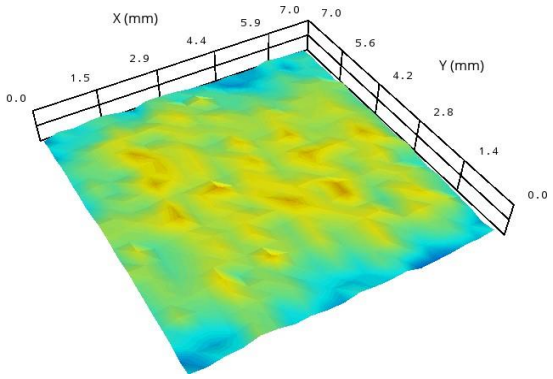


25° C



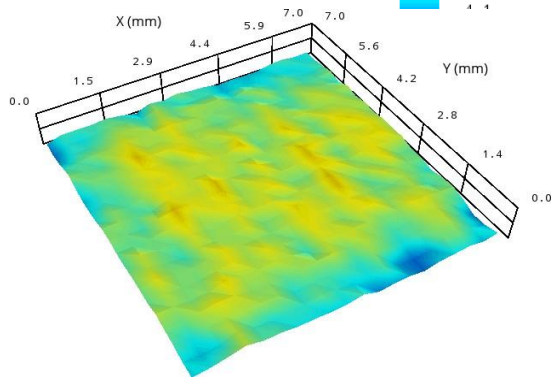
Coplanarity = 7.7 microns

100° C



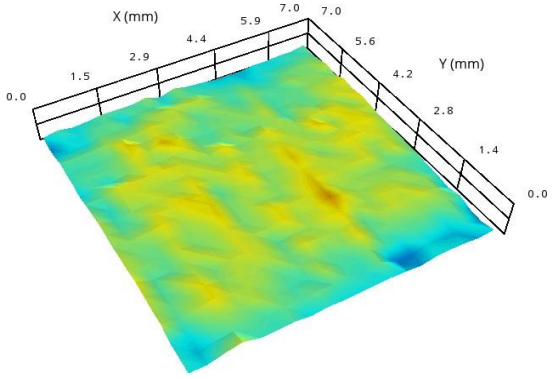
Coplanarity = 9.5 microns

150° C



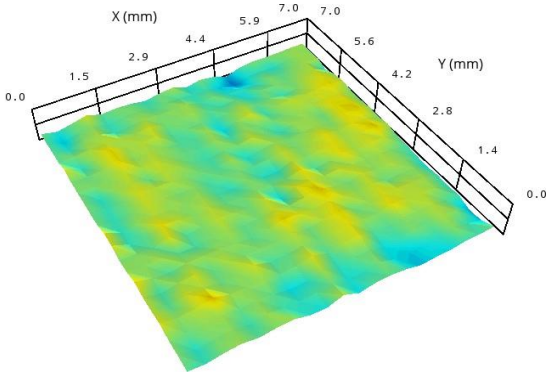
Coplanarity = 8.9 microns

183° C



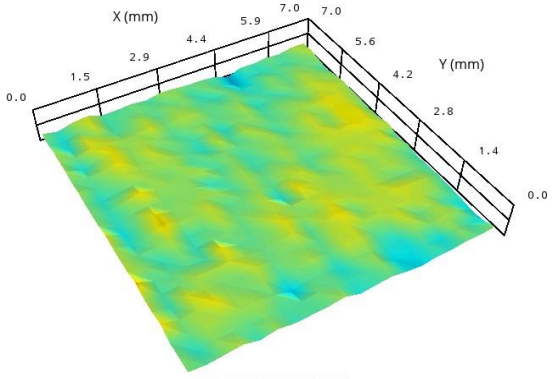
Coplanarity = 9.2 microns

245° C



Coplanarity = 8.6 microns

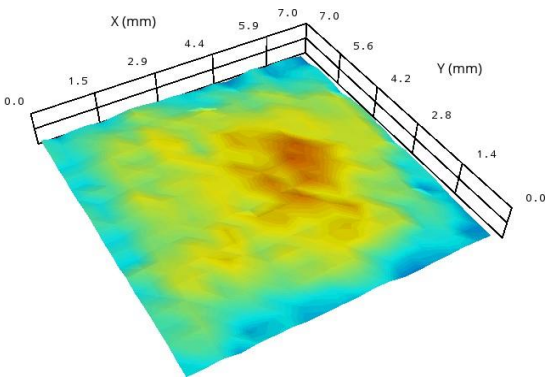
260° C



Coplanarity = 7.6 microns

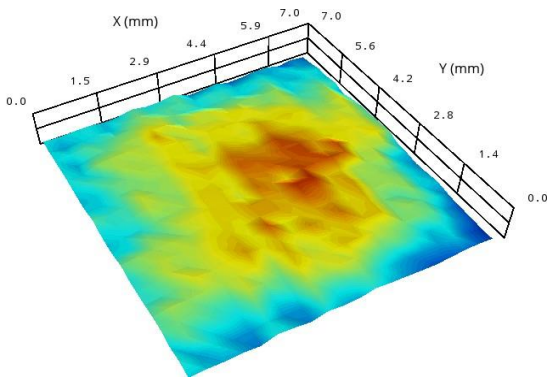
FOWLP SACB UBM – ThermoIr Warpage

25° C



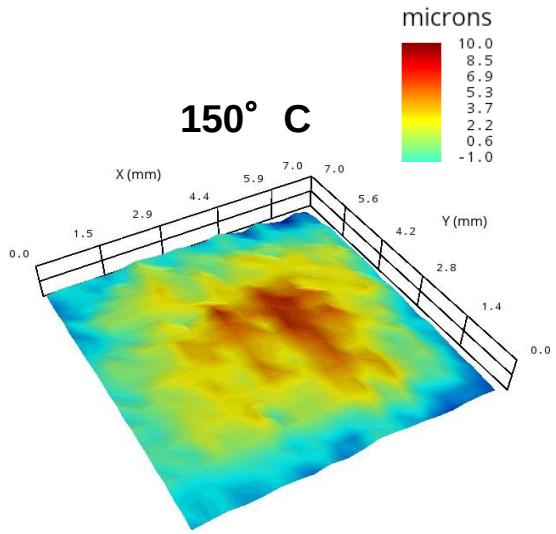
Coplanarity = 10.3 microns

100° C



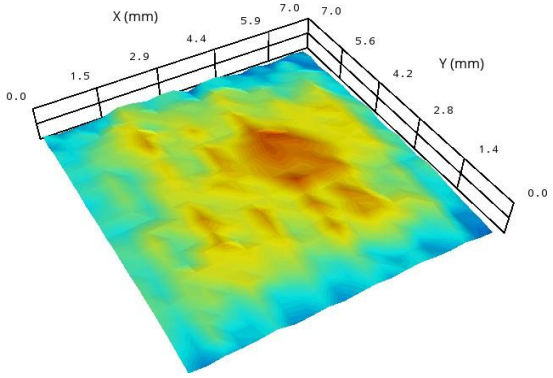
Coplanarity = 13.2 microns

150° C



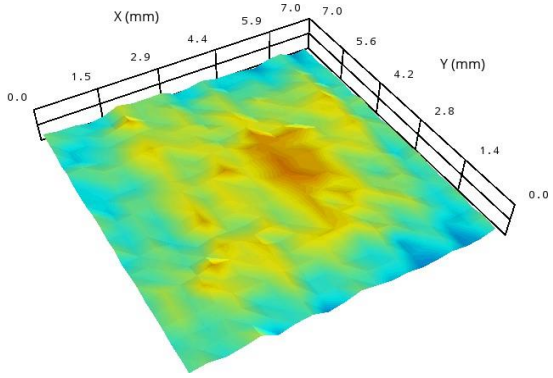
Coplanarity = 14.5 microns

183° C



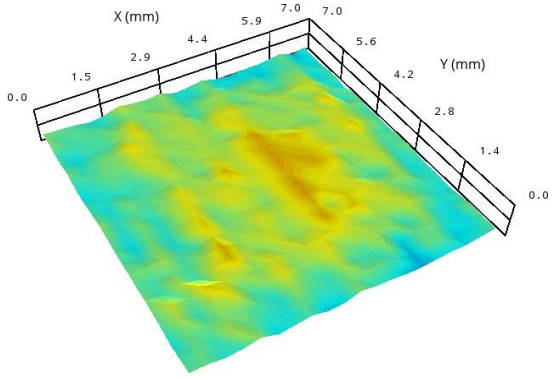
Coplanarity = 11.8 microns

245° C



Coplanarity = 9.7 microns

260° C



Coplanarity = 8.0 microns

Summary & Conclusions

- Extensive solder alloy, package RDL stack up DOE were used to down select product package POR
- Developed FOWLP met/exceeded all product reliability requirements - BLR-TC, drop, AL-TC, BHAST, HTSL
- Using stiffer solder alloy SACB in conjunction with the optimized package RDL stack up led to:
  - For no UBM case, BLR-TC characteristic life improvement of 341%
  - For UBM case, BLR-TC characteristic life improvement of 363%
  - No package related fail till 1000 drops

Summary & Conclusions

- Developed FOWLP had 0 fail during product board level reliability testing for up to 1500 cycles
- Excellent chip package integration across all interconnect levels (die-package-board) was achieved

Thank You for Your Attention!

Q & A